

J509, J510, J511 Current Regulator Diode

Features

- InterFET [N0016H Geometry](#)
- Low Noise: 5 nV/VHz Typical
- Low Capacitance: 2pF Typical
- RoHS Compliant
- SMT, TH, and Bare Die Package options.

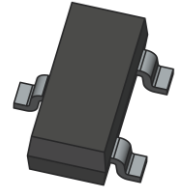
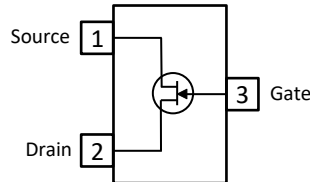
Applications

- Current Regulation
- Current Limiting

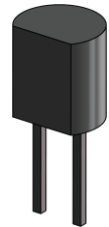
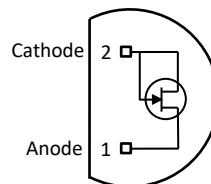
Description

The 50V InterFET J509, J510, and J511 JFET's are targeted for current regulation and limiting applications. The SOT23 package is pinned out as a standard JFET and is required by the user to connect the Gate to the Source or Drain.

SOT23 Top View



TO-92 Bottom View



Product Summary

Parameters	J509 Min	J510 Min	J511 Min	Unit
V _{OP} Peak Operating Voltage	50	50	50	V
I _{F1} Forward Current	2.4	2.9	3.8	mA
V _L Limiting Voltage	2.5 (typ)	2.8 (typ)	3.0 (typ)	V

Ordering Information Custom Part and Binning Options Available

Part Number	Description	Case	Packaging
J509; J510; J511	Through-Hole	TO-92-2L	Bulk
SMPJ509; SMPJ510; SMPJ511	Surface Mount	SOT23	Bulk
SMPJ509TR; SMPJ510TR; SMPJ511TR	7" Tape and Reel: Max 3,000 Pieces 13" Tape and Reel: Max 9,000 Pieces	SOT23	Minimum 1,000 Pieces Tape and Reel
J509COT; J510COT; J511COT	Chip Orientated Tray (COT Waffle Pack)	COT	400/Waffle Pack
J509CFT; J510CFT; J511CFT	Chip Face-up Tray (CFT Waffle Pack)	CFT	400/Waffle Pack



Disclaimer: It is the Buyers responsibility for designing, validating and testing the end application under all field use cases and extreme use conditions. Guaranteeing the application meets required standards, regulatory compliance, and all safety and security requirements is the responsibility of the Buyer. These resources are subject to change without notice.

Electrical Characteristics

Maximum Ratings (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Value	Unit
V_{OP} Peak Operating Voltage	50	V
I_{FG} Continuous Forward Gate Current	20	mA
P_D Continuous Device Power Dissipation	360	mW
P Power Derating	3.27	mW/ $^\circ\text{C}$
T_J Operating Junction Temperature	-55 to 135	$^\circ\text{C}$
T_{STG} Storage Temperature	-55 to 135	$^\circ\text{C}$

Static Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

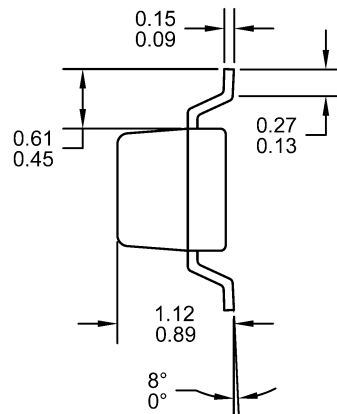
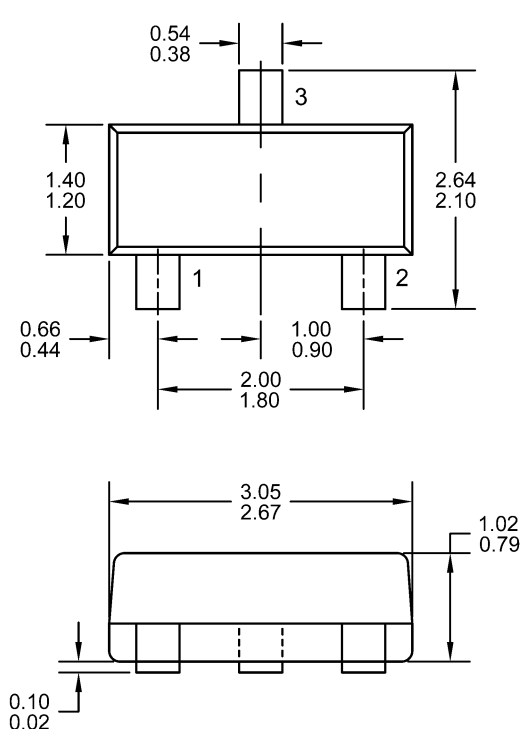
Parameters	Conditions	J509			J510			J511			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{F1} Forward Current	$V_F = 25\text{V}$	2.4	3.0	3.6	2.9	3.6	4.3	3.8	4.7	5.6	mA
V_L Limiting Voltage	$I_F = 0.9 I_{F(MIN)}$		2.5	3.5		2.8	3.9		3.0	4.2	V
V_{OP} Peak Operating Voltage	$I_F = 1.1 I_{F(MAX)}$	50			50			50			V

Dynamic Characteristics (@ $T_A = 25^\circ\text{C}$, Unless otherwise specified)

Parameters	Conditions	J509			J510			J511			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Z_{fi} Dynamic Impedance	$V_F = 25\text{V}$, $f = 1\text{kHz}$	0.15	0.6		0.15	0.5		0.12	0.3		$M\Omega$
C_F Anode-Cathode Capacitance	$V_F = 25\text{V}$, $f = 1\text{kHz}$		2			2			2		pF

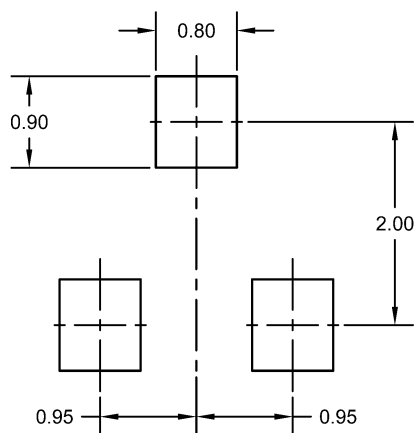
SOT23 (TO-236AB) Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.12 grams
3. Molded plastic case UL 94V-0 rated
4. For Tape and Reel specifications refer to InterFET CTC-021 Tape and Reel Specification, Document number: IF39002
5. Bulk product is shipped in standard ESD shipping material
6. Refer to JEDEC standards for additional information.

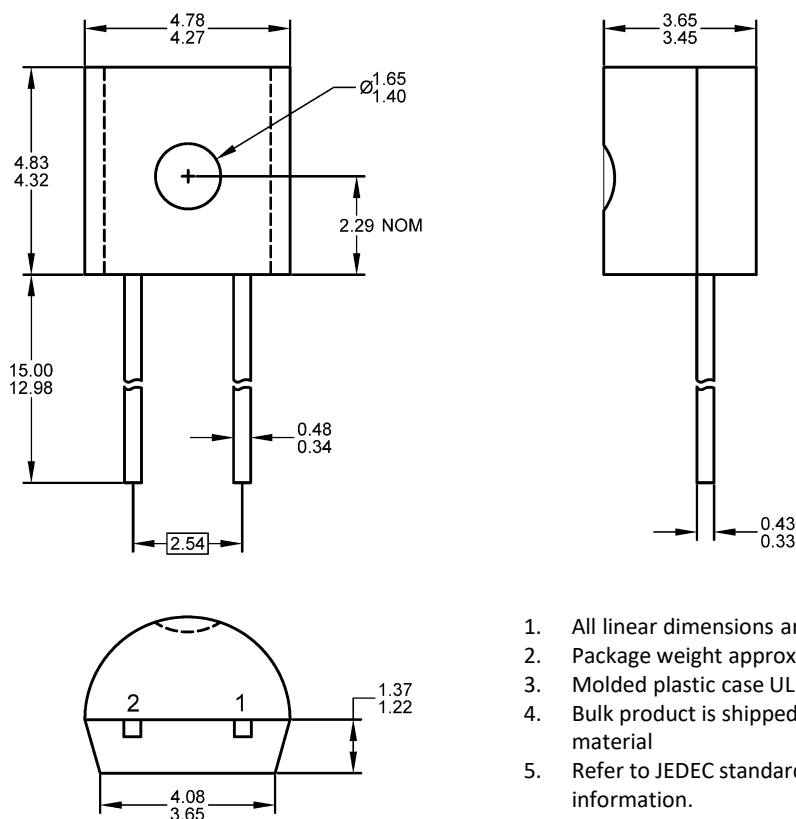
Suggested Pad Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided for reference only. A more robust pattern may be desired for wave soldering.

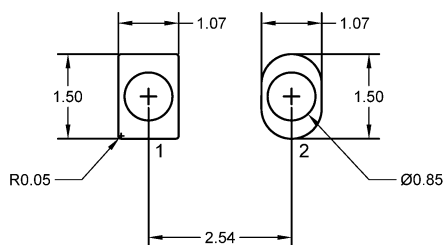
TO-92-2L Mechanical and Layout Data

Package Outline Data



1. All linear dimensions are in millimeters.
2. Package weight approximately 0.19 grams
3. Molded plastic case UL 94V-0 rated
4. Bulk product is shipped in standard ESD shipping material
5. Refer to JEDEC standards for additional information.

Suggested Through-Hole Layout



1. All linear dimensions are in millimeters.
2. The suggested land pattern dimensions have been provided as a straight lead reference only. A more robust pattern may be desired for wave soldering and/or bent lead configurations.