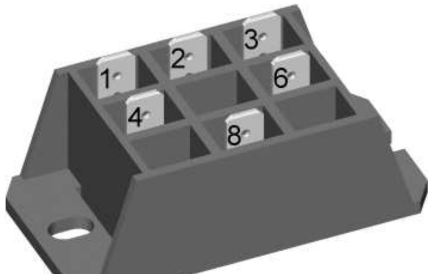
Half Controlled Single Phase Rectifier Bridge

with Freewheeling Diode

I_{dAVM} = 32 A
V_{RRM} = 800-1600 V

Part numbers

V_{RSM} V_{DSM} V	V_{RRM} V_{DRM} V	Type
900	800	VHF 28-08io5
1300	1200	VHF 28-12io5
1700	1600	VHF 28-16io5



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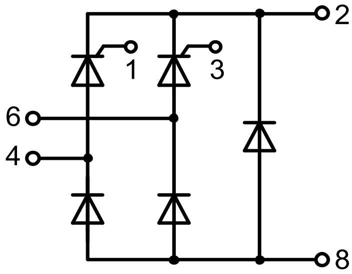

Features / Advantages:

- Planar passivated chips
- Space and weight savings
- Improved temperature & power cycling

Applications:

- Supply for DC power equipment
- DC motor control

Package: FO-F

- Isolation Voltage: 3600 V~
- DCB ceramic base plate
- 1/4" fast-on terminals
- Easy to mount with two screws
- RoHS compliant

Diodes				Ratings		
Symbol	**Definitions**	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
I_{dAV} I_{dAVM}	*avarage DC output current* *max. avarage DC output current*	module $T_K = 85°C$ for resistive load			28 32	A A
I_{FRMS}, I_{TRMS}	*RMS forward current*	per leg			23	A
I_{FSM}, I_{TSM}	*max. surge forward current*	t = 1 0 ms (50 Hz), sine $T_{VJ} = 45°C$ t = 8.3 ms (60 Hz), sine; $V_R = 0$ V			300 330	A A
		t = 1 0 ms (50 Hz), sine $T_{VJ} = 125°C$ t = 8.3 ms (60 Hz), sine; $V_R = 0$ V			270 300	A A
I^2t	*I^2t value for fusing*	t = 1 0 ms (50 Hz), sine $T_{VJ} = 45°C$ t = 8.3 ms (60 Hz), sine; $V_R = 0$ V			440 455	A^2s A^2s
		t = 1 0 ms (50 Hz), sine $T_{VJ} = 125°C$ t = 8.3 ms (60 Hz), sine; $V_R = 0$ V			365 370	A^2s A^2s
$(di/dt)_{cr}$	*critical rate of rise of current*	f = 50 Hz, t_P = 200 µs, $V_D = {}^2/_3 V_{DRM}$ $T_{VJ} = 125°C$ I_G = 0.3 A, di_G/dt = 0.3 A/µs repetitive, I_T = 50 A non repetitive, $I_T = ½ I_{dAV}$			 150 500	 A/µs A/µs
$(dv/dt)_{cr}$	*critical rate of rise of voltage*	$V_D = {}^2/_3 V_{DRM}$ $T_{VJ} = 125°C$ $R_{GK} = \infty$; method 1 (linear voltage rise)			1000	V/ µs
V_{RGM}	*max. reverse gate voltage*				10	V
P_{GM}	*max. gate power dissipation*	$I_T = I_{TAVM}$ t_p = 30 µs $T_{VJ} = 125°C$ t_p = 500 µs t_p = 10 ms			10 5 1	W W W
P_{GAVM}	*max. average gate power dissipation*				0.5	W

Thyristors				Ratings		
Symbol	**Definitions**	**Conditions**	**min.**	**typ.**	**max.**	**Unit**
I_R, I_D	*reverse, drain current*	$V_R = V_{RRM}$; $V_D = V_{DRM}$ $T_{VJ} = 25°C$ $T_{VJ} = 125°C$			0,3 5	mA mA
V_T, V_F	*forward voltage*	I_T, I_F = 45 A $T_{VJ} = 25°C$			1.6	V
V_{T0} r_T		For power-loss calculations only $T_{VJ} = 125°C$		0.9 15		V mΩ
V_{GT}	*gate trigger voltage*	V_D = 6 V $T_{VJ} = 25°C$ $T_{VJ} = -40°C$			1.0 1.2	V V
I_{GT}	*gate trigger current*	V_D = 6 V $T_{VJ} = 25°C$ $T_{VJ} = -40°C$ $T_{VJ} = 125°C$			65 80 50	mA mA mA
V_{GD} I_{GD}	*gate non-trigger voltage* *non-trigger gate current*	$V_D = {}^2/_3 V_{DRM}$ $T_{VJ} = 125°C$			0.2 5	V mA
I_L	*latching current*	I_G = 0.3 A, t_G = 30 µs $T_{VJ} = 25°C$ di_G/dt = 0.3 A/µs $T_{VJ} = -40°C$ $T_{VJ} = 125°C$			150 200 100	mA mA mA
I_H	*holding current*	V_D = 6 V, $R_{GK} = \infty$ $T_{VJ} = 25°C$			100	ns
t_{gd}	*gate controlled delay time*	$V_D = ½ V_{DRM}$ $T_{VJ} = 25°C$ I_G = 0.3 A, di_G/dt = 0.3 A/µs		2		µs
t_q Q_r	*turn-off time* *reverse recovery charge*	I_T = 15 A, t_P = 300 µs, V_R = 100 V; $T_{VJ} = 125°C$ di/dt = -10 A/µs, dv/dt = 20 V/µs, $V_D = {}^2/_3 V_{DRM}$		150 75		µs µC
R_{thJC}	*thermal resistance junction to case*	per thyristor (diode); DC current per module			1.4 0.35	K/W K/W
R_{thJH}	*thermal resistance junction to heatsink*	per thyristor (diode); DC current per module		2.0 0.5		K/W K/W

Data according to IEC 60747 and refer to a single thyristor/diode unless otherwise stated.

IXYS reserves the right to change limits, test conditions and dimensions.

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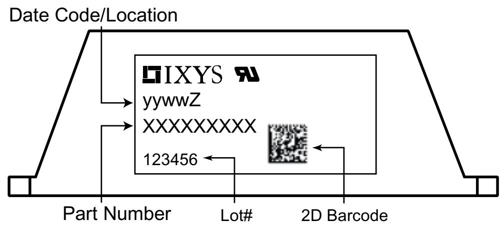
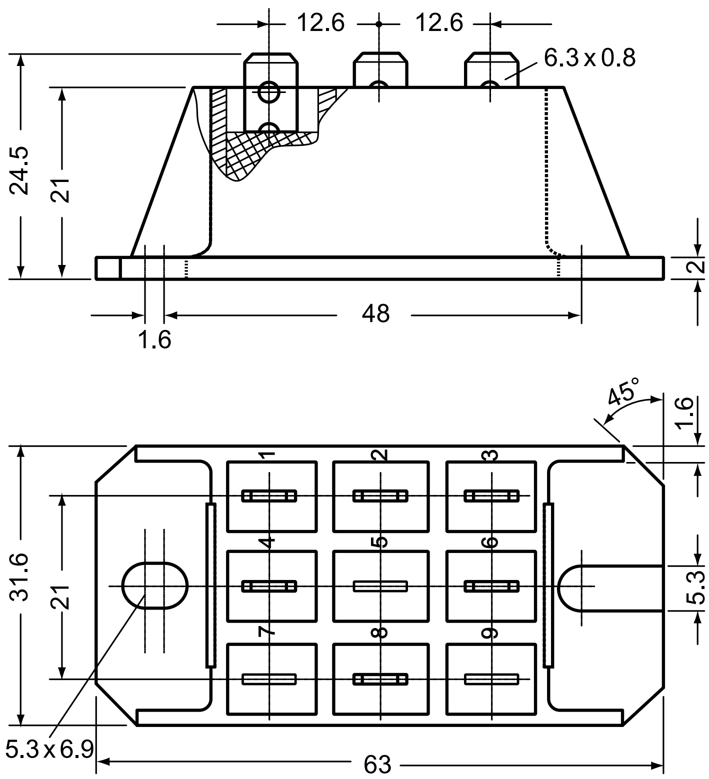
Package	FO-F				Ratings			
Symbol	**Definitions**	**Conditions**			**min.**	**typ.**	**max.**	**Unit**
I_{RMS}	*RMS current*	per terminal					100	A
T_{VJ}	*virtual junction temperature*				-40		125	°C
T_{op}	*operation temperature*				-40		100	°C
T_{stg}	*storage temperature*				-40		125	°C
Weight						45		g
M_D	*mounting torque*				2		2.5	Nm
$d_{Spp/App}$	*creepage distance on surface | striking distance through air*		*terminal to terminal*	18.0	6.0			mm
$d_{Spb/Apb}$			*terminal to backside*	26.0	20.0			mm
V_{ISOL}	*isolation voltage*	t = 1 second	50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA		3600			V
		t = 1 minute			3000			V



Dimensions in mm (1 mm = 0.0394")



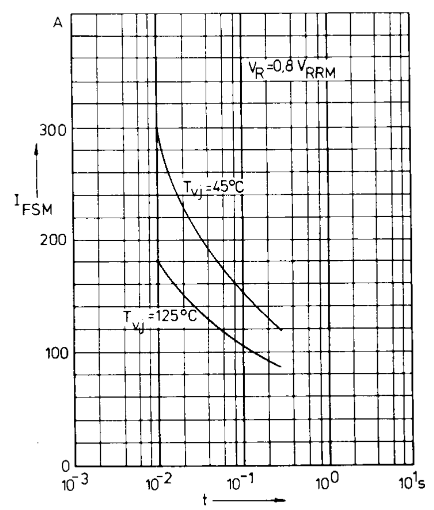


Fig. 1 Surge overload current per chip
I_{FSM}: Crest value, t: duration

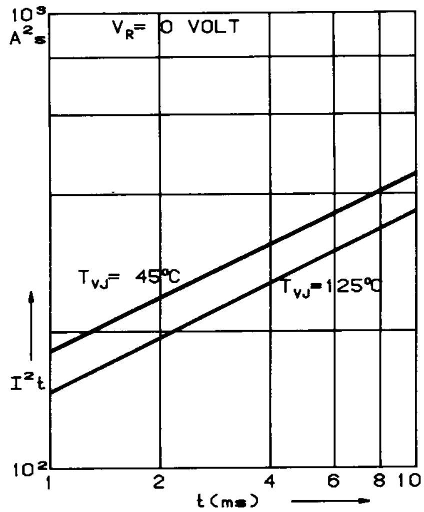


Fig. 2 I^2t versus time (1-10 ms) per chip

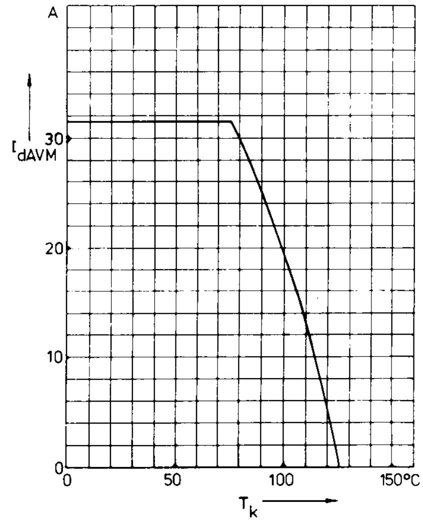


Fig. 3 Max. forward current at heatsink temperature

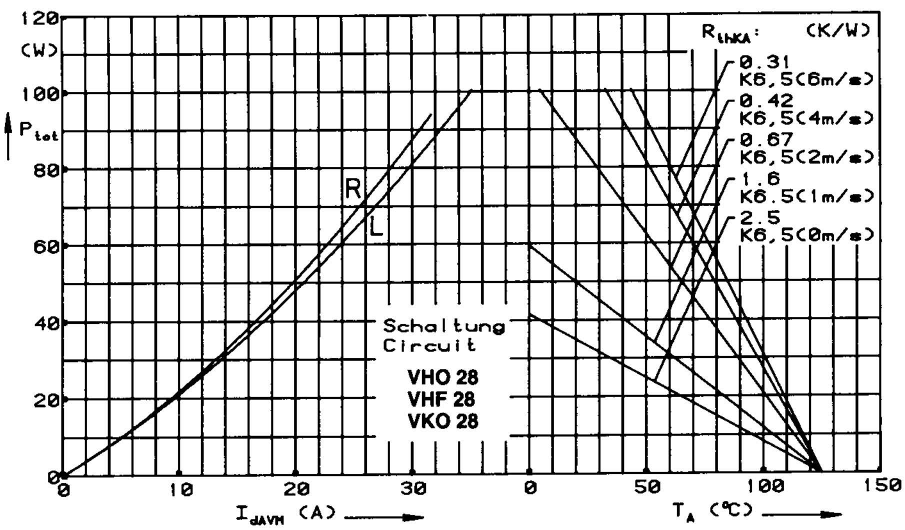


Fig. 4 Power dissipation versus direct output current and ambient temperature

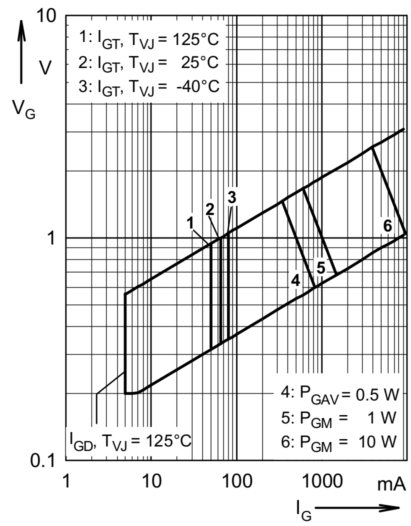
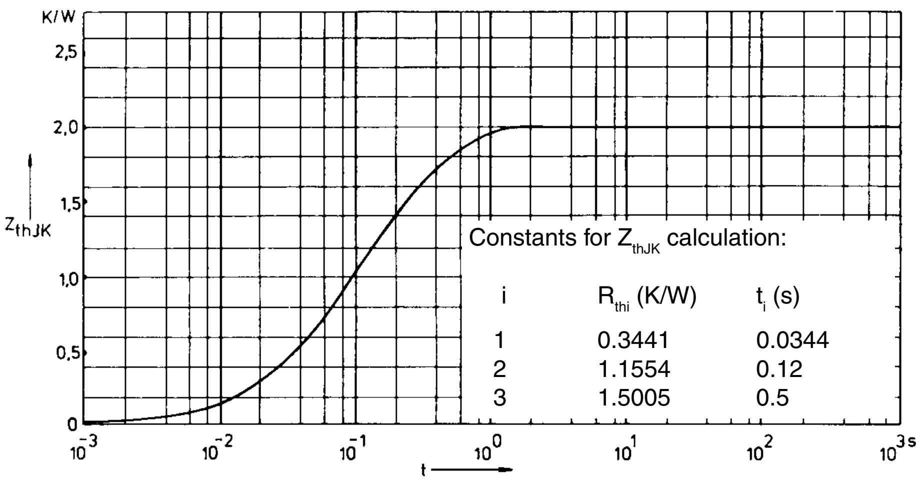


Fig. 5 Gate trigger range



Constants for Z_{thJK} calculation:

i	R_{thi} (K/W)	t_i (s)
1	0.3441	0.0344
2	1.1554	0.12
3	1.5005	0.5

Fig. 7 Transient thermal impedance junction to heatsink per chip

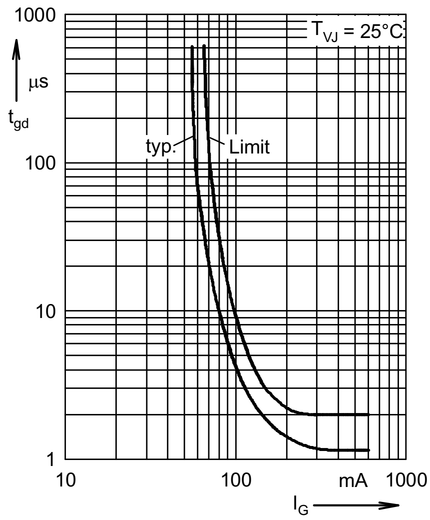


Fig. 7 Gate controlled delay time