CoreQSGMII v2.2 User Guide

Introduction

The CoreQSGMII provides a solution to combine four Serial Gigabit Media-Independent Interface (SGMII) lines into a single 5.0 Gbps link. The CoreQSGMII module takes each of the four Gigabit Media-Independent Interface (GMII) data stream and encodes it into 10-bit symbols per port to form a 40-bit interface to the transceiver. In the receive direction, the 40-bit symbols are decoded and converted into the receive G/MII signal set. The CoreQSGMII module is managed and monitored through the Management Data Input/Output (MDIO) interface.

The CoreQSGMII supports auto-negotiation for each of the four ports, which allows two link partners to exchange details of capabilities and hence determine the appropriate link operation characteristics, including the duplex mode and flow control direction.

Features

CoreQSGMII has the Following Key Features:

- Compliant with Cisco® Systems' Proprietary QSGMII Specification, Revision 1.2
- Four Independent 10/100/1000 Mbps Ports
- Implement SGMII Adaptation for 10/100/1000 Operation of Each Port
- Implements 8b/10b Encoder/Decoder and Physical Coding Sublayer (PCS) Transmit Function for Each Port in Accordance with IEEE® Standard 802.3 Clause 36, Modified to Support QSGMII
- K28.5 Swapper on Port 0 in the Transmit Path as per the QSGMII Specification
- Comma Alignment and K28.1 Swapper on Port 0 in the Receive Path as per the QSGMII Specification
- Supports Auto-Negotiation Functionality per Port
- Supports Management Interface for Register Configuration Through MDIO Interface
- The SerDes Interface on the QSGMII IP is Configured for 40-bit, Single Lane Operating at 5.0 Gbps Speed with Fabric Interface Running at 125 MHz

Supported Families

This version of CoreQSGMII supports the following families:

- PolarFire® SoC
- PolarFire
- RT PolarFire

Device Utilization and Performance

CoreQSGMII has been implemented in the PolarFire device using speed grade-1. The following table lists the device utilization and performance data. The data listed in this table is indicative only. The overall device utilization and performance of the core is system dependent.

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Table 1. Device Utilization and Performance

Device Details		Resources			Performance (MHz)
Family	**Device**	**LUTs**	**DFF**	**Logic Elements**	
PolarFire® SoC	MPFS250T	9934	4498	11168	MDC – 100 MHz TBI_TX_CLK – 150 MHz TXCLK_Px – 150 MHz TBI_RX_CLK – 150 MHz RXCLK_Px – 150 MHz
PolarFire	MPF300T	9939	4498	11351	MDC – 100 MHz TBI_TX_CLK – 150 MHz TXCLK_Px – 150 MHz TBI_RX_CLK – 150 MHz RXCLK_Px – 150 MHz
RT PolarFire	RTPF500T	9753	4498	10921	MDC – 90 MHz TBI_TX_CLK – 150 MHz TXCLK_Px – 150 MHz TBI_RX_CLK – 150 MHz RXCLK_Px – 150 MHz

Important: The data in this table is achieved using typical synthesis and layout settings. Frequency is set to 2.5 MHz for MDC clock and 125 MHz for other clocks and speed grade is -1.

Table of Contents

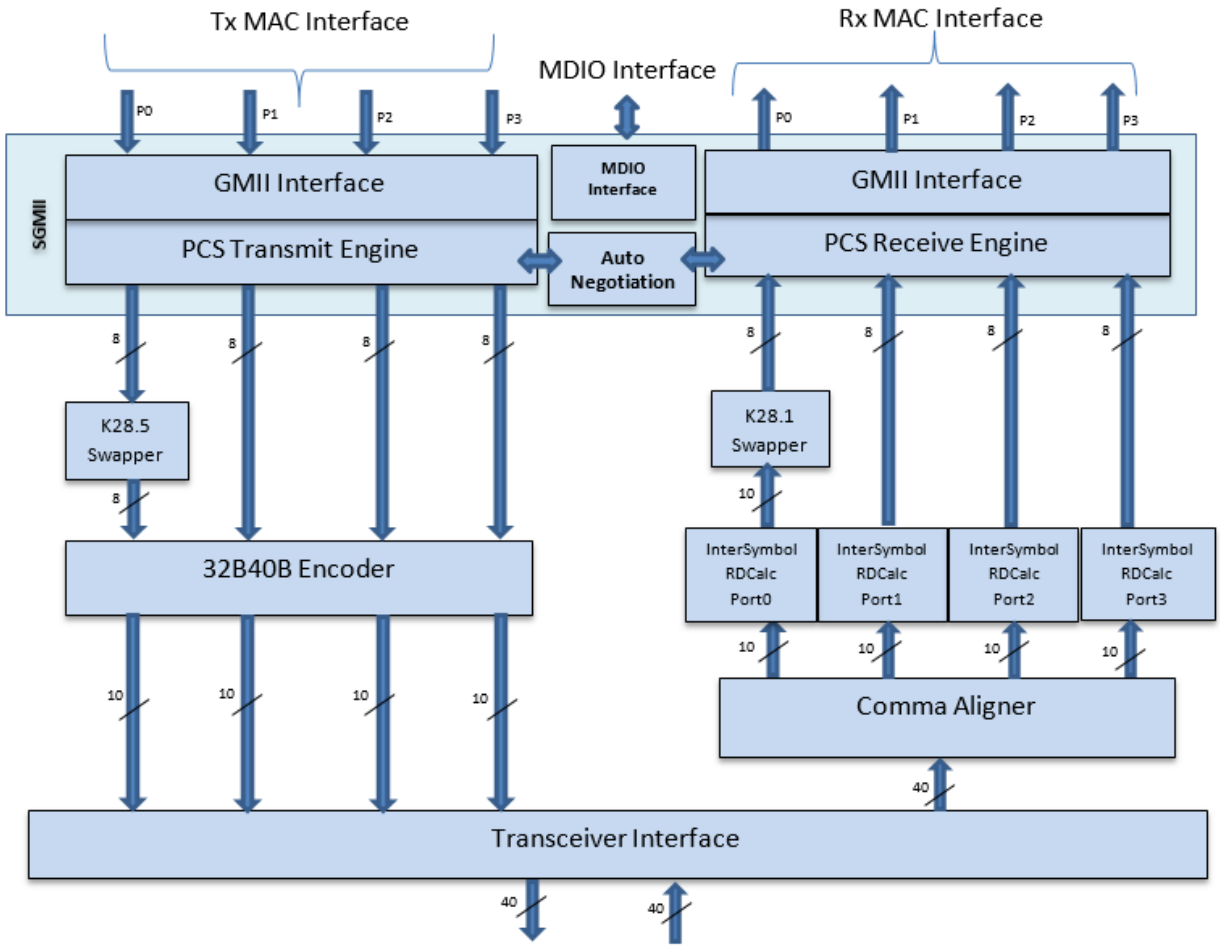
1. Functional Description

This section describes the functional description of the CoreQSGMII.

1.1 CoreQSGMII Interfaces

This section describes the various interfaces connected with CoreQSGMII IP core. The following figure shows the CoreQSGMII block diagram.

Figure 1-1. CoreQSGMII Block Diagram



The IP provides four independent ports of 1000/100/10 Mbps for the ethernet communication between the Physical Layer (PHY) and the Media Access Control (MAC) over a single link of 5.0 Gbps using the transceiver configured in 40-bit mode.

The IP contains PCS functionality logic modified in compliance with Cisco's QSGMII Specification, Revision 1.2.

CoreQSGMII consists of the following interfaces:

- MAC-side (G/MII) interface
- Management interface
- Transceiver interface

1.1.1 MAC-Side (G/MII) Interface

The IP connects to four MACs through four independent IEEE 802.3 G/MII interface.

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G/MII is an interface between the MAC device and the PHY. It defines speeds up to 1000 Mbps, implemented using an 8-bit data interface clocked at 125 MHz, and is backwards compatible with the Media-Independent Interface (MII) specification. It can also operates at speed of 10 or 100 Mbps as per the MII specification.

Data on the interface is framed using the IEEE Ethernet standard. It consists of the following:

- Preamble
- Start frame delimiter
- Ethernet headers
- Protocol specific data
- Cyclic Redundancy Check (CRC)

In case of G/MII transmission, there are two clocks, depending on whether the PHY is operating at 1000 Mbps or 10/100 Mbps speeds. TBI_TX_CLK signal is supplied to the PHY for 1000 Mbps speed, and the transmit data and the control signals are synchronized to this. Otherwise, for 10/100 Mbps, the TXCLK_Px (where x represent the range of 0 to 3) signal, supplied by the PHY, is used for synchronizing those signals. This operates at either 25 MHz for 100 Mbps or 2.5 MHz for 10 Mbps connections. The RXCLK_Px (where x represent the range of 0 to 3) is 2.5/25/125 MHz for 10/100/1000 respectively, is supplied from PHY/Transceiver.

It contains the logic for the PCS transmit path data conversion (repeating each data byte 10/100 times for 10/100 Mbps IEEE 802.3 G/MII and synchronization with the TBI_TX_CLK signal. For all the ports, the PCS transmit logic transmits only /I1/ ordered sets instead of /I2/ as per the QSGMII specification.

It also performs the receive path data conversion from the ten-bit interface to the G/MII data on the RXCLK_Px (where x represent the range of 0 to 3) domain. It stores the data every 10/100 clocks for 10/100 Mbps respectively.

1.1.2 Management Interface

The CoreQSGMII registers are accessed through the MDIO interface. A single MDIO interface is provided for the four independent ports. The MDIO controller in the MAC reads and writes the control and status registers of the CoreQSGMII. The MDIO interface is compliant with the IEEE 802.3z, Clause 45.

1.1.3 Transceiver Interface

The 10-bit data from each of the SGMII instances is transferred to the transceiver interface forming 40-bit data. In the receive path, the 40-bit data from the transceiver interface is transferred to comma alignment and K28.1 detection logic.

The transceiver is configured to operate on single lane, 40-bit mode with 125 MHz speed, at the fabric interface to give 5.0 Gbps link rate.

1.2 Functional Blocks

CoreQSGMII contains the following blocks:

- Four SGMII blocks
- Tx/Rx swapper
- 32B40B encoder
- Comma aligner
- Receive intersymbol Running Disparity (RD) swapper

1.2.1 SGMII Block

Each SGMII block has the G/MII interface to connect the MAC with the PHY. It performs the transmit exchange functionality, the receive exchange functionality, the auto-negotiation functionality, and the management functionality using the MDIO interface.

1.2.1.1 TEX (Transmit Exchange functionality)

This module performs clause 36 transmit related functionality of 802.3z.

The PCS transmit functionality is modified as per QSGMII specification Revision 1.2 (Figure 1-1) on port 0 by detaching the PCS transmit functionality from the 8b/10b encoder. This is done by incorporating a “K28.5” swapper function that modifies the IDLE/I/ and Configures /C/ ordered sets by replacing every occurrence of /K28.5/ with /

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K28.1/. The swapper function operates on the GMII octets before the 8b/10b encoding. It is important to note that the transmitter generates only /I1/ ordered set as per the QSGMII specification.

TEX operation is governed by Auto-Negotiation, which provides CFG/IDL/DAT information:

- In Configuration (CFG) mode, TEX sends /C/ ordered sets with data from Auto-Negotiation (ANX).
- In Idle (IDL) mode, TEX sends /I/ order sets.
- In Data (DAT) mode, TEX send 8b/10b encoded packets.

1.2.1.2 REX (Receive Exchange functionality)

Performs clause 36, receive related functionality of 802.3z.

Performs comma alignment and passes aligned two-code-group. It determines the alignment by searching for the comma character K28.1 on the received 40-bit data, as the port 0 data can be on any of the four 10-bit lanes. After a match is found, the K28.1 swapper logic swaps the K28.1 code-group received on the port 0 with K28.5 code-group as per the QSGMII specification.

The code-groups from the PCS are decoded for 10b/8b and inspected by the receive logic.

The received 10-bit code-groups from the Ten-Bit interface performs the exact reverse procedure as that of the transmit function by undoing the swapping function introduced in the transmit path. That is, a “K28.1” swapper function replaces the received /K28.1/ with /K28.5/ for every occurrence on the port 0. The swapper logic works post the 10b/8b decoding on the 8-bit GMII octets. However, the carrier detect function operates on the 10B code-group to detect /K28.1/ for port 0.

In Auto-Negotiation mode as indicated by the transmit variable, the PCS module looks for configuration ordered sets and passes the receive configuration register contents to the ANX module.

After Auto-Negotiation completes, removes the encapsulation codes and passes the received packet.

1.2.2 K28.5 Swapper

The port 0 transmit side incorporates a K28.5 swapper logic, which modifies each occurrence of K28.5 with K28.1. This is done in order to determine the port number based data alignment. The transmit data appears on the QSGMII link in the order of port 0 first, then port 1, then port 2 and, then port 3. This is repeated with the port 0 data again on the link and so on.

Important: The ports other than port 0 does not perform K28.5 swapping.

The following table lists the K28.5 Swapper definition for port 0.

Table 1-1. Port 0 K28.5 Swapper Definition

Code	Ordered_Set	Number of Code Groups	Port 0 Pre-Swapper Encoding	Port 0 Post-Swapper Encoding
/C/	Configuration	—	Alternating /C1/ and /C2/	Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg	/K28.1/D21.5/Config_Reg
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg	/K28.1/D2.2/Config_Reg
/I/	IDLE	—	Correcting /I1/	Correcting /I1/
/I1/	IDLE 1	2	/K28.5/D5.6/	/K28.1/D5.6/

1.2.3 32B40B Encoder

The 8-bit data from each of the SGMII blocks is formed into a 32-bit data. This module performs the 32B40B PCS encoding. The running disparity between the transmitted 10-bit symbols from each SGMII block is handled in this block.

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1.2.4 Comma Aligner Block

The Comma Aligner block performs alignment on two consecutive 40-bit data received from the transceiver interface. It also performs barrel shifting on the incoming data and searches for the K28.1 comma code. The detection of comma code determines the 10-bit symbol alignment with respect to port 0 data.

It provides the 40-bit aligned data with each 10-bit data going to each of the four InterSymbol RD swapper modules.

1.2.5 InterSymbol RD Swapper

This block calculates the running disparity between the successive 10-bit aligned data in the receive path. The output is 10-bit data with the running disparity maintained between successive 10-bit symbols.

1.2.6 K28.1 Swapper Logic

The K28.1 swapper module receives 10-bit code group from the InterSymbol RD swapper module. It undoes the modification done in the transmit path by replacing every occurrence of K28.1 with K28.5 symbol code. Every occurrence of K28.1 in IDLE /I/ and configuration /C/ ordered sets is replaced with K28.5.

The following table lists the K28.1 Swapper definition for Port 0.

Table 1-2. Port0 K28.1 Swapper Definition

Code	Ordered_Set	Number of Code Groups	Port 0 “Pre-Swapper” Encoding	Port 0 “Post-Swapper” Encoding
/C/	Configuration	—	Alternating /C1/ and /C2/	Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.1/D21.5/Config_Reg	/K28.5/D21.5/Config_Reg
/C2/	Configuration 2	4	/K28.1/D2.2/Config_Reg	/K28.5/D2.2/Config_Reg
/I/	IDLE	—	Correcting /I1/	Correcting /I1/
/I1/	IDLE 1	2	/K28.1/D5.6/	/K28.5/D5.6/

2. Interface

This section describes the parameters in the CoreQSGMII GUI configurator and I/O signals.

2.1 Configuration Parameters

CoreQSGMII has parameters (Verilog) for configuring the RTL code. The following table lists the CoreQSGMII parameters and their description. All parameters are integer types.

Table 2-1. CoreQSGMII Parameters and Generics Descriptions

Parameter	Valid Values	Default	Description
MDIO_PHYID_PORT0	0–31	0	MDIO PHY address for Port 0
MDIO_PHYID_PORT1	0–31	1	MDIO PHY address for Port 1
MDIO_PHYID_PORT2	0–31	2	MDIO PHY address for Port 2
MDIO_PHYID_PORT3	0–31	3	MDIO PHY address for Port 3

2.2 I/O Signals

The following table lists the clock port signals for the CoreQSGMII IP.

Table 2-2. CoreQSGMII Clock Signals

Port Name	Direction	Width	Description
CoreQSGMII Clocks (x represents the range of 0 to 3)			
TBI_TX_CLK	1	Input	125 MHz Ten Bit Interface (TBI) transmit clock from transceiver.
TXCLK_Px	1	Input	2.5/25/125 MHz transmit clock generated from transceiver TX clock according to 10/100/1000 Mbps support for port x.
TBI_RX_CLK	1	Input	125 MHz TBI receive clock from transceiver.
RXCLK_Px	1	Input	2.5/25/125 MHz receive clock generated from transceiver RX clock according to 10/100/1000 Mbps support for port x.
MDC	1	Input	Management data clock, recommended to drive 2.5 MHz.

The following table describes the input/output ports of the CoreQSGMII IP.

Table 2-3. CoreQSGMII Input/Output Ports

Port Name	Direction	Clock Domain	Width	Description
Reset Port				
RESET	Input	Asynchronous	1	Asynchronous active high reset. The reset is internally synchronized with the respective clock domains.
G/MII Interface (x represents the range of 0 to 3)				
TXD_x	Input	TXCLK_Px	8	G/MII transmit data
TXEN_x	Input	TXCLK_Px	1	G/MII transmit enable
TXER_x	Input	TXCLK_Px	1	G/MII transmit error

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Port Name	**Direction**	**Clock Domain**	**Width**	**Description**
RXD_x	Output	RXCLK_Px	8	G/MII receive data
RXDV_x	Output	RXCLK_Px	1	G/MII receive data valid
RXER_x	Output	RXCLK_Px	1	G/MII receive error
COL_x	Output	RXCLK_Px	1	MII collision
CRS_x	Output	RXCLK_Px	1	MII carrier sense
Ten-Bit Interface (x represents the range of 0 to 3)				
TCG_x	Output	TBI_TX_CLK	1	TBI Transmit Code Group (TCG) for port x
RCG_x	Input	TBI_RX_CLK	1	TBI Receive Code Group (RCG) for port x
Other Ten-Bit Interface Signals				
TBI_RX_READY	Input	Asynchronous	1	RCG ready, recommended to connect with transceiver.
TBI_RX_VALID	Input	Asynchronous	1	RCG valid, recommended to connect with transceiver.
MDIO Interface				
MDO	Input	MDC	1	Management data output
MDOEN	Input	MDC	1	Management data output enable
MDI_EXT	Input	MDC	1	Management data input from external PCS/PHY
MDI	Output	MDC	1	MII Management data Input

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3. Register Map and Descriptions

The following table lists the registers that are accessed through the MDIO interface, Clause 22 of the IEEE 802.3 specification. The PHY address for the MDIO registers is configurable. The CoreQSGMII contains the management registers specified in IEEE 802.3, Clause 37. The register set is read/write through MDIO interface.

Prefix 0x represents hex value and 0b represents binary value in the following register summary and register description tables.

Type columns in the register's tables indicate the access type of the registers. The following table describes the access type.

Table 3-1. Access Type Descriptions

Access Type	Description
RW	Read or Write
RO	Read only
ROC	Read on clear

Some register's bits may support different access type. All the supported access types are shown under Type column for those registers. All the reserved bits are always read as zero and reserved bits must always be written to zero if accessed unless otherwise specified.

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3.1 Register Summary

The following table lists the register summary of CoreQSGMII.

Table 3-2. CoreQSGMII Register Summary

Address	Register Name	Type	Width	Reset Value	Description
0x00	CTRL	R/W	16	0x0000	Control Register
0x01	STS	RO	16	0x0149	Status Register
0x04	AN_ADV	R/W	16	0x0000	AN Advertisement Register
0x05	AN_LNKPGABL	RO	16	0x0000	AN Link Partner Base Page Ability Register
0x06	AN_EXPNSN	RO ROC	16	0x0004	AN Expansion Register
0x07	AN_NPTX	R/W RO	16	0x0000	AN Next Page Transmit Register
0x08	AN_LNKABLNXP	RO	16	0x0000	AN Link Partner Ability Next Page Register
0x0F	EXT_STS	RO	16	0xA000	Extended Status Register
0x10	JTR_DIGN	R/W	16	0x0000	Jitter Diagnostics Register
0x11	TBI_CTRL	R/W	16	0x0008	TBI Control Register

3.2 CoreQSGMII Register Descriptions

This section describes the register's functionalities.

3.2.1 Control Register

This register provides controls bits for the PHY and auto-negotiation process. The following table lists the control register descriptions.

Table 3-3. Control Register

Address	Register Name	Type	Width	Reset Value	Description
0x00	CTRL	R/W	16	0x0000	Control Register

The following table lists the control register bit definitions.

Table 3-4. Control Register Bit Definitions

Bits	Name	Type	Reset Value	Description
15	PHY_RST	R/W	0	PHY Reset Setting this bit causes the TEX, REX, and ANX sub-modules in the CoreQSGMII core to be reset. This bit is self-cleared by the IP.
14	LPBK_EN	R/W	0	Loopback Enbale Setting this bit causes the transmit output of the CoreQSGMII to be connected to the receive inputs. Clearing this bit results in normal operation.
13	Reserved			

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Bits	**Name**	**Type**	**Reset Value**	**Description**
12	AN_EN	R/W	0	Auto-Negotiation Enable Setting this bit enables the auto-negotiation process.
11:10	Reserved			
9	AN_RSTRT	R/W	0	Restart Auto-Negotiation Setting this bit causes the auto negotiation process to restart. This action is only available when Auto-Negotiation has been enabled. This bit is self-cleared by the IP.
8:0	Reserved			

3.2.2 Status Register

This register provides PHY status, auto-negotiation process status and link status. The following table lists the status register descriptions.

Table 3-5. Status Register

Address	Register Name	Type	Width	Reset Value	Description
0x01	STS	RO	16	0x0149	Status Register

The following table lists the status register bit definitions.

Table 3-6. Status Register Bit Definitions

Bits	Name	Type	Reset Value	Description
15:9	Reserved			
8	EXTND_STS	RO	1	Extended Status This bit indicates that PHY status information is also contained in extended status register.
7	Reserved			
6	PRMBLE_SUPPRES_EN	RO	1	Preamble Suppression Enable This bit indicates whether the PHY is capable of handling MII management frames without the 32-bit preamble field. Returns 1 to indicate support for suppressing preamble MII management frames.
5	AN_CMPL	RO	0	Auto-Negotiation Complete When 1, this bit indicates that the auto-negotiation process has completed. This bit returns ‘0’ when either the auto-negotiation process is in progress, or the auto-negotiation function is disabled.
4	RMT_FAULT	RO	0	Remote Fault Assertion of this bit indicates that remote fault condition has been detected between the CoreQSGMII and the PHY.
3	AN_ABL	RO	1	Auto Negotiation Ability Assertion of this bit indicates that the CoreQSGMII can perform auto-negotiation.

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Bits	**Name**	**Type**	**Reset Value**	**Description**
2	LINK_STS	RO	0	Link Status Assertion of this bit indicates that a valid link has been established between the CoreQSGMII and the PHY. De-assertion of this bit indicates that no valid link has been established.
1	Reserved			
0	EXTND_CAP	RO	1	Extended Capability Assertion of this bit indicates that the CoreQSGMII contains the extended set of registers.

3.2.3 AN Advertisement Register

This register provides configuration of local device ability during auto-negotiation operation with PHY. The following table lists the auto-negotiation advertisement register descriptions.

Table 3-7. AN Advertisement Register

Address	Register Name	Type	Width	Reset Value	Description
0x04	AN_ADV	R/W	16	0x0000	AN Advertisement Register

The following table lists the auto-negotiation advertisement register bit definitions.

Table 3-8. AN Advertisement Register Bit Definitions

Bits	Name	Type	Reset Value	Description
AN Advertisement - SGMII				
15:13	Reserved			
12	FDUPLX	R/W	0	Full-Duplex The assertion of this bit indicates that the link is transferring data in full-duplex mode.
11:10	LSPEED	R/W	0b00	Link Speed Link speed set by the application for the auto-negotiation. For link speed encoding, see the following table speed. **Table 3-9. Link Speed Descriptions** **Bits [11:10] / Speed** 00 / 10 Mbps 01 / 100 Mbps 10 / 1000 Mbps 11 / Reserved
9:0	RSVD	R/W	0b0000000000	Reserved As per the SGMII specification this register must be written to 0x00000001.
AN Advertisement - 1000BASE-X				

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Bits	Name	Type	Reset Value	Description
15	NXTPG	R/W	0	Next Page The local device asserts this bit to either request Next Page transmission or advertise next page exchange capability. This bit is set when the local has no Next Pages but wishes to allow reception of Next Pages. If the local device has no Next Pages, and the link partner wishes to send Next Pages, the local device must send null message codes and have the **MESSAGE PAGE** set to 0b000_0000_0001.This bit must be cleared where the local device wishes not to engage in Next Page exchange.
14	Reserved			
13:12	RMTFLT_ENC	R/W	0b00	Remote Fault Encodes the local device's remote fault condition. A fault may be indicated by setting a nonzero Remote Fault encoding and re-negotiating. For remote fault encoding, see the following table. **Table 3-10. Remote Fault Encoding** RF1(4,12) / RF2(4,13) / Description 0 / 0 / No error, link ok 0 / 1 / Offline 1 / 0 / Link failure 1 / 1 / Auto negotiation error
11:9	Reserved			
8:7	PAUS_ABL	R/W	0b00	Pause Ability Encodes the local device's PAUSE capability. For pause encoding, see the following table. **Table 3-11. Pause Encoding** Pause(4,7) ASM_DIR / (4,8) / Capability 0 / 0 / No pause 0 / 1 / Asymmetric pause toward link partner 1 / 0 / Symmetric pause 1 / 1 / Asymmetric pause toward local device
6	HDUPLX	R/W	0	Half-Duplex Setting this bit to 1 indicates local device is capable of half-duplex operation.
5	FDUPLX	R/W	0	Full-Duplex Setting this bit to 1 indicates local device is capable of half-duplex operation.
4:0	Reserved			

3.2.4 AN Link Partner Base Page Ability Register

This register provides details of PHY ability received during auto negotiation process. The following table lists the auto-negotiation link partner base page ability register descriptions.

Table 3-12. AN Link Partner Base Page Ability Register

Address	Register Name	Type	Width	Reset Value	Description
0x05	AN_LNKPGABL	RO	16	0x0000	AN Link Partner Base Page Ability Register

The following table lists the auto-negotiation link partner base page ability register definitions.

Table 3-13. AN Link Partner Base Page Ability Register Bit Definitions

Bits	Name	Type	Reset Value	Description
AN Link Partner Base Page Ability - SGMII				
15	LNKUP	RO	0	Link Up Status Assertion of this bit indicates that the link is up.
14:13	Reserved			
12	LP_ FDUPLX	RO	0	Link Partner Full Duplex Ability Assertion of this bit indicates that link partner supports full duplex data transfer.
11:10	LP_LSPEED	RO	0b00	Link Partner Link Speed Ability These two bits indicates the link partner's link speed ability. For link partner speed encoding, see the following table. **Table 3-14. Link Parter Speed** Bits[11:10] / Speed 00 / 10 Mbps 01 / 100 Mbps 10 / 1000 Mbps 11 / Reserved
9:0	Reserved			
AN Link Partner Base Page Ability - 1000BASE-X				
15	LP_NXTPG	RO	0	Link Partner Next Page The link partner asserts this bit either to request Next Page transmission or to indicate the capability to receive Next Pages. De-assertion of this bit indicates that the link partner has no subsequent Next Pages or is not capable of receiving Next Pages.
14	Reserved			

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Bits	Name	Type	Reset Value	Description
13:12	LP_RMTFLT_ENC	RO	0b00	Link Partner Remote Fault These two bits indicates the link partner's remote fault condition. For link partner remote fault encoding, see the following table. **Table 3-15. Remote Fault Encoding** RF1(4,12) / RF2(4,13) / Description: 0 / 0 / No error, link ok 0 / 1 / Offline 1 / 0 / Link failure 1 / 1 / Auto negotiation error
11:9	Reserved			
8:7	LP_PAUS_ABL	RO	0b00	Link Partner Pause Ability These two bits indicates the link partner's pause capability. For pause encoding, see the following table. **Table 3-16. Pause Encoding** Pause(4,7) / ASM_DIR(4,8) / Capability: 0 / 0 / No pause 0 / 1 / Asymmetric pause toward link partner 1 / 0 / Symmetric pause 1 / 1 / Asymmetric pause toward local device
6	LP_HDUPLX	RO	0	Link Partner Half-Duplex Ability Assertion of this bit indicates that link partner supports half-duplex mode and de-assertion of this bit indicates that link partner does not support half-duplex mode.
5	LP_FDUPLX	RO	0	Link Partner Full-Duplex Ability Assertion of this bit indicates that link partner supports full-duplex mode and de-assertion of this bit indicates that link partner does not support full-duplex mode.
4:0	Reserved			

3.2.5 AN Expansion Register

This register provides details of Next Page status. The following table lists the auto-negotiation expansion register descriptions.

Table 3-17. AN Expansion Register

Address	Register Name	Type	Width	Reset Value	Description
0x06	AN_EXPNSN	RO ROC	16	0x0004	AN Expansion Register

The following table lists the auto-negotiation expansion register bit definitions.

Table 3-18. AN Expansion Register Bit Definitions

Bits	Name	Type	Reset Value	Description
15:3	Reserved			
2	NP_ABL	RO	1	Next Page Ability Assertion of this bit indicates that local device supports the next page function.
1	PG_RCVD	ROC	0	Page Received Assertion of this bit indicates that a new page has been received and stored in the applicable AN Link Partner Ability or AN Next Page. Reading AN Expansion Register clears this bit.
0	Reserved			

3.2.6 AN Next Page Transmit Register

Use of this register is user dependent. User can define the functionality of bits of this register as per the system requirement. The following table lists the auto-negotiation next page transmit register descriptions.

Table 3-19. AN Next Page Transmit Register

Address	Register Name	Type	Width	Reset Value	Description
0x07	AN_NPTX	R/W, RO	16	0x0000	AN Next Page Transmit Register

The following table lists the auto-negotiation next page register bit definitions.

Table 3-20. AN Next Page Transmit Register Bit Definitions

Bits	Name	Type	Reset Value	Description
AN Next Page Transmit - SGMII				
15:0	USR_REG	R/W	0x0000	User Defined Register This is user defined register and user can configure as per the system requirement.
AN Next Page Transmit - 1000BASE-X				
15	NXT_PG	R/W	0	Next Page Status Assert this bit to indicate additional next pages to follow. To indicate last page, this bit must be cleared.
14	Reserved			
13	MSG_PG	R/W	0	Message Page Assert bit to indicate Message Page. Clear bit to indicate Unformatted Page.
12	ACK2	R/W	0	Acknowledge 2 Used by Next Page function to indicate device has ability to comply with the message. Assert if local device complies with message. Clear bit if the local device cannot comply with the message.

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.....continued				
Bits	**Name**	**Type**	**Reset Value**	**Description**
11	TGL	RO	0	Toggle Used to ensure synchronization with the link partner during next page exchange. This bit always takes the opposite value of the toggle bit of the previously exchanged link code word. The initial value in the first next page transmitted is the inverse of bit 0b11 in the base link code word.
10:0	MSG_CODE	R/W	0b00000000000	Message/Unformatted Code Field Message pages are formatted pages that carry a predefined message code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

3.2.7 AN Link Partner Ability Next Page Register

Use of this register is user dependent. User can use the functionality of bits of this register as per the system requirement. The following table lists the auto-negotiation link partner ability next page transmit register descriptions.

Table 3-21. AN Link Partner Ability Next Page Register

Address	Register Name	Type	Width	Reset Value	Description
0x08	AN_LNKABLNXP	RO	16	0x0000	AN Link Partner Ability Next Page Register

The following table lists the auto-negotiation link partner ability next page register bit definitions.

Table 3-22. AN Link Partner Ability Next Page Register Bit Definitions

Bits	Name	Type	Reset Value	Description
AN Link Partner Ability Next Page Register - SGMII				
15:0	USR_REG	RO	0x0000	User Defined Register This is user defined register and user can use as per the system requirement.
AN Link Partner Ability Next Page Register - 1000BASE-X				
15	NXT_PG	RO	0	Next Page Status The Link Partner asserts this bit to indicate additional Next Pages to follow. When 0 - it indicates last Next Page from link partner.
14	Reserved			
13	MSG_PG	RO	0	Message Page The link partner asserts this bit to indicate Message Page and de-asserts this bit to indicate Unformatted Page.
12	ACK2	RO	0	Acknowledge 2 Indicates link partner's ability to comply with the message. Assertion of this bit indicates that link partner complies with message. De-assertion of this bit indicates that link partner cannot comply with the message.

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.....continued				
Bits	**Name**	**Type**	**Reset Value**	**Description**
11	TGL	RO	0	Toggle Used to ensure synchronization with the link partner during Next Page exchange. This bit always takes the opposite value of the toggle bit of the previously exchanged link code word. The initial value in the first Next Page transmitted is the inverse of bit 0b11 in the base link code word.
10:0	MSG_CODE	RO	0b00000000000	Message/Unformatted Code Field Message pages are formatted pages that carry a predefined message code, which is enumerated in IEEE 802.3u/Annex 28C. Unformatted Code Fields take on an arbitrary value.

3.2.8 Extended Status Register

This register provides capability status of the PHY. The following table lists the extended status register descriptions.

Table 3-23. Extended Status Register

Address	Register Name	Type	Width	Reset Value	Description
0x0F	EXT_STS	RO	16	0xA000	Extended Status Register

The following table lists the extended status register bit definitions.

Bits	Name	Type	Reset Value	Description
15	FDUPLX_BASEX	RO	1	1000BASE-X Full-Duplex Assertion of this bit indicates PHY can operate in 1000BASE-X full-duplex mode. De-assertion of this bit indicates PHY cannot operate in 1000BASE-X full-duplex mode.
14	HDUPLX_BASEX	RO	0	1000BASE-X Half Duplex Assertion of this bit indicates PHY can operate in 1000BASE-X half-duplex mode. De-assertion of this bit indicates PHY cannot operate in 1000BASE-X half-duplex mode.
13	FDUPLX_BASET	RO	1	1000BASE-T Full Duplex Assertion of this bit indicates PHY can operate in 1000BASE-T full-duplex mode. De-assertion of this bit indicates PHY cannot operate in 1000BASE-T full-duplex mode.
12	HDUPLX_BASET	RO	0	1000BASE-T Half Duplex Assertion of this bit indicates PHY can operate in 1000BASE-X half-duplex mode. De-assertion of this bit indicates PHY cannot operate in 1000BASE-X half-duplex mode.
11:0	Reserved			

3.2.9 Jitter Diagnostics Register

This register controls the diagnostic mode and jitter pattern. The following table lists the jitter diagnostics register descriptions.

Table 3-24. Jitter Diagnostics Register

Address	Register Name	Type	Width	Reset Value	Description
0x10	JTR_DIGN	R/W	16	0x0000	Jitter Diagnostics Register

The following table lists the jitter diagnostics register bit definitions.

Table 3-25. Jitter Diagnostics Register Bit Definitions

Bits	Name	Type	Reset Value	Description
15	JTR_DIGN_EN	R/W	0	Jitter Diagnostic Enable Set this bit to enable the CoreQSGMII to transmit the jitter test patterns defined in IEEE 802.3z, 36A. Clear this bit to enable normal transmit-operation.
14:12	JTR_PAT_SEL	R/W	0b000	Jitter Pattern Select Selects the jitter pattern to be transmitted in diagnostics mode. For jitter pattern select encoding, see the following table.
11:10	Reserved			
9:0	CUST_JIT_PAT	R/W	0	Custom Jitter Pattern Used in conjunction with Jitter Pattern Select and Jitter Diagnostic Enable. Set this field to the desired custom pattern.

Table 3-26. Table Jitter Pattern Select Encoding

Bits[14:12]	Jitter Pattern Select
0b000	User defined custom pattern
0b001	Annex 36A defined high frequency 10101010101010101010…
0b010	Annex 36A defined mixed frequency 11111010110000010100…
0b011	Custom defined low frequency 11111000001111100000**…**
0b100	Random jitter pattern
0b101	Annex 36A defined low frequency 11111000001111100000…
0b110	Reserved
0b111	Reserved

3.2.10 TBI Control Register

This register controls the reset, disparity calculation, and link timer value. The following table lists the TBI control register descriptions.

Table 3-27. TBI Control Register

Address	Register Name	Type	Width	Reset Value	Description
0x10	TBI_CTRL	R/W	16	0x0008	TBI Control Register

The following table lists the TBI control register bit definitions.

Table 3-28. TBI Control Register Bit Definitions

Bits	Name	Type	Reset Value	Description
15	SOFT_RST	R/W	0	Soft Reset This bit resets the functional modules in the CoreQSGMII. Clear it for normal operation.
14	SHRT_LNK_TMR	R/W	0	Shortcut Link Timer Set this bit 1 to reduce the value of Go Link Timer and Sync. Status Fail Timer to 64 clock pulse. This reduces the simulation time needed to time the 1.6 ms link timer. Clear it for normal operation. In normal operation, the value of Go Link Timer is 200000 clock pulses and the value of the Sync. Status Fail Timer is 1250000 clock pulses.
13	RX_DPRTY_DIS	R/W	0	Disable Receive Running Disparity Set this bit to disable the running disparity calculation and checking in the receive direction. This bit must be 0 for correct CoreQSGMII operation.
12	TX_DPRTY_DIS	R/W	0	Disable Transmit Running Disparity Set this bit to disable the running disparity calculation and checking in the transmit direction. This bit must be 0 for correct CoreQSGMII operation.
11	GO_LNK_TMR_CTRL	R/W	0	Go Link Timer Value Control When 0 the Go Link Timer Value = 1.6 milli second (ms) When set to 1 the Go Link Timer Value = 10 ms
10:9	Reserved			
8	AN_SENSE	R/W	0	Auto Negotiation Sense Set this bit to allow the auto-negotiation function to sense either a MAC in auto-negotiation bypass mode or an older MAC without auto-negotiation capability. When sensed, Auto Negotiation Complete becomes true; however, Page Received is low, indicating no page is exchanged. Management can then act accordingly. Clear this bit when IEEE 802.3z Clause 37 behaviour is desired, which results in the link not coming up.
7:4	Reserved			
3:2	SPEED	R/W	0b10	Link Speed These two bits indicates the local device's link speed ability. For local device's link speed encoding refer the following table. **Table 3-29. Local Device Speed Encoding** Bits [3:2] / Speed 00 / 10 Mbps 01 / 100 Mbps 10 / 1000 Mbps 11 / Reserved
1:0	Reserved			

4. Timing Diagrams

This section describes various timing diagrams.

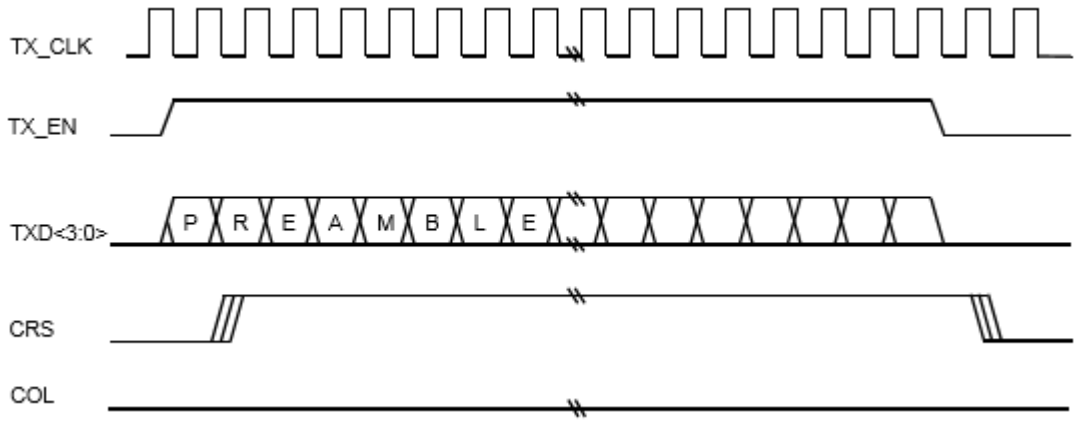
4.1 G/MII Timing Diagrams

This section describes the various G/MII timing behaviour.

4.1.1 Transmission with no Collision

This section describes the transmission with no collision timing behaviour. The following figure shows the transmission with no collision timing waveform.

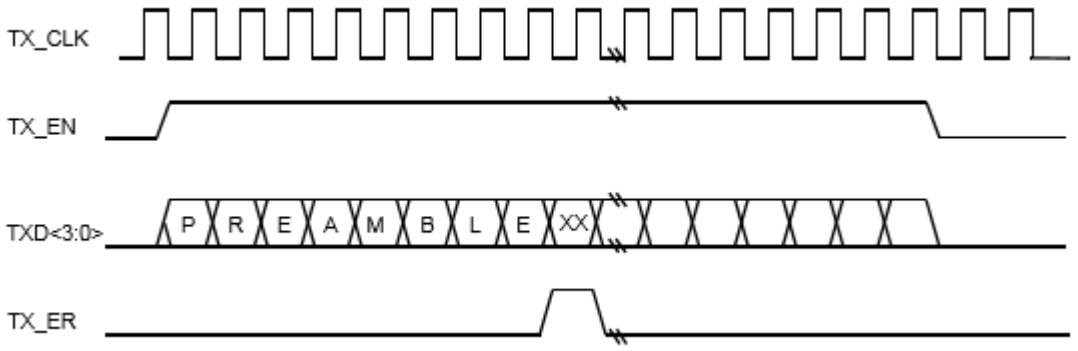
Figure 4-1. Transmission with no Collision



4.1.2 Propagating an Error

This section describes the propagation of error timing behaviour. The following figure shows the propagating an error timing waveform.

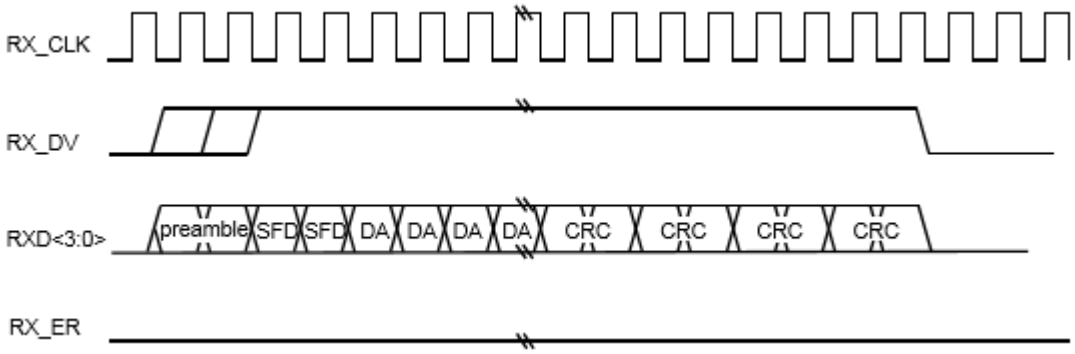
Figure 4-2. Propagating an Error



4.1.3 Reception with No Errors

This section describes the reception with no error timing behaviour. The following figure shows the reception with no error timing waveform.

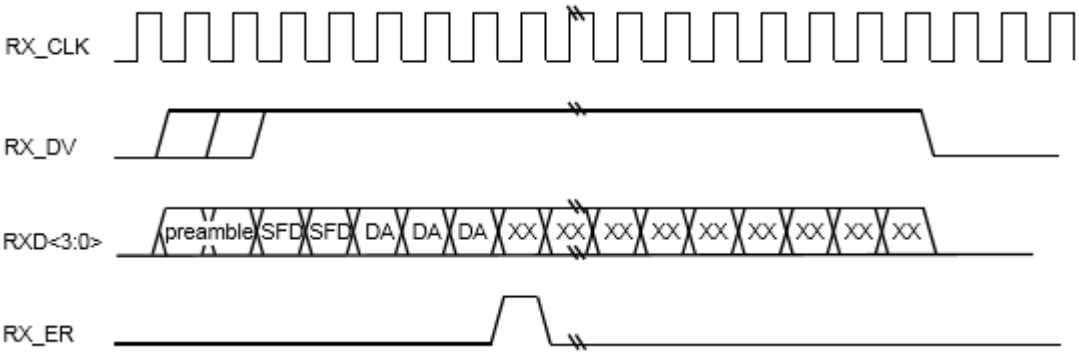
Figure 4-3. Reception With No Errors



4.1.4 Reception With Errors

This section describes the reception with error timing behaviour. The following figure shows the reception with error timing waveform.

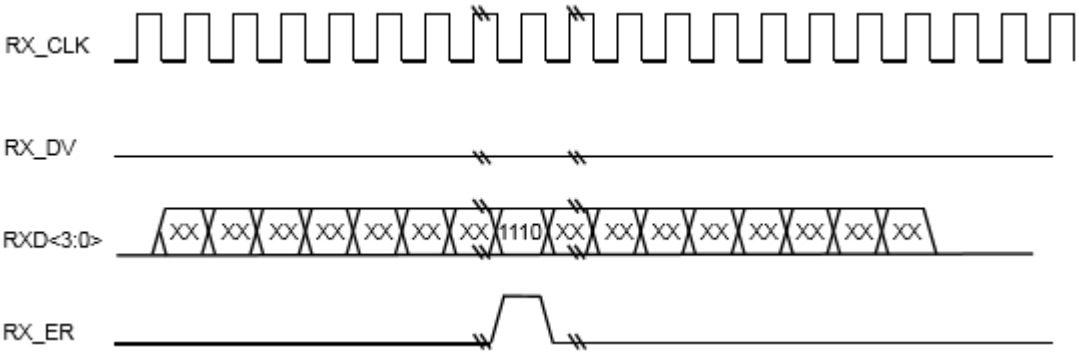
Figure 4-4. Reception With Errors



4.1.5 False Carrier Indication

This section describes the indication of false carrier timing behaviour. The following figure shows the false carrier indication timing waveform.

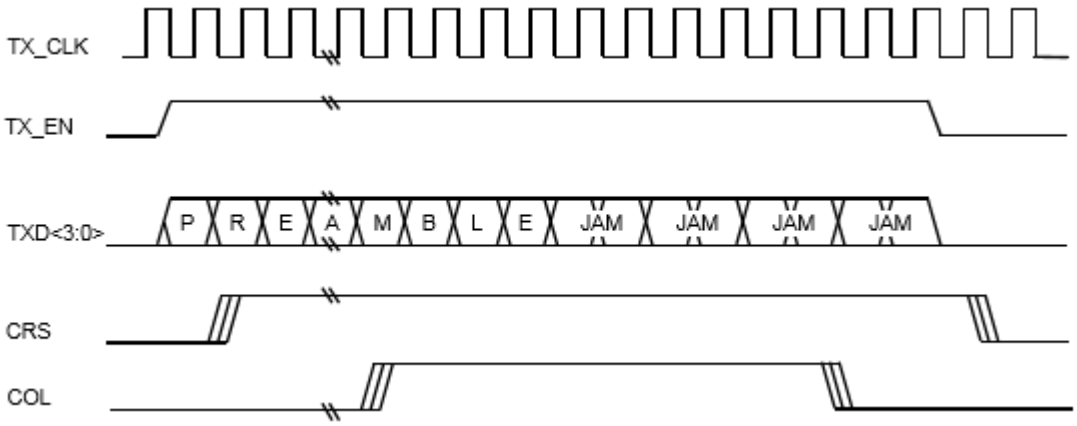
Figure 4-5. False Carrier Indication



4.1.6 Transmission with Collision

This section describes the transmission with collision timing behaviour. The following figure shows the transmission with collision timing waveform.

Figure 4-6. Transmission with Collision



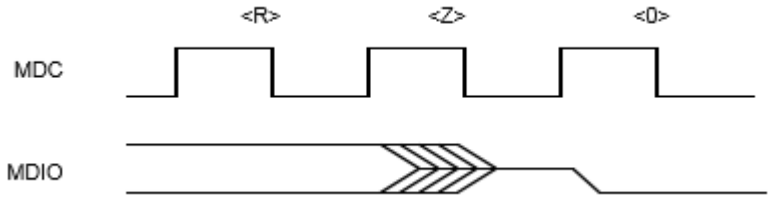
4.2 MDIO Timing Diagrams

This section describes the different timing behaviour of MDIO.

4.2.1 Behavior Of MDIO During TA Field Of Read Transaction

This section describes the behaviour of MDIO during TA field of a read transaction. The following figure shows the timing behaviour of MDIO during TA field of a read transaction.

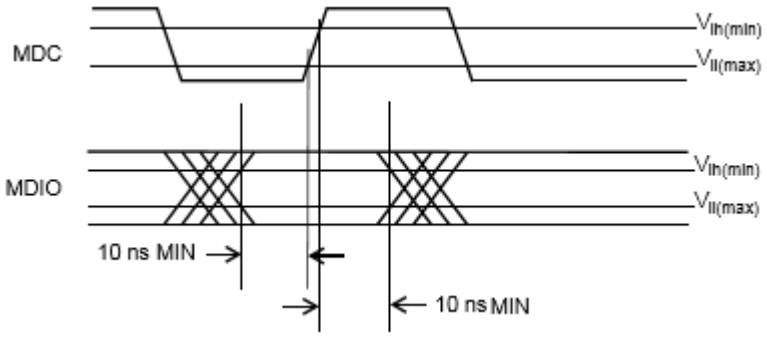
Figure 4-7. Behavior Of MDIO During TA Field Of Read Transaction



4.2.2 MDIO Sourced By STA

This section describes the behaviour of MDIO sourced by STA. The following figure shows the timing behaviour of MDIO sourced by STA .

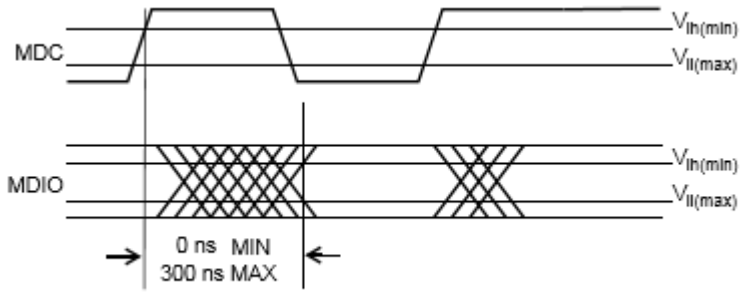
Figure 4-8. MDIO Sourced By STA



4.2.3 MDIO Sourced By PHY

This section describes the behaviour of MDIO sourced by PHY. The following figure shows the timing behaviour of MDIO sourced by PHY .

Figure 4-9. MDIO Sourced By PHY



5. Design Constraints

This section provides design constraints of CoreQSGMII.

5.1 Timing Constraints

To meet the CoreQSGMII timing requirement, it is important to provide timing constraint. You must provide set clock group timing constraint to set false path between asynchronous clocks. CoreQSGMII uses the following clocks:

Transmit path clocks

- TBI_TX_CLK
- TXCLK_P0
- TXCLK_P1
- TXCLK_P2
- TXCLK_P3

Receive path clocks

- TBI_TX_CLK
- RXCLK_P0
- RXCLK_P1
- RXCLK_P2
- RXCLK_P3
- **MDIO clock**
  MDC: All the transmit path clocks must be synchronous with each other and similarly, all the receive path clocks must be synchronous with each other. MDC clock can be generated from one of the transmit path clocks or one of the receive path clocks. MDC clock can also be generated independently from transmit path clocks or receive path clocks.

  In the following example, the MDC clock is assumed to be synchronous with transmit path clock TBI_TX_CLK, and all TX_CLK_Px (x represents range from 0 to 3), and TBI_TX_CLK is connected to same clock source and similarly all the RX_CLK_Px (x represents range from 0 to 3) and TBI_RX_CLK is connected to same clock source .

```
set_clock_group -asynchronous -group {PF_XCVR_ERM_C0_0/I_XCVR/LANE0/TX_CLK_R MDC}\-group
{PF_XCVR_ERM_C0_0/I_XCVR/LANE0/RX_CLK_R}
```

  The source clock name used in the preceding example is for reference only. The source name may be different in your design, and you must change the clock name in the constraint accordingly. You can find reference sdc timing constraint file from the following path.

```
<project_directory/component/Actel/DirectCore/CoreQSGMII/2.2.xxx/constraints/
CoreQSGMII.sdc>
```

6. Tool Flow

This section discuss the tool flow of QSGMII.

6.1 License

CoreQSGMII is available with evaluation and obfuscated RTL license.

6.1.1 Obfuscated

Obfuscated license is a license locked. Enabling the core to be instantiated with SmartDesign. Simulation, Synthesis, and Layout are performed with Libero software. The RTL code for the core is obfuscated and encrypted.

6.1.2 Evaluation

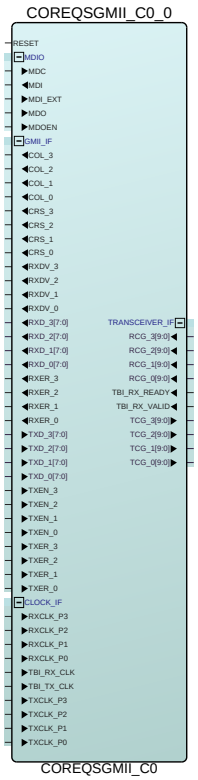
The RTL code for the core is obfuscated and encrypted and has a self-destruct feature that stops functioning after four hours at 1.25 Gbps data rate.

6.2 SmartDesign

CoreQSGMII is preinstalled in SmartDesign IP Deployment design environment. The core must be configured using the configuration GUI within SmartDesign, see the following figure.

To know how to create SmartDesign project using the IP cores, see Libero SoC Documentation and use the latest *SmartDesign User Guide*.

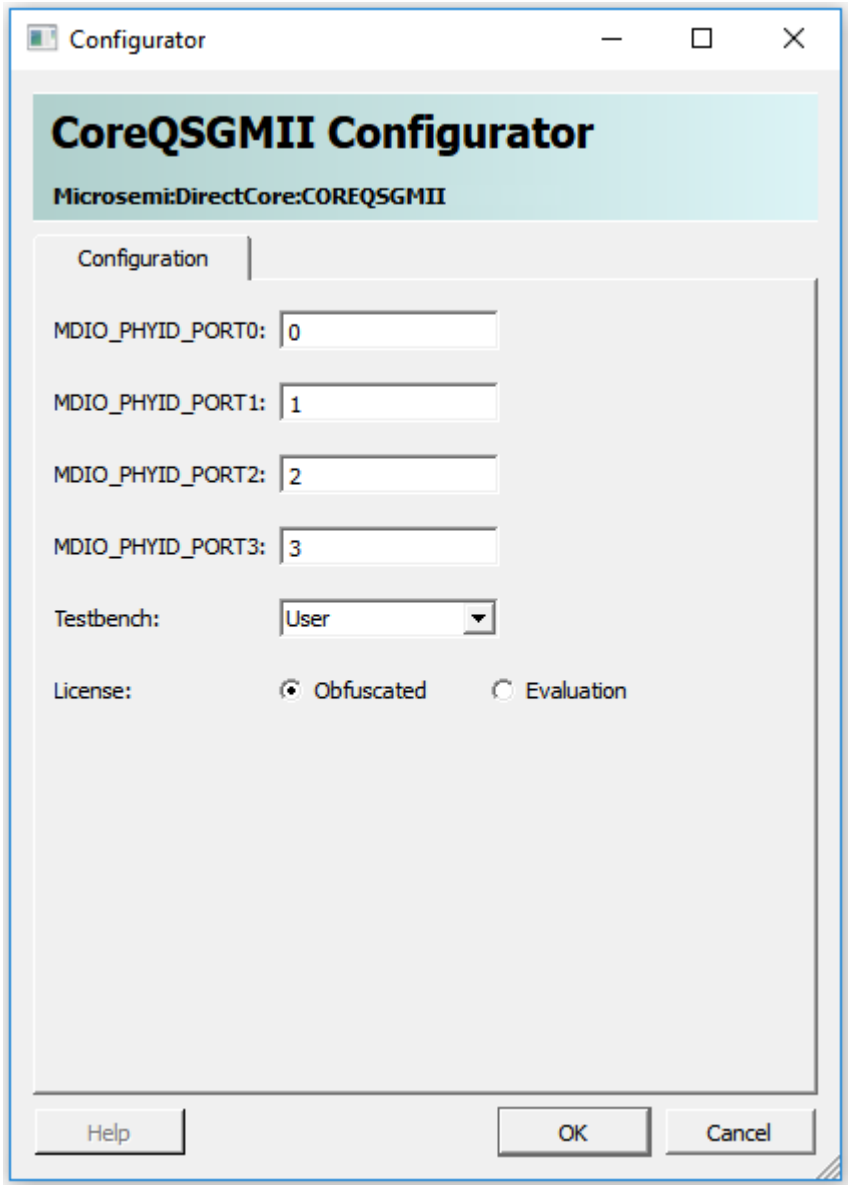
Figure 6-1. SmartDesign CoreQSGMII Instance View



6.3 Configuring CoreQSGMII in SmartDesign

The following figure shows the options available in the **Configuration** tab.

Figure 6-2. CoreQSGMII SmartDesign Configuration GUI



6.4 Simulation Flows

The User Testbench for CoreQSGMII is included in all releases. To run simulation flows, perform the following steps:

1. To run simulations, select the **User Testbench flow** within the SmartDesign CoreQSGMII configuration GUI, right-click the **canvas**, and select **Generate Design**.
2. When SmartDesign generates the design files, it installs the user testbench files.
3. To run the user testbench, set the design root to the CoreQSGMII instantiation in the Libero SoC design hierarchy pane and click **Simulation** in the **Libero SoC Design Flow** window. This invokes ModelSim® and automatically runs the simulation.

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6.5 Synthesis in Libero

To run synthesis in Libero, perform the following steps:

1. After setting the design root appropriately for your design, click **Synthesis** in the Libero SoC software.
2. The **Synthesis** window appears, displaying the Synplicity® project. Set Synplicity to Verilog 2001 standard if Verilog is being used. To run Synthesis, click **Run**.

6.6 Place-and-Route in Libero

To run place-and-route, perform the following steps:

1. After the design is synthesized, run the compilation and the place and-route tools.
2. Click the **Layout** icon in the Libero SoC to invoke Designer. CoreQSGMII requires no special place-and-route settings.

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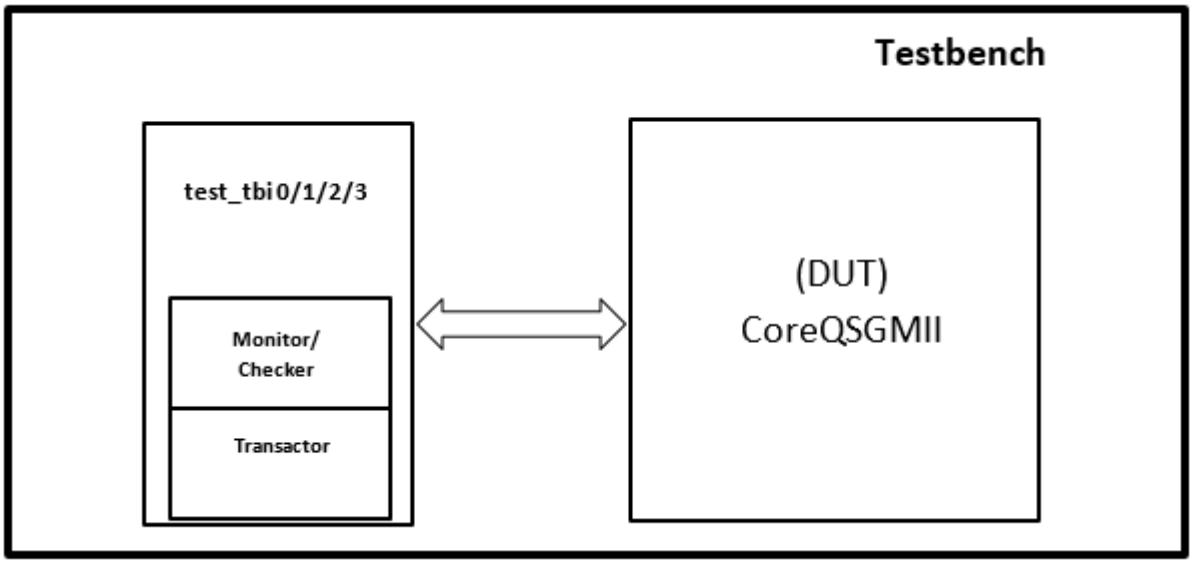
7. User Testbench

CoreQSGMII user testbench gives an example of how to use the core. The following figure shows the simulation testbench including an instantiation of the CoreQSGMII DUT and the Test TBI module.

Figure 7-1. CoreQSGMII User Testbench



The transactor in the Test TBI module generates the G/MII data on TXD output and receives RXD input to/from the DUT (CoreQSGMII). The monitor/checker checks for the TCG data from the DUT and sends the loopback data to DUT. The purpose of the testbench is to test the functionality of the core by inputting known data, monitoring the output, and checking for expected results.

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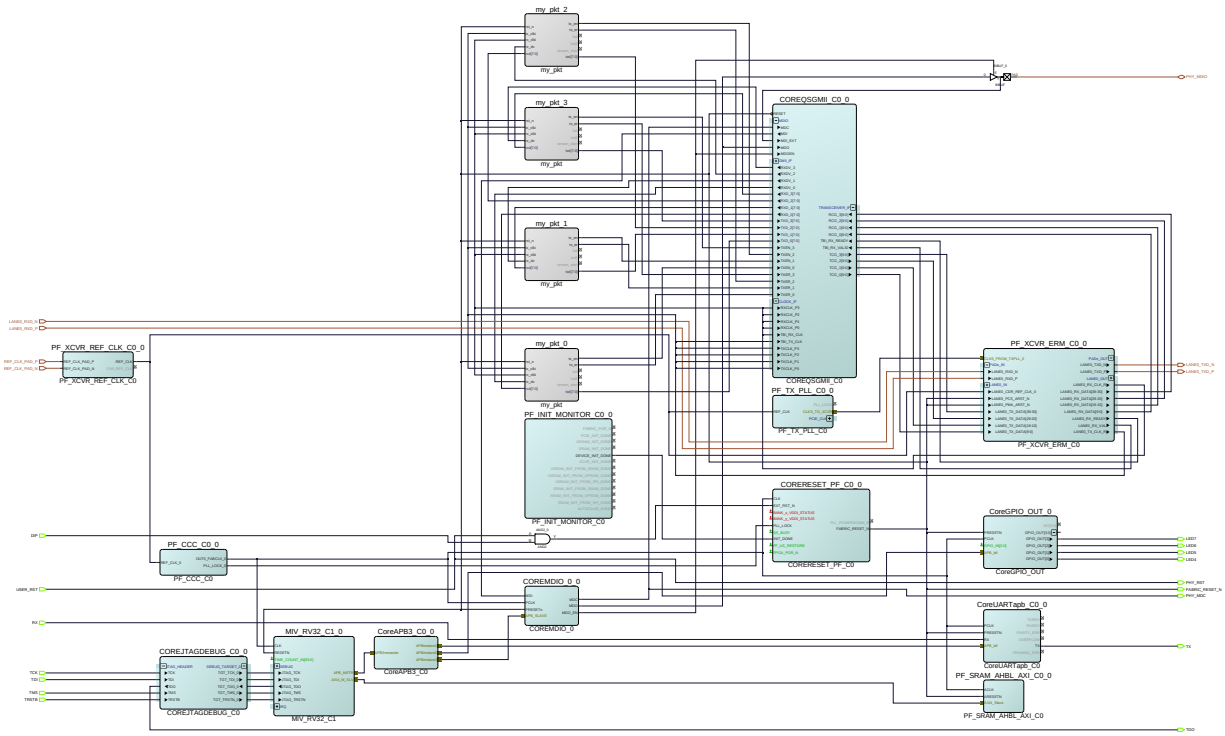
8. System Integration

The example design explains the CoreQSGMII features and implements the loopback at Transceiver pad level for 1000 Mbps mode on each of four ports on the PolarFire and PolarFire SoC Evaluation Kit. The following figure shows the CoreQSGMII example design.

Figure 8-1. CoreQSGMII Example Design



The following are the descriptions of CoreQSGMII example design.

- On board user RESET and DEVICE_INIT_DONE of PF_INIT_MONITOR_C0_0 are used as reset for COREQSGMII_C0_0
- COREQSGMII_C0_0 has TXCLK_P0, TXCLK_P1, TXCLK_P2, TXCLK_P3, RXCLK_P0, RXCLK_P1, RXCLK_P2, RXCLK_P3, TBI_TX_CLK, TBI_RX_CLK, and MDC clocks
- TXCLK_P0, TXCLK_P1, TXCLK_P2, TXCLK_P3, and TBI_TX_CLK are connected to 125 MHz LANE0_TX_CLK_R of PF_XCVR_ERM_C0_0
- RXCLK_P0, RXCLK_P1, RXCLK_P2, RXCLK_P3, and TBI_RX_CLK are connected to 125 MHz LANE0_RX_CLK_R of PF_XCVR_ERM_C0_0
- MIV_RV32_C1 application configures the management interface of COREQSGMII_C0_0 through COREMDIO
- my_pkt_0, my_pkt_1, my_pkt_2, and my_pkt_3 are user defined modules for generating GMII data to each port of COREQSGMII_C0_0. The TBI data is sent to PF_XCVR_ERM_C0_0 and looped back at TX/RX pads of PF_XCVR_ERM_C0_0.

Important: Set 'Synthesis gate level netlist format' to 'Verilog netlist' in case this setting is optional in **Libero** > **Project** > **Project Settings** > **Design Flow**.

Run the Libero flow with enabling the **Timing Driven** and **Repair Minimum Delay Violations**.

Important: The example design can be obtained from the Microchip technical support team.

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
A	10/2022	The following is a summary of the changes made in revision A of this document: • Migrated the document from Microsemi template to Microchip template • Updated the version of CoreQSGMII throughout the document • Replaced Table 1 • Replaced Table 2-2 and Table 2-3 with the previious table • Added new tables in 3. Register Map and Descriptions • Added 5. Design Constraints
2.0	_	Added PolarFire® SoC support.
1.0	_	The first publication of this document.

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ISBN: 978-1-6683-1381-7

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