# EVB-LAN9662 Evaluation Board User's Guide

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**NOTES:**

# Preface

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**For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.**

## INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-LAN9662 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

## DOCUMENT LAYOUT

This document features the EVB-LAN9662 Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Overview"** – This chapter provides a brief overview of the EVB-LAN9662 evaluation board and its features.
- **Chapter 2. "Management Software"** – This chapter provides information on the software management and debugging of the EVB-LAN9662.
- **Chapter 3. "EVB-LAN9662 End-Node and EVB-LAN9662-Carrier Boards"** – This chapter gives an overview of the EVB-LAN9662 End-Node and EVB-LAN9662-Carrier for the EVB-LAN9662.
- **Chapter 4. "EVB-LAN9662 End-Node Hardware Details"** – This chapter provides hardware details of the EVB-LAN9662 End-Node module.
- **Chapter 5. "EVB-LAN9662-Carrier Hardware Details"** – This chapter provides hardware details of the EVB-LAN9662-Carrier board.
- **Appendix A. "PCB Layout and Silk Screens"** – This appendix shows the PCB layout and silk screen images of EVB-LAN9662 End-Node and EVB-LAN9662-Carrier.

## CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

**DOCUMENTATION CONVENTIONS**

| Description | Represents | Examples |
|---|---|---|
| **Arial font:** | | |
| Italic characters | Referenced books | *MPLAB® IDE User's Guide* |
| | Emphasized text | ...is the *only* compiler... |
| Initial caps | A window | the Output window |
| | A dialog | the Settings dialog |
| | A menu selection | select Enable Programmer |
| Quotes | A field name in a window or dialog | "Save project before build" |
| Underlined, italic text with right angle bracket | A menu path | *File>Save* |
| Bold characters | A dialog button | Click **OK** |
| | A tab | Click the **Power** tab |
| N'Rnnnn | A number in verilog format, where N is the total number of digits, R is the radix and n is a digit. | 4'b0010, 2'hF1 |
| Text in angle brackets < > | A key on the keyboard | Press <Enter>, <F1> |
| **Courier New font:** | | |
| Plain Courier New | Sample source code | `#define START` |
| | Filenames | `autoexec.bat` |
| | File paths | `c:\mcc18\h` |
| | Keywords | `_asm, _endasm, static` |
| | Command-line options | `-Opa+, -Opa-` |
| | Bit values | `0, 1` |
| | Constants | `0xFF, 'A'` |
| Italic Courier New | A variable argument | *`file.o`*`, where `*`file`*` can be any valid filename` |
| Square brackets [ ] | Optional arguments | `mcc18 [options] file [options]` |
| Curly brackets and pipe character: { \| } | Choice of mutually exclusive arguments; an OR selection | `errorlevel {0\|1}` |
| Ellipses... | Replaces repeated text | `var_name [, var_name...]` |
| | Represents code supplied by user | `void main (void) { ... }` |

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICkit™ 2 and 3.

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- Embedded Solutions Engineer (ESE)
- Technical Support

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Technical support is available through the website at:
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## DOCUMENT REVISION HISTORY

| Revisions | Section/Figure/Entry | Correction |
|---|---|---|
| DS50003432B (07-10-24) | Figure 4-1 | Updated block diagram. |
| | Figure 5-1 | Updated block diagram. |
| | All | Made minor formatting changes.<br>Changed all occurrences of UNG8309(B) to LAN9662-Carrier.<br>Changed all occurrences of UNG8291(C) to EVB-LAN9662 End-Node. |
| DS50003432A (11-04-22) | Initial release | |

# Chapter 1. Overview

## 1.1 INTRODUCTION

This hardware manual describes the design of the LAN9662 End-Node module and its associated carrier board, demonstrating the LAN9662 TSN Ethernet switch architecture with Real-Time Engine (RTE) functionality. The LAN9662 End-Node module is based on the EVB-LAN9662 End-Node reference design, and the carrier board is based on EVB-LAN9662-Carrier reference design.

This document is intended primarily for hardware and software engineers who want to get an overview of designing products based on the LAN9662.

## 1.2 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN9662 Data Sheet*
- *EVB-LAN9662 End-Node Reference Design Schematic*
- *EVB-LAN9662-Carrier Reference Design Schematic*
- *IO-FPGA Feature Specification*

## 1.3 TERMS AND ABBREVIATIONS

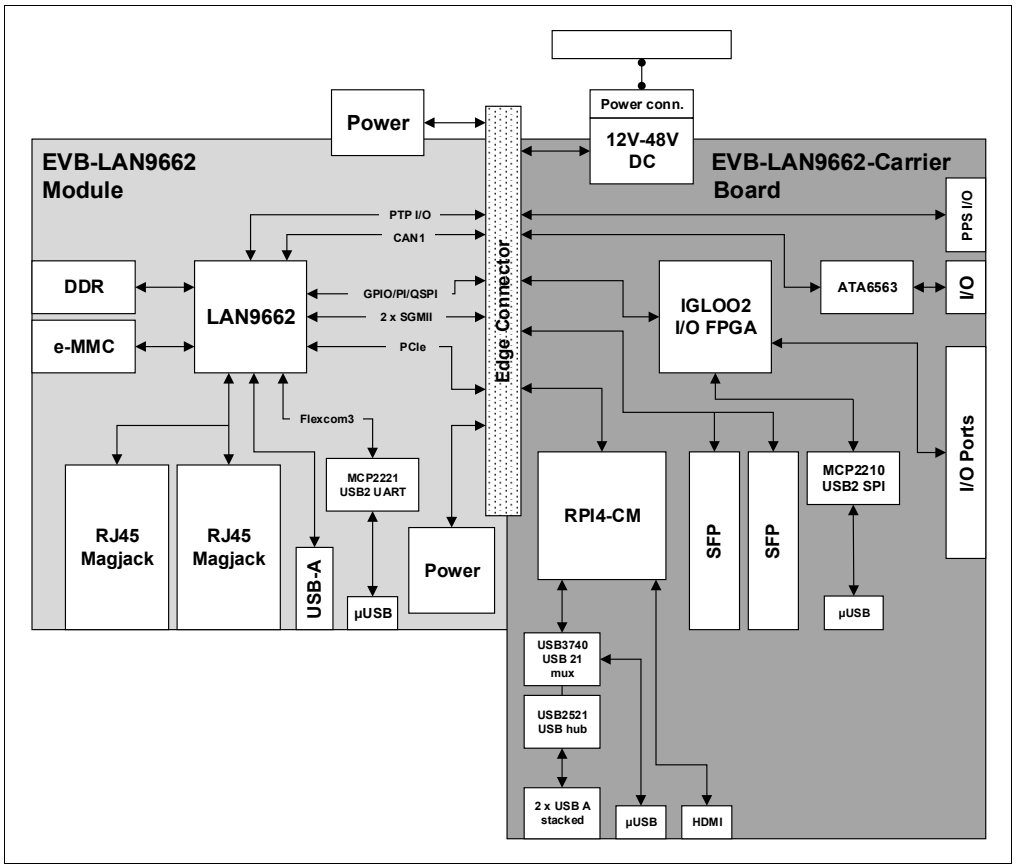
The following are the terms and abbreviations used in this document:

- AMS – Automatic Media-Sense
- CLI – Command Line Interface
- EMI – Electromagnetic Interference, emissions
- HAT – Hardware Attached on Top
- JTAG – Joint Test Access Group, IEEE1149
- LVDS – Low Voltage Differential Signaling
- LVTTL – Low Voltage TTL
- PCS – Physical Coding Sublayer
- PHY – Physical Layer Device
- PTP – Precision Time Protocol, IEEE1588
- RTE – Real-Time Engine
- SI – Serial Interface, SPI
- SME – Small/Medium Enterprise
- SSM – Synchronization Status Message
- SyncE – Synchronous Ethernet, ITU-T G.8262/Y.1362

## 1.4 EVB-LAN9662 OVERVIEW

Figure 1-1 shows how the two PCBs (EVB-LAN9662 End-Node module and EVB-LAN9662-Carrier) are interconnected through a low-cost, 260-pin SO-DIMM socket (referenced here as the Edge connector) to extend the functionality of the EVB-LAN9662.

**FIGURE 1-1: EVB-LAN9662 BLOCK DIAGRAM**




The setup is designed to demonstrate the following use cases:

- 4-port Profinet input/output (I/O) device with digital I/O
- 4-port Profinet PLC with local digital I/O using the internal CPU (low cost)
- 4-port Profinet PLC with local digital I/O with high performance external CPU via PCIe®
- 4-port Ethernet media conversion
- OPC/UA endpoints
- Ultra fast frame manipulation for cyclical data flows

## 1.5 FEATURES

The EVB-LAN9662 is a managed end-node module with expansion headers for all other than the basic functionality of the LAN9662. The module features:

- LAN9662 AVB/TSN switch with internal Real-Time Engine and 600 MHz ARM Cortex A7 CPU
- Two tri-speed (10/100/1000M) RJ45 front ports using internal copper PHYs
- USB 2.0 host port (female type-A connector)
- micro-USB 2.0 console port for local management and debugging through a

Linux® driver
- Reset status LED and per-network port status LEDs for link and activity indication
- Reset button
- 2x20, 0.1” Expansion pin header exposing various interfaces: UART, SPI, $I^2C$, PTP, CAN, and IRQ
- Powered from either micro-USB port, the Edge connector, or the Expansion header

The EVB-LAN9662-Carrier board exposes more interfaces and functionality of the LAN9662 device. The carrier board is designed to hold the end-node module and provides the following additional features:

- Two SFP slots connected to the internal SerDes ports on LAN9662 to provide support for 100BASE-FX, 1000BASE-X, and 2.5GBASE-X/KX interfaces
- One CAN interface using ATA6563 CAN transceiver
- Support for Raspberry Pi compute module 4 as an external CPU system, connected via PCIe and SPI (https://www.raspberrypi.org/products/compute-module-4/?variant=raspberry-pi-cm4001000)
  - One HDMI
  - Two USB 2.0 host ports
  - One micro SD card connector
  - One micro-USB console/upgrade port
- Two SMA connectors for PTP/IEEE1588v2 applications: 1PPS input and 1PPS output
- Two FLEXCOMs
  - FLEXCOM 2 is currently unused, but can be configured to support RS232 UART, $I^2C$, and RS422
  - FLEXCOM 4 configured as $I^2C$ attached to the SFP module $I^2C$ ports
- IGLOO2 M2GL050T on-board FPGA implementing the IO-FPGA functionality (see the *IO-FPGA Feature Specification* document)
  - Connection to the LAN9662 using QSPI1 or PI
  - Digital I/O ports for a Profinet/OPC-UA end-node applications
    a) 16 digital input ports with 16 associated status LEDs
    b) 16 digital output ports with 16 associated status LEDs
  - One debug SPI interface connected to a MCP2210 USB-to-SPI device
  - One debug SPI interface connected to a pin header (LVTTL levels)
- 12V-30V DC power input Jack (5.5 mm/2.5 mm center pin), powering the carrier board, as well as the attachable modules: LAN9662 End-Node module and Raspberry Pi compute module 4

## 1.6 CPU SYSTEM

### 1.6.1 Embedded ARM® Cortex A7 CPU System

By default, the LAN9662 switch core is managed by its embedded CPU system with on-board SDRAM and SPI boot from either e-MMC™ NAND or NOR Flash device or using both:

- Embedded ARM Cortex A7 single core 32-bit processor operating at 600 MHz.
- External memories, which include 1 GB (512 MBx16) DDR3L-1333 SDRAM (can be upgraded to 2 GB), 4 GB e-MMC QSPI NAND, and (optionally mounted) 2 MB NOR Flash device.

The Flash devices are used as second stage bootloader in the secure boot environment.

### 1.6.2 External CPU Interfaces

An external host CPU system can be connected to and control the LAN9662 configured as a client device through the external CPU, using either:

- PCIe 2.0 endpoint connection through the EVB-LAN9662 Edge connector to an external host system located on EVB-LAN9662-Carrier board Raspberry Pi compute module 4 connectors
- SPI, serial register access through the switch SPI client interface exposed in the Edge connector

Both the PCIe 2.0 endpoint and the SPI client are set up through specific boot modes. See Table 4-1.

## 1.7 MANAGEMENT

The embedded CPU system is locally managed through a Switchdev driver running under the Linux command prompt by using the micro-USB connection on the EVB-LAN9662 module and a standard terminal application, like PuTTY or TeraTerm.

## 1.8 NETWORK PORTS

The end-node module offers two tri-speed Cu PHY ports, which have low EMI line drivers with integrated line-side termination resistors and support for HP Auto MDI-/MDI-X™, and operates over standard Category 5 cabling at 10/100/1000 Mbit/s and Category 3 cabling at 10 Mbit/s.

The carrier board offers additional two SFP slots connected to the LAN9662 through the Edge connector, supporting 100BASE-FX, 1000BASE-X with Clause 37 ANEG and 2.5GBASE-X Optical SFP modules, Cu SFP modules with the Cisco defined SGMII ANEG running or SFP DAC cabling for 2.5G SGMII+.

## 1.9 TIMING AND SYNCHRONIZATION

### 1.9.1 SyncE

SyncE is not supported on this evaluation platform.

### 1.9.2 PTP/IEEE1588v2/802.1AS-2020

PTP interfacing is available through all network ports with high accuracy timestamping in the LAN9662 and through input and output of 1PPS SMA connectors.

The LAN9662 can be configured as a boundary clock, transparent clock, PTP timeTransmitter, or PTP timeReceiver. LAN9662 supports both one-step and two-step operations. Multiple time domains are available.

# Chapter 2. Management Software

## 2.1 INTRODUCTION

The EVB-LAN9662 evaluation board is managed through a console port using standard Linux commands.

## 2.2 SWITCHDEV FOR MANAGEMENT AND DEBUGGING

The EVB-LAN9662 End-Node module can be connected directly to a laptop USB port using a basic USB 2.0 A-Male to Micro-B cable to access the Linux CLI running on the switch.

When connected, the laptop will detect the end-node module's on-board USB controller.

Set up the baud-rate, data bits, parity and flow control in the terminal program running on the laptop. Default settings are: 8 data bits, 1 stop bit, no parity, 115200 baud and without flow control.

The Switchdev driver for LAN9662 is integrated into the Linux kernel, so that users will not detect if standard Linux software forwarding is used, or if the functionality is offloaded by the LAN9662.

Log in as `root`. Help is available through the normal Linux help commands. The default startup mode is NIC functionality with no frame-forwarding. When bridges are added to the configuration, the Switchdev driver will offload this to the LAN9662. Most of the configuration is done by using standard Linux commands from `iproute2` or the `libnl` library.

Example 2-1 shows some examples of the Switchdev commands supported.

**EXAMPLE 2-1: SUPPORTED SWITCHDEV COMMANDS**

```
// Check Link status
# ip –c link

// Enable port 0
# ip link set dev eth0 up

// Set MAC address for port 0
# ip link set dev eth0 address 00:00:00:22:22:22

// Set IPv4 address for port 0
# ip address add dev eth0 1.0.1.100/24

// Show link details
# ip -d link show dev eth0
4: eth0: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc mq state UP mode DEFAULT
group default qlen 1000
    link/ether 00:00:00:22:22:22 brd ff:ff:ff:ff:ff:ff permaddr 8a:64:b8:b3:63:63
promiscuity 0 minmtu 68 maxmtu 9600 addrgenmode eui64 numtxqueues 8 numrxqueues 1
gso_max_size 65536 gso_max_segs 65535 portname p2 switchid 8a64b8b36360 parentbus
platform parentdev e2000000.switch

// Show statistics
# ip -s link show dev eth0
4: eth0: <BROADCAST,MULTICAST,UP,LOWER_UP> mtu 1500 qdisc mq state UP mode DEFAULT
group default qlen 1000
    link/ether 00:00:00:22:22:22 brd ff:ff:ff:ff:ff:ff permaddr 8a:64:b8:b3:63:63
    RX:  bytes packets errors dropped  missed   mcast
         38311     473      0      25       0     353
    TX:  bytes packets errors dropped carrier collsns
         11386     115      0       0       0       0

// Show speed and duplex
# ethtool eth0
Settings for eth0:
        Supported ports: [ TP MII ]
        Supported link modes:   10baseT/Half 10baseT/Full
                                100baseT/Half 100baseT/Full
                                1000baseT/Half 1000baseT/Full
```

# Chapter 3. EVB-LAN9662 End-Node and EVB-LAN9662-Carrier Boards

## 3.1 INTRODUCTION

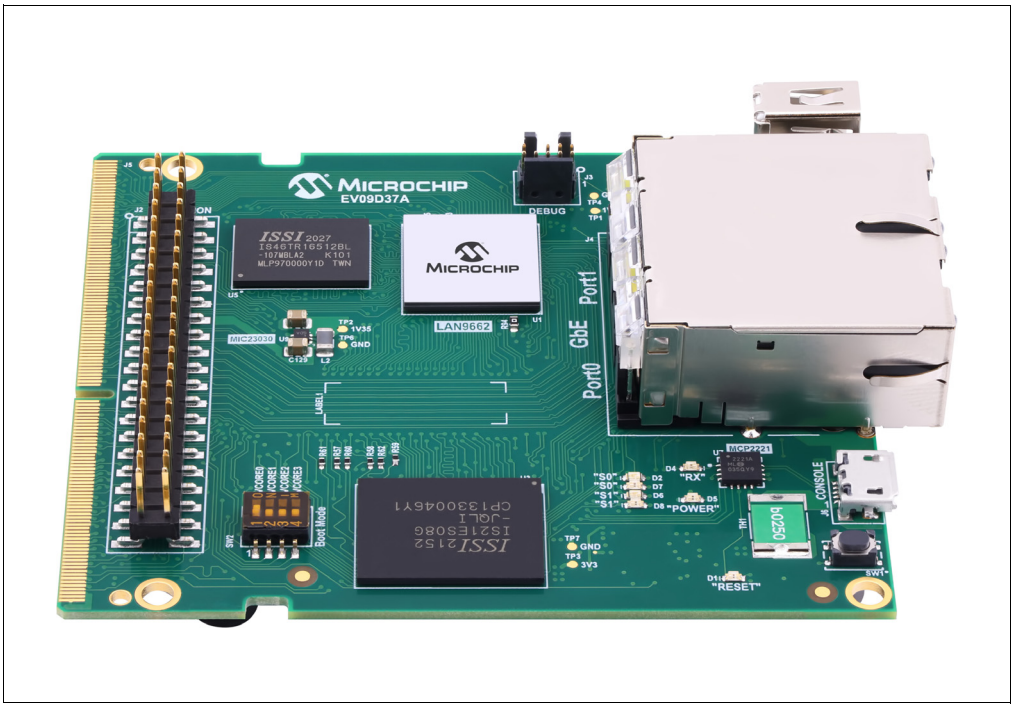
This section gives an overview of the EVB-LAN9662 End-Node module and EVB-LAN9662-Carrier board.

## 3.2 EVB-LAN9662 END-NODE MODULE

### 3.2.1 Board Overview

Figure 3-1 shows the component placement on the EVB-LAN9662 PCB.

**FIGURE 3-1: EVB-LAN9662 END-NODE MODULE**




### 3.2.2 Power DC Input and LED

The end-node module can be powered (with +5V DC) through the micro-USB connector and hereby work as a standalone system, or it can be 5V DC powered through either the Edge connector or the Expansion header.

A power source switch circuitry controls whether the 5V_USB or 5V from the connectors is being used. That is, when the 5V supply on the connectors is higher than the 5V_USB supply, the 5V_USB supply is disconnected. On-board voltage regulators then supply the different voltages needed.

The total power worst-case consumption as standalone, including conversion loss, is 3.8W, 5V at 0.75A.

The total power consumption with the carrier board in use, including conversion loss, is 4.8W, 5V at 1.0A.

A single green LED (D5) indicates Power-ON using the 3.3V supply.

### 3.2.3 Reset Button and LED

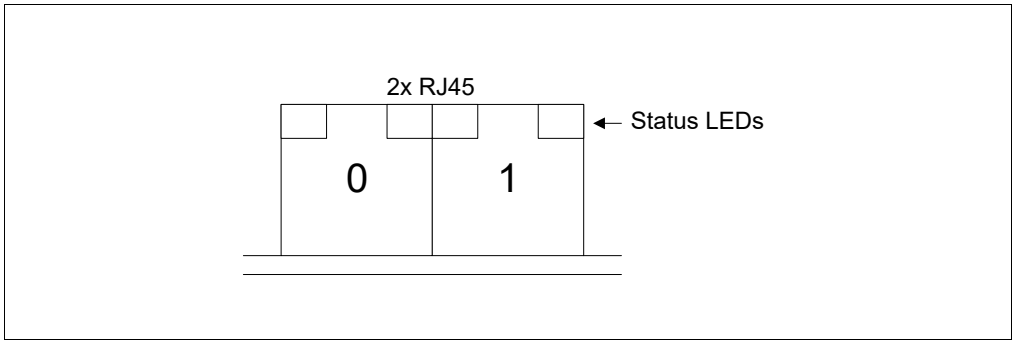
A Reset button is available on the end-node module. When pressed, it drives the input of the voltage supervisor low, creating a hard reset to the module. A red LED (D1) is used for indication.

If the Reset button is held, Reset is released. The state of the reset button can be read by the software, once it is running again, to determine 'long press' and hereby resetting the module back to the default setup.

### 3.2.4 Front Port Layout and LEDs

Figure 3-2 shows the front port layout on the end-node module.

**FIGURE 3-2: FRONT PORT LAYOUT ON EVB-LAN9662 END-NODE**




On each RJ45 slot in the ICM are two LEDs (green/yellow). These port status LEDs are automatically controlled by the LAN9662 serial GPIO controller. Currently, the left LED signals 1G link/traffic (green solid/blinks) and the right LED signals 10/100M link/traffic (yellow solid/blinks).

Likewise, for the two SerDes ports (S0 and S1) provided in the Edge connector, two LEDs (blue/green) per port are available on the end-node module.

### 3.2.5 micro-USB 2.0 Console Port

The end-node module can be controlled through a standard serial micro-USB female type-B connector, J6, by using Linux CLI commands from a terminal application, like PuTTY or TeraTerm.

The USB port connects to USB-to-UART converter using FLEXCOM 3b on LAN9662.

A single green LED (D4) indicates UART RX activity.

### 3.2.6 USB 2.0 Host Port

The end-node module also supports being a USB host by using a USB female type-A connector. The actual host capabilities depend on the Linux OS system.

An on-board Power Distribution MOSFET switch provides the 5V_host sourcing, limited to 600 mA.

### 3.2.7 PCIe® 2.0 Endpoint

The end-node module offers PCIe 2.0 endpoint connection through the Edge connector. It can only be used together with the carrier board.

### 3.2.8 ARM® CPU JTAG Connector

The end-node module offers a standard 10-pin (0.05”) ARM CPU JTAG header, J3, to be used for boundary scan and In-Circuit Emulator (ICE). ICE can be used for debugging functions, such as downloading code and single-stepping through programs.

### 3.2.9 Expansion Header

The 2x10, 0.1” pin Expansion header is targeting Raspberry Pi compatibility. It can give an external CPU control over the SPI client register access interface or can be used for programming the on-board NOR Flash device.

The Expansion header exposes various GPIO signals in Alternate mode:

- UART: RXD, TXD (FLEXCOM 0b)
- $I^2C$: SCL, SDA (FLEXCOM 1c)
- $I^2C$: SCL, SDA (FLEXCOM 4b)
- SPI: SCLK, MISO, MOSI + 5/6 Flex_Shared nCS (FLEXCOM 2b)
- SPI.SCK, SPI.D1, SPI.D0 and SPI.nCS (NOR Flash device or LAN9662)

The remaining Expansion header GPIO signals can function as normal GPIO pins, when using default software settings. However, they can also be enabled with LAN9662-specific functionality, which is not found in the originally Raspberry Pi header.

- CAN 0-1
- Recovered clock 0-1
- MII-Management (mode B)
- IRQ or TRG
- PWM
- PTP 1, 2, 4

Likewise, the on-board boot mode strapping, **VCORE_CFG[3:0]**, can be overruled through the Expansion header.

### 3.2.10 Edge Connector

A 260-pin SO-DIMM socket on the EVB-LAN9662-Carrier board is used for the interconnection with the male part on the EVB-LAN9662 End-Node module.

This Edge connector exposes the following direct interfaces on LAN9662:

- SerDes port 0, 1 (and 2—only in LAN9668)
- PCIe 2.0 endpoint
- QSPI0

The Edge connector also exposes *all* LAN9662 GPIO pins, giving access to:

- CAN 0-1
- End-node RTE functionality (Profinet/OPC-UA)
- SGPIO to control port LEDs and SFP MSA signals
- PTP 1, 2, 3 and 4
- FLEXCOM 1c ($I^2C$), FLEXCOM 2b (SPI), FLEXCOM3b (UART), FLEXCOM 4b ($I^2C$)
- QSPI1
- 16-bit parallel interface (overrules FLEXCOM 0b usage in the Expansion header)
- All strapping pins used for VCORE_CFG, JTAG and PLL

### 3.2.11 Boot Modes and Reference Clock

The LAN9662 boot mode can be selected through a 4-pin DIP switch, SW2. The system default is either set to '0000' or '0001' for boot-up from either e-MMC or a NOR Flash device, respectively. Additionally, it is possible to strap the switch core and SerDes/PHY reference clocks mode and frequency through strapping pins by using on-board resistors. The default setup is 25 MHz core clock and SerDes/PHY clock.

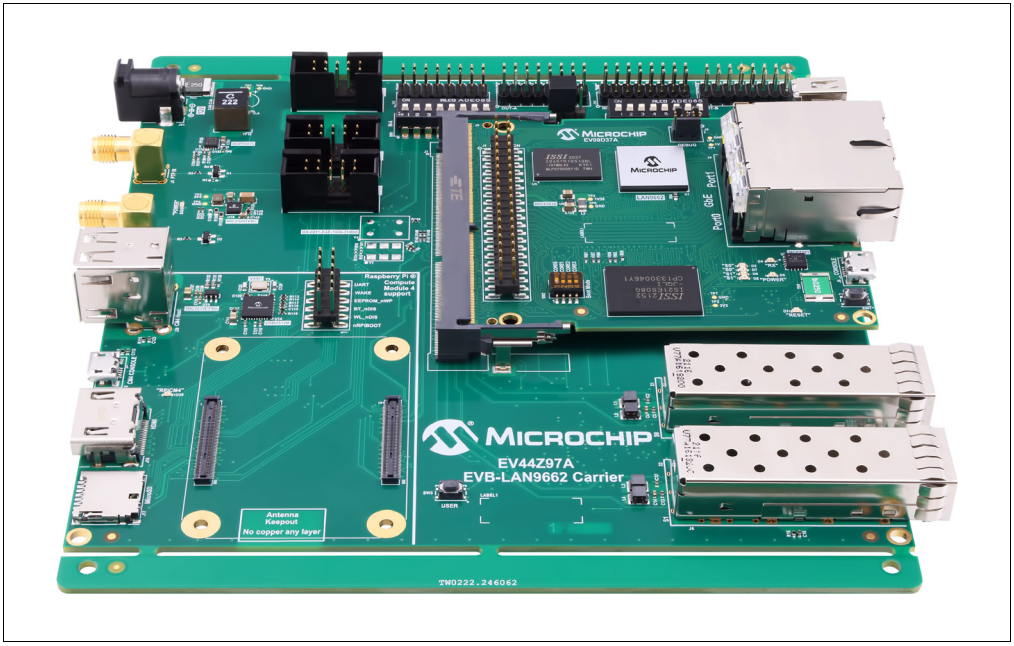
## 3.3 EVB-LAN9662-CARRIER BOARD FOR EVB-LAN9662

### 3.3.1 Board Overview

The EVB-LAN9662-Carrier board is designed so that the EVB-LAN9662 End-Node module can be placed with its RJ45 connector facing up and in the same direction as the SFP ports.

Figure 3-3 shows the component placement on the EVB-LAN9662-Carrier PCB.

**FIGURE 3-3: EVB-LAN9662-CARRIER BOARD MODULE**




### 3.3.2 Power DC Input and LED

The carrier board is intended to be 12 VDC/2A powered through a standard input jack. However, the on-board buck step-down DC-DC regulator behind accepts 7.5V to 30V input range to deliver a 5V output.

The 5 VDC output powers the EVB-LAN9662 End-Node module, the CM4 module, HDMI interface, CAN bus, USB host and the carrier board's own local DC/DC converters: 1.2V/1.2A, 2.5V/0.2A and 3.3V/1A.

A single green LED (D43) indicates power-on using the 3.3V supply.

### 3.3.3 SFP Connectors with Associated Status LEDs

The carrier board provides two SFP slots for the LAN9662 SerDes ports.

LAN9662 drives the $I^2C$ SCL and SDA signals to the SFP slots, so SFP modules can be auto-detected. Likewise, the LAN9662 also interfaces with each SFP module MSA-defined signals.

Two bi-color status LEDs (green/red) are available for each SFP slot. The LED signals 1G link/traffic with green solid/blinks and 100M link/traffic with yellow solid/blinks.

### 3.3.4 SMA Connectors at Rear

The carrier board provides two SMA connectors for PTP applications. One is used as 1PPS output and the other as 1PPS input. The output uses LVTTL levels. The input is LVTTL and 3V3-tolerant.

### 3.3.5 CAN BUS Header

The carrier board provides a 10-pin header to access the CAN BUS provided by LAN9662 CAN1 interface.

### 3.3.6 IO-FPGA for RTE Support

Digital I/O ports for Profinet/OPC-UA end-node applications are implemented in an on-board FPGA. LAN9662 GPIO pins are all connected to the IO-FPGA. This includes the RTE-associated QSPI1 and parallel interfaces.

The IO-FPGA provides 16 digital outputs and 16 digital inputs. For optional use or debug, there are 16 DIP switches, which can force the individual inputs high. Likewise, a User button is available to drive a low signal to the IO-FPGA.

Individual green status LEDs are provided for each of the 32 I/Os. Two extra LEDs, green and yellow, can be used for additional FPGA status indication.

The carrier board provides different control and debug connectors associated with the IO-FPGA:

- SPI interface pin header (LVTTL levels) for debug and control of the IO-FPGA. This header also provides $I^2C$ interface to an ID PROM for the Raspberry Pi compute module 4.
- micro-USB connector for debug and control of the IO-FPGA. Additionally, eight GPIO pins within the USB-to-SPI converter are all connected to the IO-FPGA.
- JTAG and Programming header
- I/O probe

### 3.3.7 Raspberry Pi Compute Module 4 Interface Connector

The Raspberry Pi compute module 4 and associated connectors are placed together and highlighted on the PCB silkscreen, to indicate that these connectors may only be used together with the compute module, and not when the board is using the LAN9662 internal CPU.

Through the CM4 interface connector, the carrier board provides interfaces to LAN9662 PCIe 2.0 and SPI client, so the CM4 module can act as an external CPU system.

For the CM4 module itself, the carrier board provides support for the following interfaces:

- Two USB 2.0 host ports, J20
- Micro-USB 2.0 console port, J18
- Micro-SD connector, J17
- HDMI connector, J16
- Raspberry Pi HAT ID EEPROM
- Configuration header, J22
- Raspberry Pi activity by using a green LED, D39

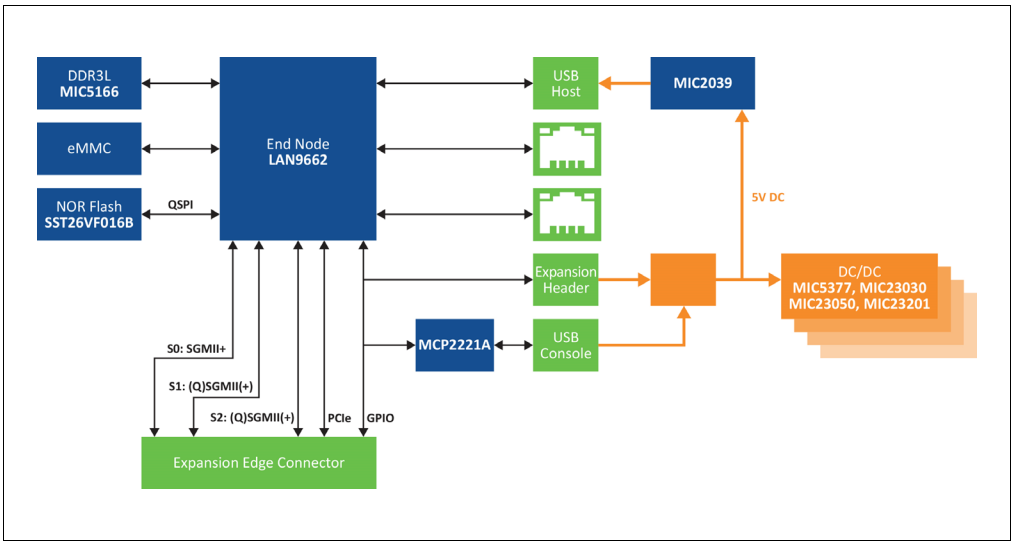
**NOTES:**

# Chapter 4. EVB-LAN9662 End-Node Hardware Details

## 4.1 BLOCK DIAGRAM

Figure 4-1 depicts the block diagram of the EVB-LAN9662 End-Node module with its two Ethernet copper front ports, USB ports and expansion connectors, all marked in green. DC/DC converters are marked red.

**FIGURE 4-1: EVB-LAN9662 END-NODE BLOCK DIAGRAM**




## 4.2 LAN9662 VCORE CPU SYSTEM

The design is based on the LAN9662 TSN switch, which includes a single core ARM Cortex A7 CPU, that externally connects to 1 GB SDRAM, 4 GB e-MMC and 2 MB NOR Flash memories. Both Flash memories can be used as second stage bootloader in a secure boot environment. The larger e-MMC is also used for bulk storage.

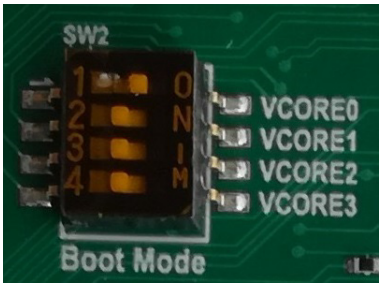
Optionally, an external CPU system can be connected and control the switch through its PCIe 2.0 endpoint interface and/or through an SPI client interface, both found in the (expansion) Edge header.

By default, the LAN9662 switch core is managed by its embedded CPU system with on-board SDRAM.

### 4.2.1 Boot Mode Strapping

LAN9662 uses strapping pins to select the initial boot mode. These pins are named **VCORE_CFG[3:0]** and located on **GPIO[65,42,41,40]**. A 4-pin DIP-switch, SW2 is used to make the actual strapping.

**FIGURE 4-2: 4-PIN DIP SWITCH, SW2**




When SW2 is set to '0001', the embedded CPU uses its QSPI0 boot interface connected to a NOR Flash device, as second bootloader in a secure boot environment. Setting SW2 to '0000', an e-MMC Flash device can be used. Both settings require the Flash device to be (pre-)programmed with a suitable bootloader.

**TABLE 4-1: BOOT MODES**

| SW2 | VCORE_CFG[3:0] Description |
|---|---|
| 0000 | Boot from e-MMC, boot traces on FLEXCOM 3b (default) |
| 0001 | Boot from QSPI0, boot traces on FLEXCOM 3b |
| 1000 | TF-A Monitor on FLEXCOM 3b |
| 0110 | Internal CPU is disabled. PCIe 2.0 endpoint is enabled. |
| 1111 | Internal CPU is disabled. SPI client (QSPI0) and MIIM client interfaces are enabled. |

Using an external CPU, SW2 can be set to either '0110' to enable the PCIe 2.0 endpoint controller found in the Edge connector, or to '1111' for register access through the SPI client or MIIM client interfaces, which are both found in the Expansion header.

### 4.2.2 PLL Strapping

LAN9662 PLL strapping, **PLL_STRP[1, 0]**, which is located on **GPIO[36, 27]**, is set to have 25 MHz on the switch core and internal Cu PHYs, and 25 MHz to the SerDes.

**TABLE 4-2: PLL STRAPPING MODES**

| Pulls | PLL_STRP[1:0] Description |
|---|---|
| 00 | SerDes: 25 MHz, Cu PHY: 25 MHz (default) |
| 01 | SerDes: 125 MHz, Cu PHY: 125 MHz |
| 10 | SerDes: 125 MHz, Cu PHY: 25 MHz |
| 11 | Reserved |

### 4.2.3 Reference Clocks

The end-node module has a local 25 MHz XTAL, VXM7-9013 as reference input, which provides all the necessary clocking for the end-node modules to function, both as standalone or together with the EVB-LAN9662-Carrier board.

However, the module is prepared for using an external 25 MHz reference clock to the switch core and internal Cu PHYs, and/or to use an external 125 MHz differential reference clock, like DSC1201 for the SerDes macros. Both reference clocks must then be provided through the Edge connector.

### 4.2.4 DDR3L SDRAM

The LAN9662 SDRAM interface is 16 bits wide and is targeted to operate at a clock rate of 600 MHz, requiring an SDRAM of speed grade 1200 MT/s or better.

The end-node module is equipped with one 800 MHz 1 GB DDR3L SDRAM (x16), IS46TR16512BL-125KBLA2, and has been tested up to 1325 MT/s. Lower densities can be substituted depending on the application. The minimum is 128 MB, and the maximum supported is 2 GB. The design is prepared for dual-rank devices, that is, CKE1, ODT1 and nCS1 are all connected on the DDR3L foot-print.

The reference design uses resistor dividers to generate the DDR_VREF, instead of using a dedicated DDR Power Manager device, like the MIC5166YML, as there is no need for driving DDR termination. DDR termination resistors can be avoided, when keeping the maximum trace length below 35 mm.

### 4.2.5 SPI NOR Flash Device

The reference board is equipped with a 2 MB NOR QSPI boot Flash device, SST26VF016B (8-pin SOIC), solely intended to hold a second stage bootloader in a secure boot environment. The NOR Flash device can be removed if only using e-MMC.

### 4.2.6 SPI NOR Flash Device Programming

The NOR Flash device can be programmed using an external Flash device programmer connected to the pins in the Expansion header, J2.

**Note:** The QSPI0 (boot) interface is daisy-chained to the NOR, then serial end-termination resistors, and then going to both Expansion headers.

To connect the Universal Programmer from ASIX (Forte or Presto), use the following connection diagram.

**TABLE 4-3: PROGRAMMING SIGNALS**

| Expansion Header | Description - Universal Programmer from ASIX |
|---|---|
| Pin 1 (VccSPI) | P3 (VDD) (Red) |
| Pin 35 (SI.D1) | P7 (DO/I) (White) |
| Pin 36 (SPI.nCS0) | P1 (P) (Yellow) |
| Pin 38 (SI.D0) | P5 (DI/D) (White) |
| Pin 39 (GND) | P4 (GND) (Blue) |
| Pin 40 (SI.CLK) | P6 (C) (Green) |

**Note:** The LAN9662 must not drive the SI_CLK and SI_D0 outputs, while programming the SPI Flash device. This is done by setting the LAN9662 boot mode to be an SPI client by setting SW2, DIP-switch to ‘1111’. See Table 4-1.

### 4.2.7 e-MMC Flash Device—Bulk Storage

The reference board is equipped with a 4 GB e-MMC, IS21ES04G-JQLI or equivalent for bulk storage.

The e-MMC can also be used as second stage boot ROM instead of the NOR Flash device, and hereby avoid having the NOR Flash device mounted. For production, it is then recommended to use a preprogrammed e-MMC device, or to have an additional test connector, like TC2050, being placed between LAN9662 and the e-MMC for on-board programming.

**Note:** Alternatively, setting the DIP switch, SW2, to '1000' enables TF-A monitor on the FLEXCOM 3b/UART interface, which can be used to 'bootstrap' the whole end-node module and control the programming of the on-board e-MMC and NOR Flash devices. Microchip can provide a browser-based update utility called `fwu.html`. (This can be found at https://github.com/microchip-ung/arm-trusted-firmware/releases.)

### 4.2.8 PCIe® 2.0 Endpoint

The LAN9662 implements a single-lane PCIe Gen2 endpoint controller that can be connected to any PCIe-capable system. The PCIe interface can be used by an external CPU to read or write switch registers.

**Note:** The LAN9662 has some frame-DMA capabilities, but the injection and extraction rates highly depend on the frame size as the major overhead is in setting up the DMA. The rule of thumb is that injection from the CPU queues is twice as fast as extraction to the CPU queues when using the internal CPU system. A powerful external CPU system can however easily make it opposite and much faster.

The PCIe 2.0 endpoint connection goes through the EVB-LAN9662 Edge connector to the external host system, which is located on EVB-LAN9662-Carrier Raspberry Pi compute module 4 connectors.

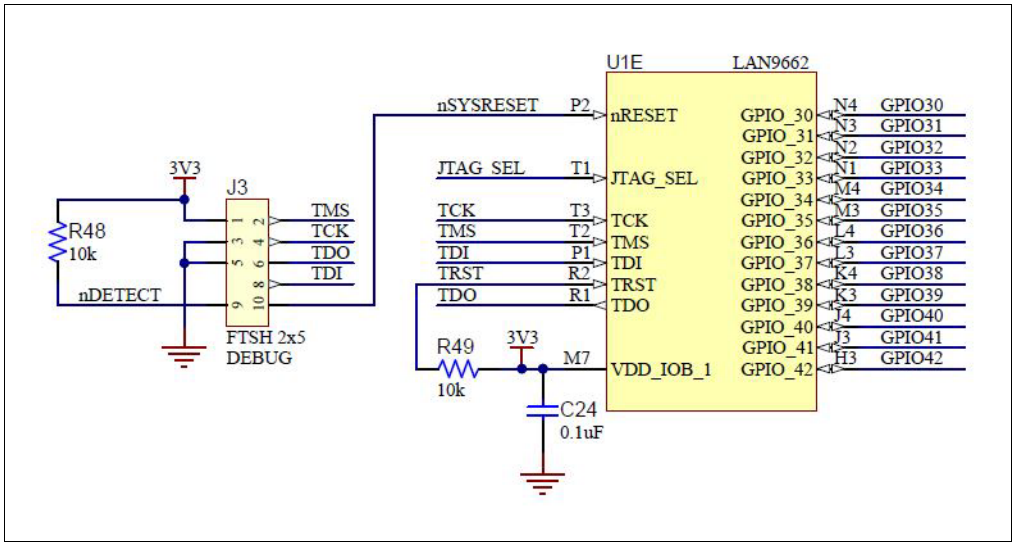
**Note:** The LAN9662 TX direction has AC coupling. It is expected that the PCIe host has a similar setup. Likewise, the received PCIe_CLK should be AC-coupled or biased to 0.6V.

An external PCIe reset signal to LAN9662 should be used, either by PCIe_PERST#_A/GPIO29 or by nSYSRESET. Using the latter may not comply to the PCIe reset timing.

### 4.2.9 ARM® CPU JTAG Connector

The end-node module offers a standard 10-pin (0.05") ARM CPU JTAG header, J3, to be used for boundary scan and In-Circuit Emulator (ICE). ICE can be used for debugging functions, such as downloading code and single-stepping through programs.

**FIGURE 4-3: JTAG HEADER**



The **JTAG_SEL** strapping input pin controls the mapping of the chip-level JTAG to select between the CPU subsystem TAP controller or the Test TAP controller. The on-board resistor setting is pulled up for CPU.

To connect a JTAG probe or ICE emulator, refer to Table 4-4 for the connections.

**TABLE 4-4: JTAG HEADER—PIN DESCRIPTIONS**

| Pin | JTAG | In/Out | Description |
|---|---|---|---|
| 1 | 3.3V | — | Power |
| 2 | TMS | VIS (PU) | Test mode select input |
| 3 | GND | — | Ground |
| 4 | TCK | VIS (PU) | Test clock input |
| 5 | GND | — | Ground |
| 6 | TDO | VO (PU) | Test data output |
| 7 | — | — | NC |
| 8 | TDI | VIS (PU) | Test data input |
| 9 | nDETECT | VIS (PU) | Voltage sense |
| 10 | nSYSRESET | VIS (PU) | HW reset |

**Note 1:** The JTAG signals are not 5V-tolerant. JTAG signal levels are determined by the VDD_IOB power supply pin, which is set to 3.3V on EVB-LAN9662. VDD_IOB can also be set to 1.8V or 2.5V.

## 4.3 ETHERNET PORTS

The LAN9662 has four logical Ethernet ports exposed on various interfaces. The LAN9662 end-node module exposes two internal Cu PHYs (ports 0 and 1) and two SerDes interfaces (ports 2 and 3).

**Note:** Only the LAN9668 can provide the third SerDes interface, which has been allocated in the Edge connector.

The 10/100/1000 Mbps Cu PHY ports are found on the end-node module itself.

The SerDes interfaces are found in the Edge connector and are intended to be used with SFP connections. The SerDes signals are therefore not AC-coupled to ensure Common-mode voltage compatibility, as this is mandatory for an SFP module.

### 4.3.1 PHY Copper Interface

The LAN9662 built-in, low-latency Cu PHYs integrate all passive components required to connect the PHYs' line-side interface to an external 1:1 transformer and Common-mode choke. This reduces the number of components in a design and greatly simplifies the layout of this interface.

The PHYs support auto-negotiation and downshift, and can automatically detect the speed of a link if auto-negotiation is disabled, and as a result provides the appropriate connection (called parallel detect).

The PHYs include Automatic Crossover Detection functionality for all speeds (HP Auto MDI/MDI- X™ function) and the ability to detect and correct polarity errors on all MDI pairs. These functions are normally enabled but can be disabled.

Instead of separate magnetic modules and RJ45 connectors, the reference board uses RJ45 connectors with integrated magnetics. This reduces the number of components on the board and the actual board area.

The PHYs support the IEEE standard range of 1m to 100m using twisted pair cabling, however:

- 1000BASE-T mode requires Category 5 enhanced cable in accordance to the cabling specifications as defined by IEEE802.3-2005.
- 100BASE-TX mode requires Category 5 cable and 10BASE-T requires Category 3 cable as specified in ISO/IEC 11801.

### 4.3.2 ICM—Integrated Magnetics

The end-node module uses a 1x2 RJ45 8P8C ICM with integrated LEDs.

| **Note:** | Using quality magnetics has significant influence on the EMI performance. |
|---|---|

### 4.3.3 MII-Management

LAN9662 serves the Cu PHYs over an internal MII-Management bus 1 interface.

### 4.3.4 Port LEDs Controlled Through Serial GPIO Engine

Port LEDs are automatically controlled by the LAN9662 using its serial GPIO interface. The serial GPIO engine is set up to provide two LEDs per port.

The conversion from a serial bit stream is made using an 8-bit Parallel-Out Serial Shift Register, SN74HC164. For LED control, the serial GPIO 'load' signal to hold the current state in the register is not used, as the human eye cannot detect the fast changes when the serial bit stream is being clocked through the shift registers.

Copper ports use a green LED to indicate 1G link and yellow LED for 10/100M. The SerDes ports use a green LED for 1G/2.5G link and blue LED for 100M. Solid ON means linkup, while blinking means traffic.

## 4.4 MICRO-USB CONSOLE PORT

Local management and software debugging is supported by using a micro-USB 2.0 type-B female connector, J6 connected to LAN9662 UART interface (FLEXCOM 3b) through an USB-to-UART Serial Converter, MCP2221A.

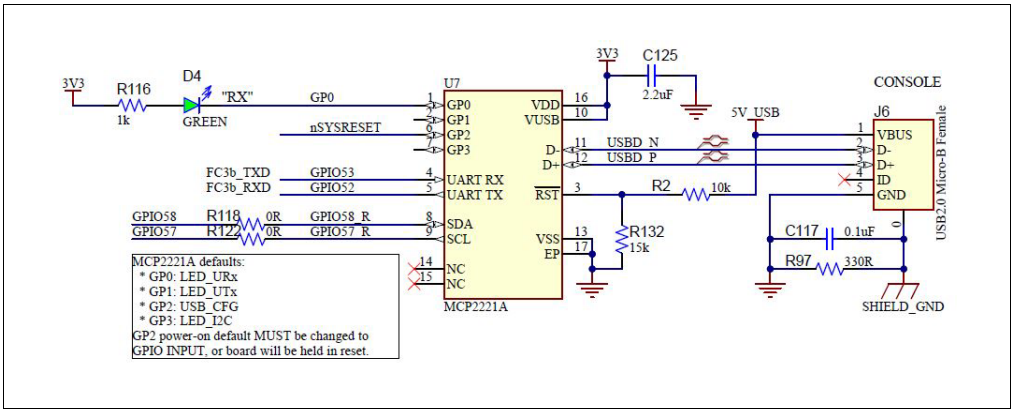
The MCP2221A also offers an $I^2C$ host interface. However, there are no current plans to use this interface. It is a shared connection to the Edge connector and Expansion header, shared with the LAN9662 $I^2C$ host interface (FLEXCOM 4b), but the MCP2221A does not support 'multiple masters' mode. The LAN9662 $I^2C$ host (FLEXCOM 4b) is used to read out the MSA PROM content in SFP modules attached to the carrier board for auto-detection purposes.

The MCP2221A default GP settings display the activity on UART Rx, UART Tx and $I^2C$ data. GP0/UART Rx is connected to a green LED (D4) for this purpose. GP2 provides a remote controlled 'system reset' to the end-node module and the carrier board.

| **Note:** | It is important to program the MCP2221A during board bring-up, so that GP2 is changed from the default output mode to an input. Otherwise, the EVB-LAN9662 will be in held in reset. |
|---|---|

Figure 4-4 outlines the micro-USB console port on the end-node module.

**FIGURE 4-4: MICRO-USB CONSOLE PORT USING MCP2221A UART**

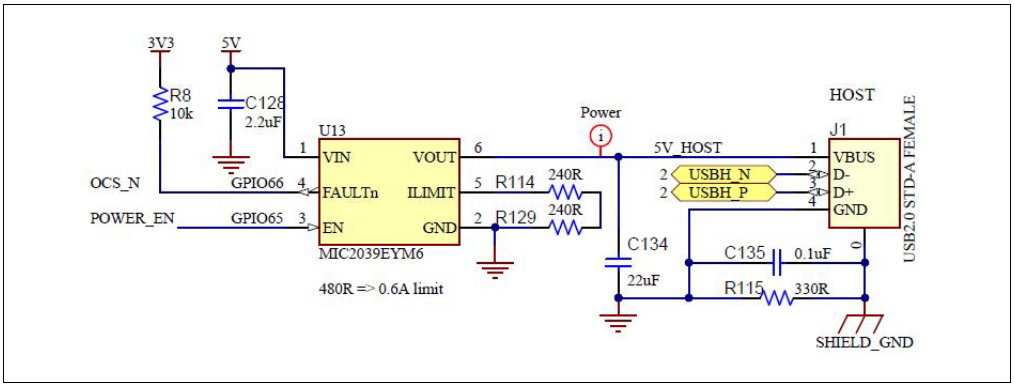



## 4.5 USB 2.0 HOST PORT

USB 2.0 Host mode is supported by using a USB 2.0 female type-A connector, which exposes the local USB 2.0 port in the LAN9662.

The USB host port is current limited to 600 mA by using a MIC2039EYM6 USB power switch driver.

**FIGURE 4-5: USB 2.0 HOST PORT**



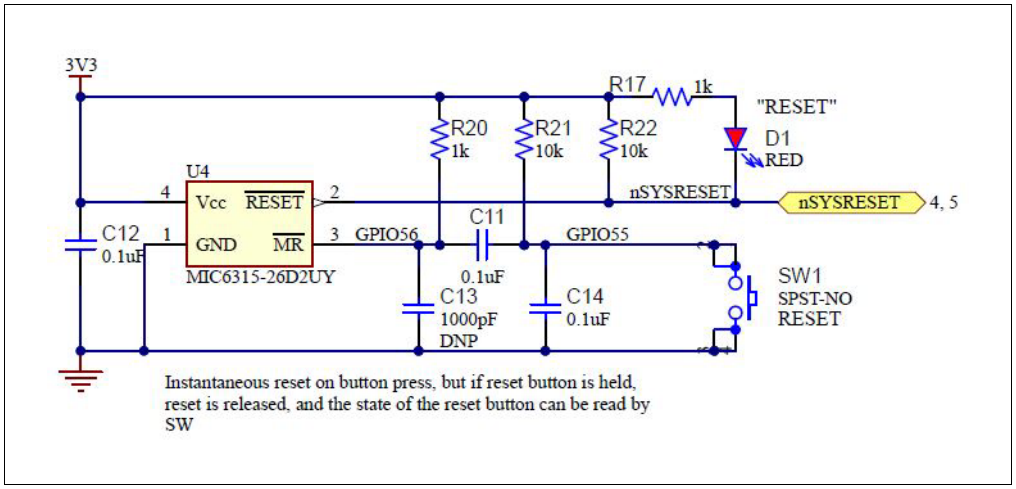

The LAN9662 controls the Host-mode signals: power enable—POWER_EN (GPIO65/VCORE_CFG4) and overcurrent status—OCS_N (GPIO66).

## 4.6 RESET AND RESET BUTTON

A voltage supervisor, MIC6315-26D2UY, is used to hold the end-node module (and the carrier board) in Reset state until all supplies are up. The MIC6315 monitors the 3.3V supply, as it is the last in the power sequence. The MIC6315 also provides a manual reset (nMR) input, which is connected to a reset button, SW1. (The nMR input signal also goes to the LAN9662 GPIO56.)

The MIC6315 generates the overall board reset signal, nSYSRESET. A red LED, D1, is controlled by this output signal and is used to indicate the Reset state.

**FIGURE 4-6: RESET AND POWER MONITORING**




The reset button is available at the front of the end-node module. Reset functions as a one-shot, so pressing it causes a low-reset pulse to the MR input. However, it can then be sampled (through GPIO55) by firmware to determine if it is still being pressed during boot-up, and as a result initiating a 'reset to factory defaults'.

## 4.7 POWER SUPPLY

A power source switch circuitry controls whether the 5V from the micro-USB port or 5V from one of the two connectors is being used. That is, when the 5V supply from the connector is higher than the 5V_USB supply, the 5V_USB supply is disconnected. On-board DC/DC converters then supply the different voltages needed.

### 4.7.1 DC/DC Converters

The end-node module generates the following power supplies (worst-case currents):

- 1.10V at 1.4A use MIC23201 2A buck regulator. Powers LAN9662.
- 1.35V at 0.4A use MIC23030 0.4A buck regulator. Powers LAN9662 DDR interface (175 mA), RAM (220 mA).
- 3.30V at 0.6A use MIC23050 0.6A buck regulator. Powers LAN9662 I/O (0.1A/0.3A), miscellaneous (0.3A).
- 2.50V at 0.05A use MIC5377 linear regulator. Powers DDR interface PLL (40 mA).

A single green LED (D5) indicates power-on using the 3.3V supply.

### 4.7.2 Power Supply Sequencing

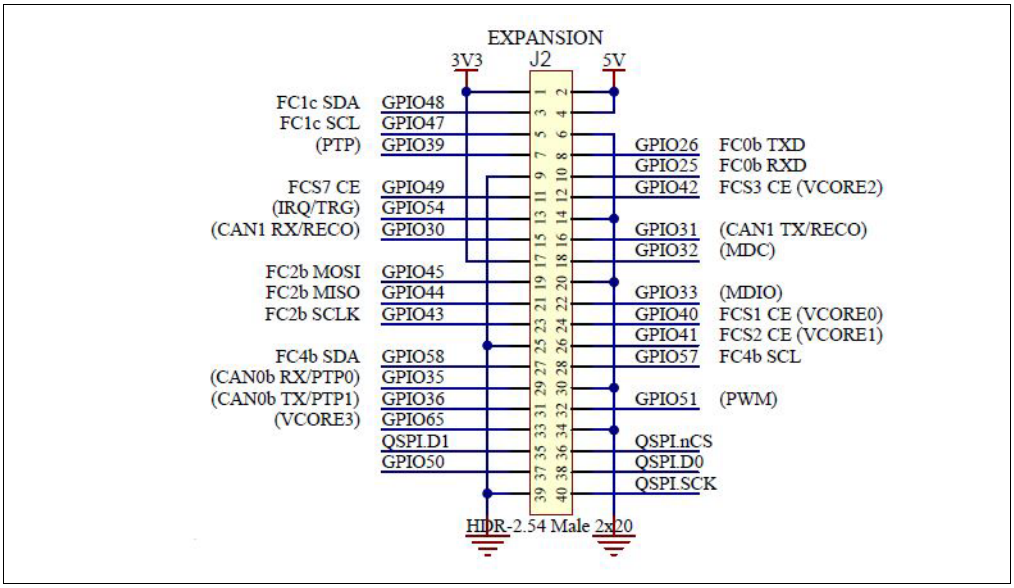
The overall strategy for the switch power supply sequencing is to prevent higher-level power supply to feed through lower-level power grids through the internal protection diode network. The general power sequence is:

1V1 → 1V35/3V3

## 4.8 EXPANSION HEADER

The Expansion header, J2, is a 2x20, 0.1" pin connector and targets Raspberry Pi compatibility. It can be used for programming the NOR Flash device or give an external CPU control over the SPI client register interface, and exposes various LAN9662 GPIO signals in Alternate mode.

**FIGURE 4-7: EXPANSION HEADER LAYOUT**




**Note:** An add-on board using the Expansion header, *must* have its own Power-On-Reset (POR), and ensure that the strapping settings are not overridden unintentionally: GPIO 36, 40, 41, 42 and 65 (marked green in Table 4-5). Likewise, the overall power consumption should be considered.

The I/O functionality, which is not compatible with Raspberry Pi, is marked in gray in Table 4-5. For these, the GPIO signals function as normal GPIO pins when using default software settings.

**TABLE 4-5: EXPANSION HEADER—PIN DESCRIPTIONS**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 1 | 3V3 | VccSPI | 2 | 5V | — |
| 3 | GPIO 48 | $I^2C$ SDA (FC1c) | 4 | 5V | — |
| 5 | GPIO 47 | $I^2C$ SCL (FC1c) | 6 | GND | — |
| 7 | GPIO 39 | (PTP4_IN) | 8 | GPIO 26 | UART TX (FC0b) |
| 9 | GND | — | 10 | GPIO 25 | UART RX (FC0b) |
| 11 | GPIO 49 | CE (FCS7) | 12 | GPIO 42 | CE (FCS3) (VCORE_CFG2) |
| 13 | GPIO 54 | (IRQ3 or TRG3_C) | 14 | GND | — |
| 15 | GPIO 30 | (CAN1_Rx) | 16 | GPIO 31 | (CAN1_Tx) |
| 17 | 3V3 | — | 18 | GPIO 32 | (~~MDC_B~~) |
| 19 | GPIO 45 | MOSI (FC2b) | 20 | GND | — |
| 21 | GPIO 44 | MISO (FC2b) | 22 | GPIO 33 | (~~MDIO_B~~) |
| 23 | GPIO 43 | SCLK (FC2b) | 24 | GPIO 40 | CE (FCS1) (VCORE_CFG0) |
| 25 | GND | — | 26 | GPIO 41 | CE (FCS2) (VCORE_CFG1) |
| 27 | GPIO 58 | $I^2C$ SDA (FC4b) | 28 | GPIO 57 | $I^2C$ SCL (FC4b) |
| 29 | GPIO 35 | (CAN0b Rx/PTP0 IN) | 30 | GND | — |
| 31 | GPIO 36 | (CAN0b Tx/PTP1 OUT) (PLL1) | 32 | GPIO 51 | (PWM_B) |
| 33 | GPIO 65 | (VCORE_CFG3) | 34 | GND | — |

**TABLE 4-5: EXPANSION HEADER—PIN DESCRIPTIONS (CONTINUED)**

| Pin | Signal | Description | Pin | Signal | Description |
|---|---|---|---|---|---|
| 35 | QSPI.D1 | SPI.D1 | 36 | QSPI.nCS0 | SPI.nCS0 LAN9662 |
| 37 | GPIO 50 | SPI.nCS NOR Flash device | 38 | QSPI.D0 | SPI.D0 |
| 39 | GND | — | 40 | QSPI.CLK | SPI.CLK |

**Note 1:** FC = FLEXCOM, FCS = FLEXCOM Shared

**2:** Although the schematic shows the MDC_B/MDIO_B signals in the Expansion header, they are not currently available because the serial GPIO0 uses the same GPIO pins.

## 4.9 EDGE CONNECTOR

The EVB-LAN9662 End-Node module is the male part of a 260-pin, high-speed SO-DIMM socket on the EVB-LAN9662-Carrier board.

The Edge connector exposes most I/O pins on the LAN9662. Table 4-6 shows the placement in the Edge connector. Strapping pins are marked in green, power is marked in orange and ground in gray.

**TABLE 4-6: SO-DIMM (EDGE) CONNECTOR**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | GND | 45 | GPIO7 | 89 | GND | 133 | S1.TX_N | 177 | RSVD | 221 | RSVD |
| 2 | GND | 46 | GPIO9 | 90 | GND | 134 | ~~(S4.TX_N)~~ | 178 | GPIO51 | 222 | GND |
| 3 | GPIO24 | 47 | GND | 91 | GPIO30 | 135 | GND | 179 | RSVD | 223 | GND |
| 4 | GPIO34 | 48 | GND | 92 | GPIO31 | 136 | GND | 180 | GND | 224 | GPIO68 |
| 5 | GND | 49 | GPIO4 | 93 | GND | 137 | S1.RX_p | 181 | GND | 225 | GPIO73 |
| 6 | GND | 50 | GPIO10 | 94 | GND | 138 | ~~(S4.RX_N)~~ | 182 | GPIO52* | 226 | GND |
| 7 | GPIO20 | 51 | GND | 95 | RSVD | 139 | S1.RX_N | 183 | GPIO53* | 227 | GND |
| 8 | GPIO29 | 52 | GND | 96 | GPIO32 | 140 | ~~(S4.RX_P)~~ | 184 | GND | 228 | GPIO74 |
| 9 | GND | 53 | RSVD | 97 | RSVD | 141 | GND | 185 | GND | 229 | GPIO76 |
| 10 | GND | 54 | GPIO5 | 98 | GND | 142 | GND | 186 | GPIO36 | 230 | GND |
| 11 | RSVD | 55 | RSVD | 99 | GND | 143 | RSVD | 187 | GPIO55 | 231 | GND |
| 12 | GPIO27 | 56 | GND | 100 | GPIO45 | 144 | RSVD | 188 | GND | 232 | GPIO75 |
| 13 | RSVD | 57 | GND | 101 | GPIO44 | 145 | RSVD | 189 | GND | 233 | GPIO77 |
| 14 | GND | 58 | GPIO6 | 102 | GND | 146 | RSVD | 190 | GPIO56 | 234 | GND |
| 15 | GND | 59 | GPIO3 | 103 | GND | 147 | GND | 191 | GPIO59 | 235 | GND |
| 16 | GPIO21 | 60 | GND | 104 | nSYSRESET | 148 | GND | 192 | GND | 236 | RSVD |
| 17 | GPIO23 | 61 | GND | 105 | SGPIO_DO | 149 | PCIE.TX_P | 193 | GND | 237 | QSPI.D0 |
| 18 | GND | 62 | GPIO1 | 106 | GND | 150 | ~~(S5.TX_P)~~ | 194 | GPIO60 | 238 | GND |
| 19 | GND | 63 | GPIO37 | 107 | GND | 151 | PCIE.TX_N | 195 | GPIO61 | 239 | GND |
| 20 | GPIO22 | 64 | GND | 108 | S2.TX_P | 152 | ~~(S5.TX_N)~~ | 196 | GND | 240 | RSVD |
| 21 | GPIO19 | 65 | GND | 109 | CKM_25 | 153 | GND | 197 | GND | 241 | QSPI.D1 |
| 22 | GND | 66 | GPIO2 | 110 | S2.TX_N | 154 | GND | 198 | PCIE_CLK_P | 242 | RSVD |
| 23 | GND | 67 | GPIO28 | 111 | GND | 155 | PCIE.RX_P | 199 | GPIO62 | 243 | GND |
| 24 | GPIO17 | 68 | GND | 112 | GND | 156 | ~~(S5.RX_N)~~ | 200 | PCIE_CLK_N | 244 | GND |
| 25 | GPIO16 | 69 | GND | 113 | CKM_125_P | 157 | PCIE.RX_N | 201 | GND | 245 | QSPI.D2 |
| 26 | GND | 70 | GPIO0 | 114 | S2.RX_P | 158 | ~~(S5.RX_P)~~ | 202 | GND | 246 | QSPI.SCK |
| 27 | GND | 71 | GPIO48 | 115 | CKM_125_N | 159 | GND | 203 | GPIO63 | 247 | GND |
| 28 | GPIO18 | 72 | GND | 116 | S2.RX_N | 160 | GND | 204 | GPIO71 | 248 | GND |
| 29 | GPIO15 | 73 | GND | 117 | GND | 161 | GPIO43 | 205 | GND | 249 | QSPI.D3 |
| 30 | GND | 74 | RSVD | 118 | GND | 162 | GPIO33 | 206 | GND | 250 | QSPI.nCS |
| 31 | GND | 75 | GPIO47 | 119 | S0.TX_P | 163 | GND | 207 | GPIO65 | 251 | GND |
| 32 | RSVD | 76 | RSVD | 120 | ~~(S3.TX_P)~~ | 164 | GND | 208 | GPIO66 | 252 | GND |
| 33 | GPIO12 | 77 | GND | 121 | S0.TX_N | 165 | GPIO40 | 209 | GND | 253 | GPIO57 |
| 34 | RSVD | 78 | GND | 122 | ~~(S3.TX_N)~~ | 166 | GPIO46 | 210 | GND | 254 | GPIO58 |
| 35 | GND | 79 | GPIO26 | 123 | GND | 167 | GND | 211 | GPIO69 | 255 | 5V |
| 36 | GND | 80 | GPIO39 | 124 | GND | 168 | GND | 212 | GPIO72 | 256 | 5V |
| 37 | GPIO11 | 81 | GND | 125 | S0.RX_P | 169 | GPIO41 | 213 | GND | 257 | 5V |
| 38 | GPIO13 | 82 | GND | 126 | ~~(S3.RX_N)~~ | 170 | GPIO64 | 214 | GND | 258 | 5V |
| 39 | GND | 83 | GPIO42 | 127 | S0.RX_N | 171 | GND | 215 | GPIO67 | 259 | 5V |
| 40 | GND | 84 | GPIO25 | 128 | ~~(S3.RX_P)~~ | 172 | GND | 216 | GPIO70 | 260 | 5V |
| 41 | GPIO8 | 85 | GND | 129 | GND | 173 | GPIO38 | 217 | GND | — | — |
| 42 | GPIO14 | 86 | GND | 130 | GND | 174 | GPIO35 | 218 | GND | — | — |
| 43 | GND | 87 | GPIO54 | 131 | S1.TX_P | 175 | GND | 219 | RSVD | — | — |
| 44 | GND | 88 | GPIO49 | 132 | ~~(S4.TX_P)~~ | 176 | GND | 220 | GPIO50 | — | — |

**Note 1:** Although the schematic shows the S3 SerDes pins, they are only available when using LAN9668. Likewise, S4 and S5 SerDes pins have been allocated in the connector for future products.

### 4.9.1 GPIO Usage Overview

Each GPIO pin in the LAN9662 can be assigned to one of up to eight functions. The following tables show which GPIOs and functionality have been used in the EVB-LAN9662 End-Node design. Strapping pins are marked in green.

**TABLE 4-7: GPIO USAGE—PI INTERFACE**

| GPIO | Alt Mode | Connected To | Board | Function |
|---|---|---|---|---|
| 0 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD0 |
| 1 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD |
| 2 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD2 |
| 3 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD3 |
| 4 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD4 |
| 5 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD5 |
| 6 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD6 |
| 7 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD7 |
| 8 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD8 |
| 9 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD9 |
| 10 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD10 |
| 11 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD11 |
| 12 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD12 |
| 13 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD13 |
| 14 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD14 |
| 15 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_AD15 |
| 16 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR0 |
| 17 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR1 |
| 18 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR2 |
| 19 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR3 |
| 20 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR4 |
| 21 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR5 |
| 22 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ADDR6 |
| 23 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ALH |
| 24 | PI | IO-FPGA | EVB-LAN9662-Carrier | PI_ALL |
| 25 | PI (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PI_RD (FB0b - RxD) |
| 26 | PI (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PI_WR (FC0b - TxD) |

**TABLE 4-8: GPIO USAGE—SGPIO AND CAN1 INTERFACE**

| GPIO | Alt Mode | Connected To | Board | Function |
|---|---|---|---|---|
| 27 | 4 | IO-FPGA | EVB-LAN9662-Carrier | OB_TRIG_11 (PLL_STRP0) |
| 28 | 4 | IO-FPGA | EVB-LAN9662-Carrier | OB_TRIG_12 |
| 29 | 4 (2) | IO-FPGA | EVB-LAN9662-Carrier | OB_TRIG_13 (PCIE_nRST) |
| 30 | 2 | CAN | EVB-LAN9662-Carrier/Exp.header | CAN1_RX |
| 31 | 2 | CAN | EVB-LAN9662-Carrier/Exp.header | CAN1_TX |
| 32 | 3 (6) | SFP control | EVB-LAN9662-Carrier/Exp.header | SGPO_SCK (MDC_B) |
| 33 | 3 (6) | SFP control | EVB-LAN9662-Carrier/Exp.header | SGPO_DO (MDIO_B) |
| 34 | 3 | SFP control | EVB-LAN9662-Carrier | SGPIO_DI |
| 35 | 3 (4) | SFP control | EVB-LAN9662-Carrier/Exp.header | SGPO_LD (CAN0b_RX) |
| 36 | 2 (4) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PTPSYNC_1 (STRAP_PLL1) (CAN0b_TX) |
| 37 | 2 | IO-FPGA | EVB-LAN9662-Carrier | PTPSYNC_2 (STRAP_JTAG0) |
| 38 | 2 | 1PPS out SMA | EVB-LAN9662-Carrier | PTPSYNC_3 (STRAP_JTAG1) |
| 39 | 2 | 1PPS in SMA | EVB-LAN9662-Carrier/Exp.header | PTPSYNC_4 (PTP4_IN) |

**TABLE 4-9: GPIO USAGE—VARIOUS INTERFACES**

| GPIO | Alt Mode | Connected To | Board | Function |
|---|---|---|---|---|
| 40 | 2 (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PTPSYNC_5 (STRAP_VCORE0) (FCS1) |
| 41 | 2 (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PTPSYNC_6 (STRAP_VCORE1) (FCS2) |
| 42 | 2 (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | PTPSYNC_7 (STRAP_VCORE2) (FCS3) |
| 43 | 1 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | FC2b_SCK – SPI.SCLK |
| 44 | 1 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | FC2b_RXD – SPI.MISO |
| 45 | 1 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | FC2b_TXD – SPI.MOSI |
| 46 | 3 (5) | IO-FPGA | EVB-LAN9662-Carrier | IB_TRIG_3 (FCS4 – SPI.nCS) |
| 47 | 3 (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | IB_TRIG_4 (FC1c – I2C.SCL) |
| 48 | 3 (1) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | IB_TRIG_5 (FC1c – I2C.SDA) |
| 49 | 1 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | FCS7 |
| 50 | 0 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | GPIO50 |

**TABLE 4-9: GPIO USAGE—VARIOUS INTERFACES (CONTINUED)**

| GPIO | Alt Mode | Connected To | Board | Function |
|---|---|---|---|---|
| 51 | 5 | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | (PWM) |
| 52 | 1 | m-USB UART | EVB-LAN9662 End-Node | FC3b_RXD - |
| 53 | 1 | m-USB UART | EVB-LAN9662 End-Node | FC3b_TXD |
| 54 | 0 (4,6/3) | IO-FPGA | EVB-LAN9662-Carrier/Exp.header | CAN STBY (IRQ3/TRG3_C) |
| 55 | | IO-FPGA | EVB-LAN9662 End-Node | nBUTTON |
| 56 | | IO-FPGA | EVB-LAN9662 End-Node | nMR |
| 57 | 1 | SFP module | EVB-LAN9662-Carrier/Exp.header | FC4b_RXD – I2C.SCL to SFP module |
| 58 | 1 | SFP module | EVB-LAN9662-Carrier/Exp.header | FC4b_TXD – I2C.SDA to SFP module |
| 59 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_SCK |
| 60 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_nCS |
| 61 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_DAT0 |
| 62 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_DAT1 |
| 63 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_DAT2 |
| 64 | 1 | IO-FPGA | EVB-LAN9662-Carrier | QSPI1_DAT3 |
| 65 | 1 | USB-A control | EVB-LAN9662-Carrier/Exp.header | USB_POWER_EN (STRAP_VCORE3) |
| 66 | 1 | USB-A control | EVB-LAN9662 End-Node | USB_OCS_N |

**TABLE 4-10: GPIO USAGE—E-MMC INTERFACE**

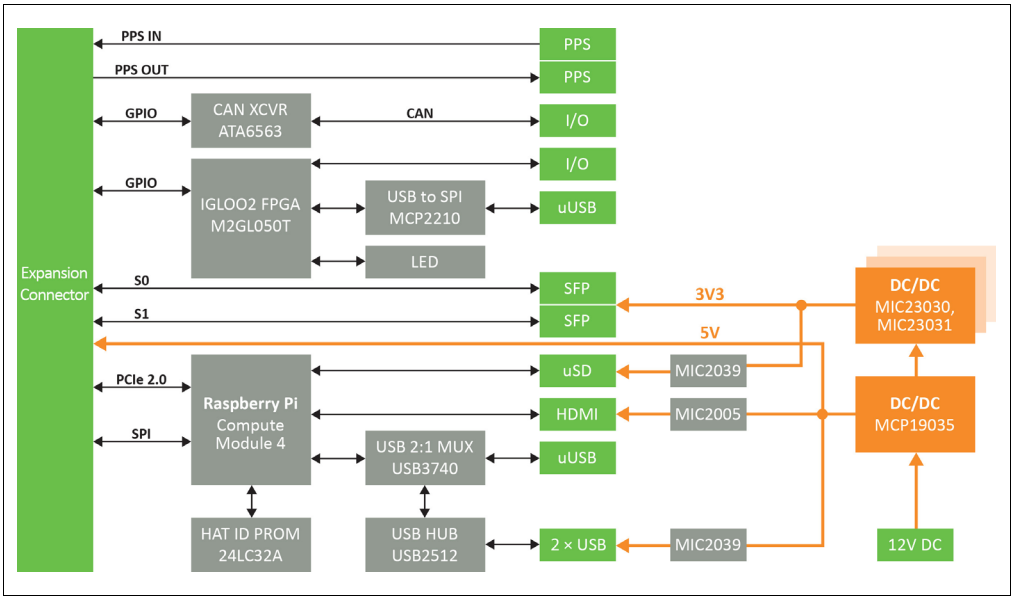
| GPIO | Alt Mode | Connected To | Board | Function |
|---|---|---|---|---|
| 67 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD CMD (QSPI2_nCS) |
| 68 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD CLK (QSPI2_SCK) |
| 69 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD D0 (QSPI2_-DATA0) |
| 70 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD D1 (QSPI2_-DATA1) |
| 71 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD D2 (QSPI2_-DATA2) |
| 72 | 1 (3) | e-MMC | EVB-LAN9662 End-Node | e-MMC/SD D3 (QSPI2_-DATA3) |
| 73 | 1 (4) | e-MMC | EVB-LAN9662 End-Node | e-MMC D4 (SD VSEL) |
| 74 | 1 (4) | e-MMC | EVB-LAN9662 End-Node | e-MMC D5 (SD WP) |
| 75 | 1 (4) | e-MMC | EVB-LAN9662 End-Node | e-MMC D6 (SD CD) |
| 76 | 1 (4) | e-MMC | EVB-LAN9662 End-Node | e-MMC D7 (SD LED - unused) |
| 77 | 1 | e-MMC | EVB-LAN9662 End-Node | e-MMC RSTN |

# Chapter 5. EVB-LAN9662-Carrier Hardware Details

## 5.1 BLOCK DIAGRAM

The EVB-LAN9662-Carrier board is intended to expand the functionality of the EVB-LAN9662 End-Node module. Figure 5-1 depicts the block diagram of the EVB-LAN9662-Carrier board with its various I/O interfaces (marked in green) and DC/DC converters (marked in red). To support the different I/O interfaces and LAN9662 RTE functionality, additional devices (in gray) have been added.

**FIGURE 5-1: EVB-LAN9662-CARRIER BLOCK DIAGRAM**




## 5.2 260-PIN SO-DIMM CONNECTOR

The various interfaces found in the SO-DIMM connector are already described in **Section 3.2.10 "Edge Connector"** and their placement in the connector itself in **Section 4.9 "Edge Connector"**.

Currently, both the parallel interface (PI) and QSPI1 interfaces are connected to the IO-FPGA. The PI provides maximum bandwidth but takes up many signals. The QSPI1 interface is enough for most applications. So, the IO-FPGA code currently only support QSPI1.

| **Note:** | If the PI interface is *not* used for the IO-FPGA, then FLEXCOM 0b or CAN 0a can be used. The same goes for the two RGMII interface. |
|---|---|

Likewise, FLEXCOM 2b is exposed in the SO-DIMM connector and goes only to the IO-FPGA, but it is currently unused. However, FLEXCOM 2b is also exposed in EVB-LAN9662 End-Node Expansion header as an SPI interface.

## 5.3 SFP CONNECTORS SUPPORTED THROUGH THE SERIAL GPIO

The carrier board provides two SFP slots, J2 and J6, for the LAN9662 SerDes ports (S0 and S1) coming to the carrier board through the SO-DIMM connector.

To support the SFP-MSA-defined signals, the serial GPIO interface is used. The serial GPIO is configured with two bits per SGPIO port. In this mode, device 0-3 maps to SGPIO ports 0-3.

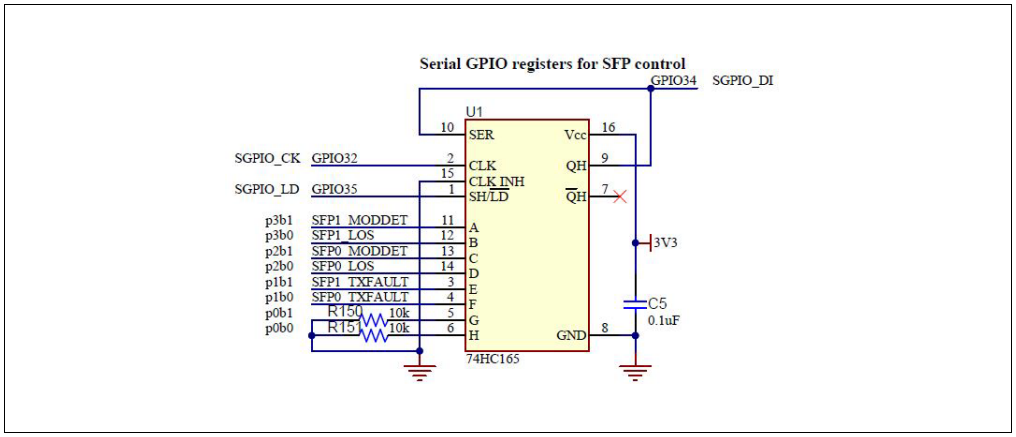
### 5.3.1 Serial GPIO Input

The serial GPIO is used to interface with each SFP module MSA-defined input signal.

- Input SGPIO port 0: Not used – spare inputs
- Input SGPIO port 1: SFP0 and SFP1 TX_Fault
- Input SGPIO port 2: SFP0 loss-of-signal and module detect
- Input SGPIO port 3: SFP1 loss-of-signal and module detect

**Note:** To fulfill the serial GPIO requirement of having the same length on both input and output serial bit streams, the input is looped-back to 74HC165, hereby simply repeating the pattern.

**FIGURE 5-2: SERIAL GPIO INPUT**



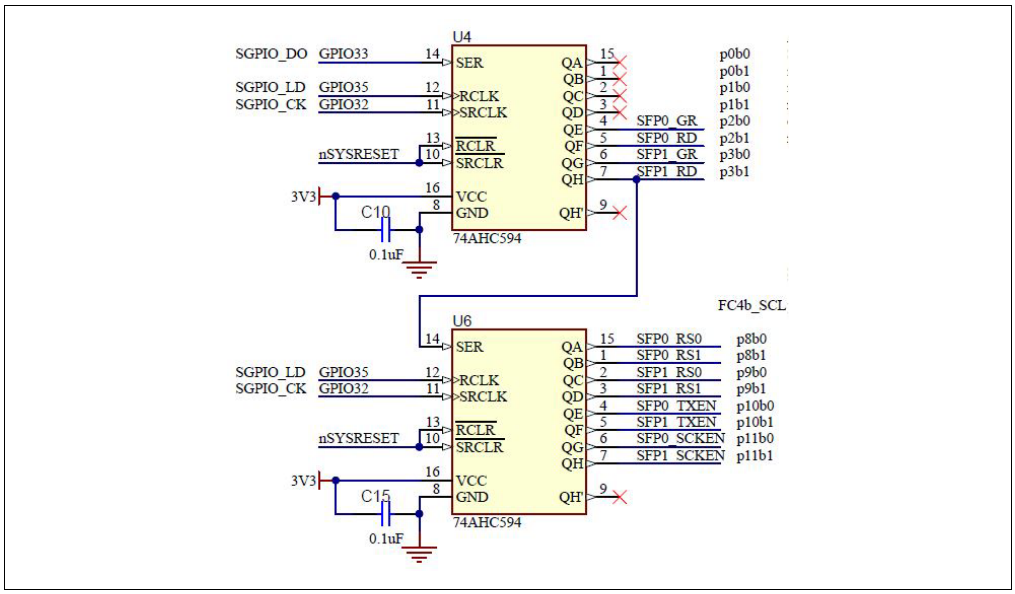

### 5.3.2 Serial GPIO Output

For the output:

- Output SGPIO ports 0-1: (EVB-LAN9662 End-Node copper ports P0 and P1 LEDs b0 and b1)
- Output SGPIO ports 2: SFP0 control of green and red LEDs
- Output SGPIO ports 3: SFP1 control of green and red LEDs
- Output SGPIO ports 4-7: Unused/disabled
- Output SGPIO ports 8: SFP0 Rate – Select 0 and 1
- Output SGPIO ports 9: SFP1 Rate – Select 0 and 1
- Output SGPIO port 10: SFP0 and SFP1 Tx_Enable
- Output SGPIO port 11: SFP0 and SFP1 $I^2C$ clock select

The $I^2C$ clock select enables reading from each SFP module. LAN9662 FLEXCOM 4b port is used to provide the $I^2C$ SCL and SDA signals to the two SFP slots. Figure 5-3 shows how 74AHC594 is using the load signal to hold the output state.

**FIGURE 5-3: SERIAL GPIO OUTPUT**




**Note:** The first 8-bit shift register has been replicated on EVB-LAN9662 End-Node module for local port LED support.

Each Tx_Enable signal is inverted before use on the SFP module, as the 74HC594 resets output signals to low, and the SFP TX_DISABLE input is active high. This means an inverting buffer is required to output disable SFPs during Reset state.

## 5.4 SMA CONNECTORS AT REAR

The carrier board provides two SMA connectors for PTP applications. One is used as 1PPS output, J4, and the other as 1PPS input, J3.

The SMA output is connected to the LAN9662 PTP3 engine. The output uses LVTTL levels. The SMA input is connected to LAN9662 PTP4 engine. The input is LVTTL and 3V3-tolerant. It is not 5V-tolerant.

Both SMA connectors are circuit-protected by using BAS70-04 voltage clamping diodes.

## 5.5 CAN BUS INTERFACE

The carrier board provides a 10-pin header, J5, to access the two-wire CAN1 BUS interface.

**TABLE 5-1: CAN BUS HEADER DESCRIPTION**

| Pin | Signal | In/Out | Description |
|---|---|---|---|
| 1 | — | — | NC |
| 2 | GND | — | Ground |
| 3 | CAN_L | I/O | Low-level CAN bus line. |
| 4 | CAN_H | I/O | High-level CAN bus line. |
| 5 | GND | — | Ground |

**Note 1:** Absolute Maximum Ratings (†)
DC Voltage at CANH, CANL (VCANH, VCANL): –27 to +42V
Transient Voltage at CANH, CANL (acc. to ISO 7637 part 2) (VCANH, VCANL): –150 to +100V
Max. Differential Bus Voltage (VDiff): –5 to +18V

**TABLE 5-1: CAN BUS HEADER DESCRIPTION (CONTINUED)**

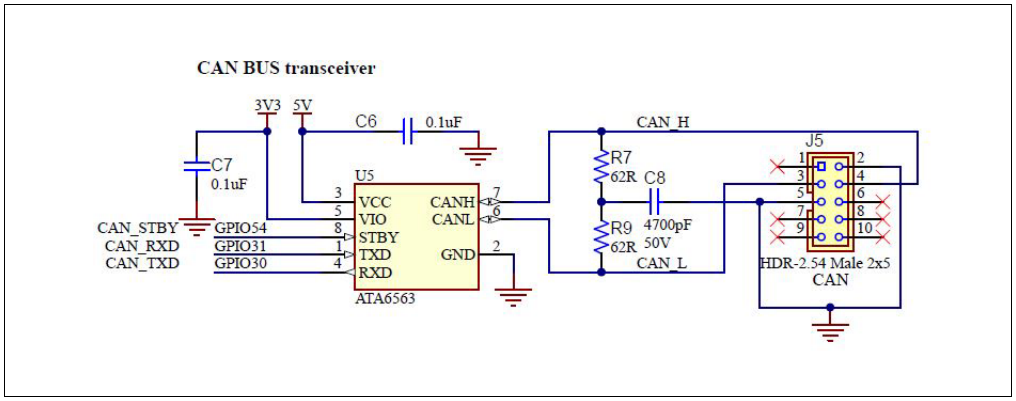
| Pin | Signal | In/Out | Description |
|---|---|---|---|
| 6 | — | — | NC |
| 7 | — | — | NC |
| 8 | — | — | NC |
| 9 | — | — | NC |
| 10 | — | — | NC |

**Note 1:** Absolute Maximum Ratings (†)
DC Voltage at CANH, CANL (VCANH, VCANL): –27 to +42V
Transient Voltage at CANH, CANL (acc. to ISO 7637 part 2) (VCANH, VCANL): –150 to +100V
Max. Differential Bus Voltage (VDiff): –5 to +18V

Power is not provided in the header.

The ATA6563 CAN BUS transceiver used is connected to the LAN9662 CAN1 interface.

**FIGURE 5-4: CAN BUS TRANSCEIVER**




## 5.6 IO-FPGA FOR RTE SUPPORT

The IO-FPGA is implemented in an IGLOO2 M2GL050T and is intended to provide digital I/O ports for Profinet/OPC-UA end-node applications.

All LAN9662 GPIO pins are connected to the IO-FPGA over the SO-DIMM connector. The LAN9662 RTE features can be explored by using the RTE-associated QSPI1 and parallel interfaces to control the various IO-FPGA functions.

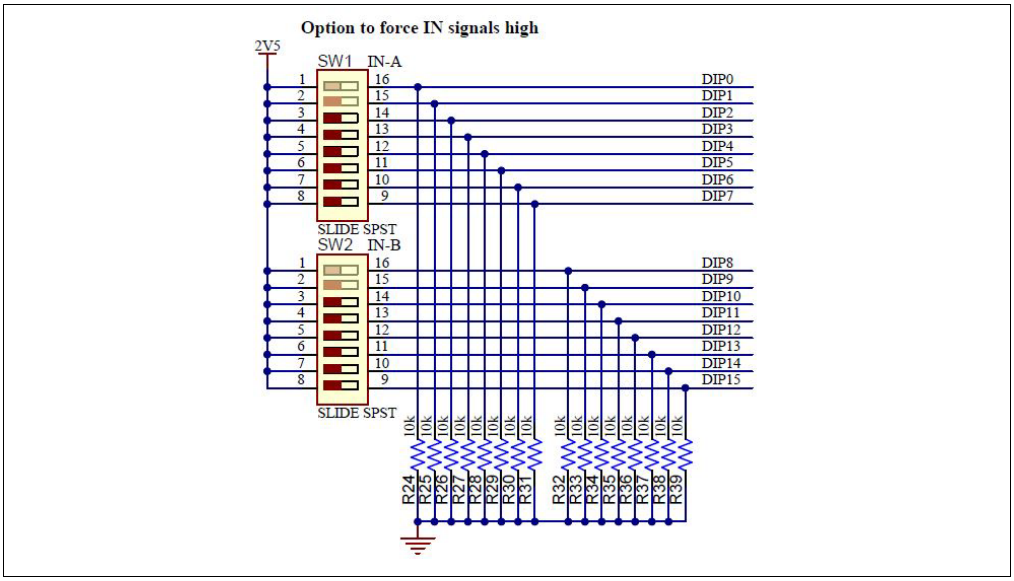
### 5.6.1 IO-FPGA Digital Inputs and Outputs with Status LEDs

The IO-FPGA provides 16 digital outputs in two 2x8-pin headers, J10 and J11. Likewise, it provides 16 digital inputs in two 2x8-pin headers, J13 and J14.

An individual green status LED is generated for each of these I/Os, D5-D36. There are two extra LEDs (green and yellow) that are used for additional IO-FPGA status indication, D37-D38.

For optional use and debug, there are two 8-pin DIP switches, SW1 and SW2, to force inputs high.

**FIGURE 5-5: DIP SWITCHES FOR FORCING INPUTS HIGH**




### 5.6.2 User Button Input to FPGA

A User button (SW3) is available to drive a low signal to the IO-FPGA (nUSRBUTTON). This button is used to implement board-level reset in the factory-programmed image in the FPGA.

### 5.6.3 JTAG and Programming Header

The carrier board provides a 2x5-pin header, J8, for the IGLOO2 FPGA JTAG programming interface.

**TABLE 5-2: FPGA JTAG HEADER DESCRIPTION**

| Pin | JTAG | In/Out | Description |
|---|---|---|---|
| 1 | TCK | In | Test clock input for JTAG boundary scan, ISP, and UJTAG |
| 2 | GND | — | Ground |
| 3 | TDO | Out | Test serial output for JTAG boundary scan, ISP, and UJTAG usage |
| 4 | NC | — | — |
| 5 | TMS | In | Test mode select input. Weak pull-up resistor |
| 6 | 3V3 | — | 3.3V power |
| 7 | NC | — | — |
| 8 | TRSTB | In | Boundary scan Reset pin, active low, weak pull-up resistor |
| 9 | TDI (PD) | In | Test serial input for JTAG boundary scan, ISP, and UJTAG usage<br>Weak pull-up |
| 10 | GND | — | Ground |

### 5.6.4 FPGA Header for Debug SPI Access

The carrier board provides a 2x5-pin header (LVTTL levels), J9, for debug and control of the IO-FPGA by using the SPI interface found in Bank 8.

**TABLE 5-3: FPGA SPI AND HAT EEPROM $I^2C$ ACCESS**

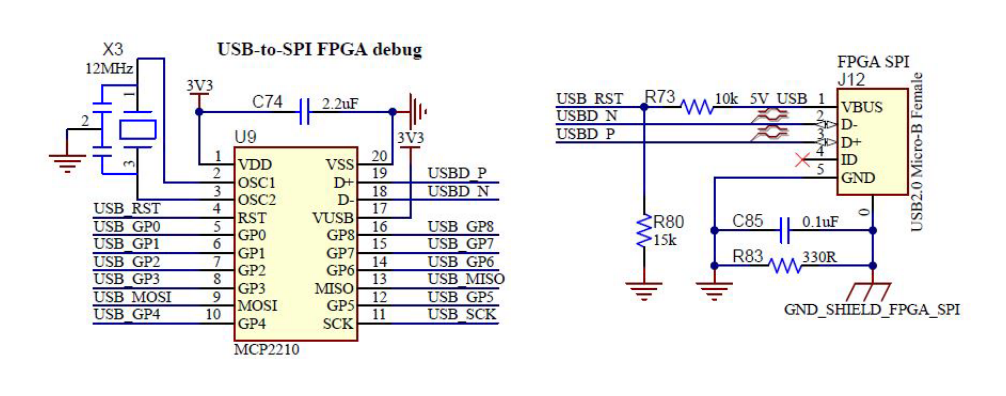
| Pin | JTAG | In/Out | Description |
|---|---|---|---|
| 1 | ID_SC | In | $I^2C$ clock to ID PROM |
| 2 | GND | — | Ground |
| 3 | ID_SD | In/Out | $I^2C$ data to ID PROM |
| 4 | PU to 3.3V | — | Pull-up resistor |
| 5 | AA_MISO | Out | SPI data output |
| 6 | NC | — | — |
| 7 | AA_SCK | In | SPI clock input |
| 8 | AA_MOSI | In | SPI data input |
| 9 | AA_SS | In | SPI slave select |
| 10 | GND | — | Ground |

The header also provides the ID PROM signals, ID_SC and ID_SD, for the HAT ID EEPROM that is used by the Raspberry Pi compute module 4.

### 5.6.5 Micro-USB Connector for FPGA Debug SPI Access

Figure 5-6 shows the on-board micro-USB type A, female connector, J12, for debug and control of the IO-FPGA by using an USB-to-SPI converter, MCP2210, connected to the SPI interface in Bank 3. MCP2210 also has eight GPIO pins, which are all connected to the IO-FPGA.

**FIGURE 5-6: MICRO-USB 2.0 FOR FPGA DEBUG**




### 5.6.6 FPGA Probe

The carrier board provides a 3-pin header, J7, for FPGA probing. The two live probe I/O cells have two purposes:

- Live probe functionality
- User I/O

## 5.7 RASPBERRY PI COMPUTE MODULE 4 INTERFACE CONNECTOR

Table 5-4 and Table 5-5 list the signals supported on the carrier boards' CM4 interface connector. Figure 5-7 and Figure 5-8 show the connection diagrams.

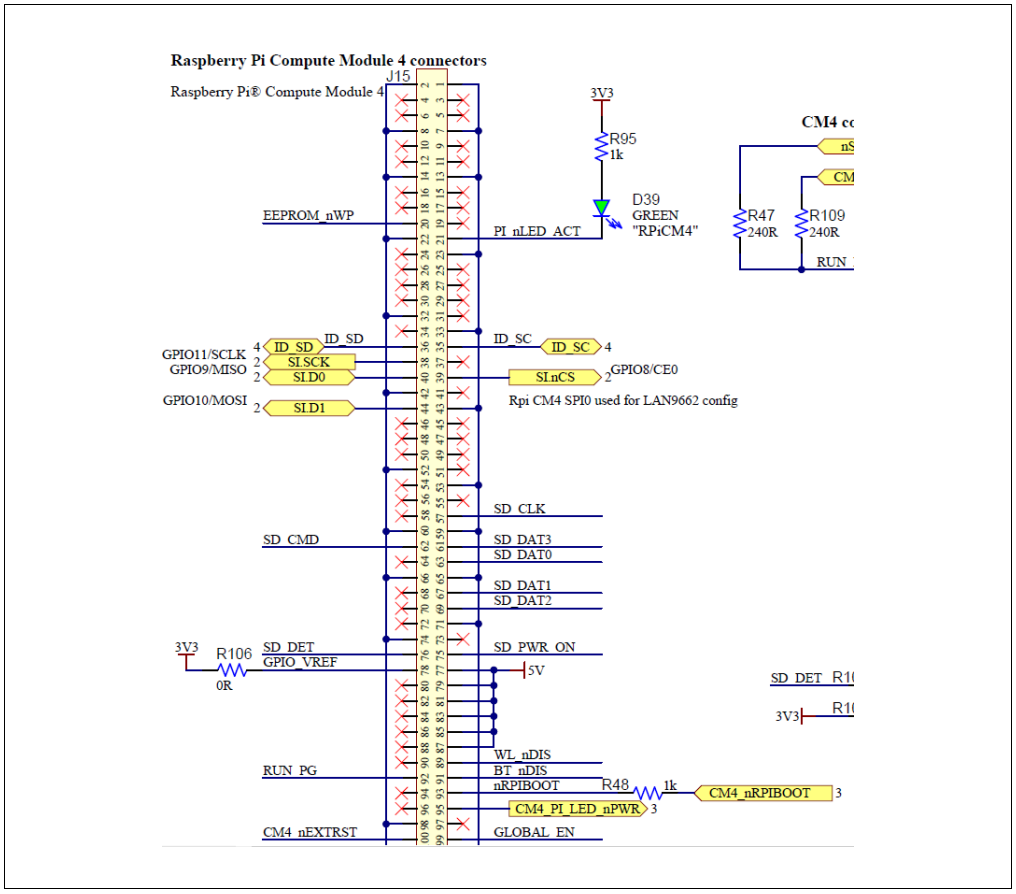
**TABLE 5-4: RPI CM4 CONNECTOR, J15**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | GND | 2 | GND |
| 3 | NC | 4 | NC |
| 5 | NC | 6 | NC |
| 7 | GND | 8 | GND |
| 9 | NC | 10 | NC |
| 11 | NC | 12 | NC |
| 13 | GND | 14 | GND |
| 15 | NC | 16 | NC |
| 17 | NC | 18 | NC |
| 19 | NC | 20 | EEPROM_nWP |
| 21 | RPI_nLED_ACT | 22 | GND |
| 23 | GND | 24 | NC |
| 25 | NC | 26 | NC |
| 27 | NC | 28 | NC |
| 29 | NC | 30 | NC |
| 31 | NC | 32 | GND |
| 33 | GND | 34 | NC |
| 35 | ID_SC | 36 | ID_SD |
| 37 | NC | 38 | SI.CLK |
| 39 | SI.nCS | 40 | SI.D0 |
| 41 | NC | 42 | GND |
| 43 | GND | 44 | SI.D1 |
| 45 | NC | 46 | NC |
| 47 | NC | 48 | NC |
| 49 | NC | 50 | NC |
| 51 | NC | 52 | GND |
| 53 | GND | 54 | NC |
| 55 | NC | 56 | NC |
| 57 | SC_CLK | 58 | NC |
| 59 | GND | 60 | GND |
| 61 | SD_DAT3 | 62 | SD_CMD |
| 63 | SD_DAT0 | 64 | NC |
| 65 | GND | 66 | GND |
| 67 | SD_DAT1 | 68 | NC |
| 69 | SD_DAT2 | 70 | NC |
| 71 | GND | 72 | NC |
| 73 | NC | 74 | GND |
| 75 | SD_PWR_ON | 76 | SD_DET |
| 77 | 5V | 78 | GPIO_VREF |
| 79 | 5V | 80 | NC |
| 81 | 5V | 82 | NC |

**TABLE 5-4: RPI CM4 CONNECTOR, J15 (CONTINUED)**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 83 | 5V | 84 | NC |
| 85 | 5V | 86 | NC |
| 87 | 5V | 88 | NC |
| 89 | WL_nDIS | 90 | NC |
| 91 | BT_nDIS | 92 | RUN_PG |
| 93 | nRPIBOOT | 94 | NC |
| 95 | CM4_PI_LED_nPWR | 96 | NC |
| 97 | NC | 98 | GND |
| 99 | GLOBAL_EN | 100 | CM4_nEXTRST |

**FIGURE 5-7: RASPBERRY PI COMPUTE MODULE 4 INTERFACE CONNECTOR, J15**




**Note:** RPI activity is displayed with a green LED, D39.

**TABLE 5-5: RPI CM4 CONNECTOR, J19**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | USBOTG_ID | 2 | PCIE_CLK_nREQ |
| 3 | USB2PI_N | 4 | NC |
| 5 | USB2PI_P | 6 | NC |

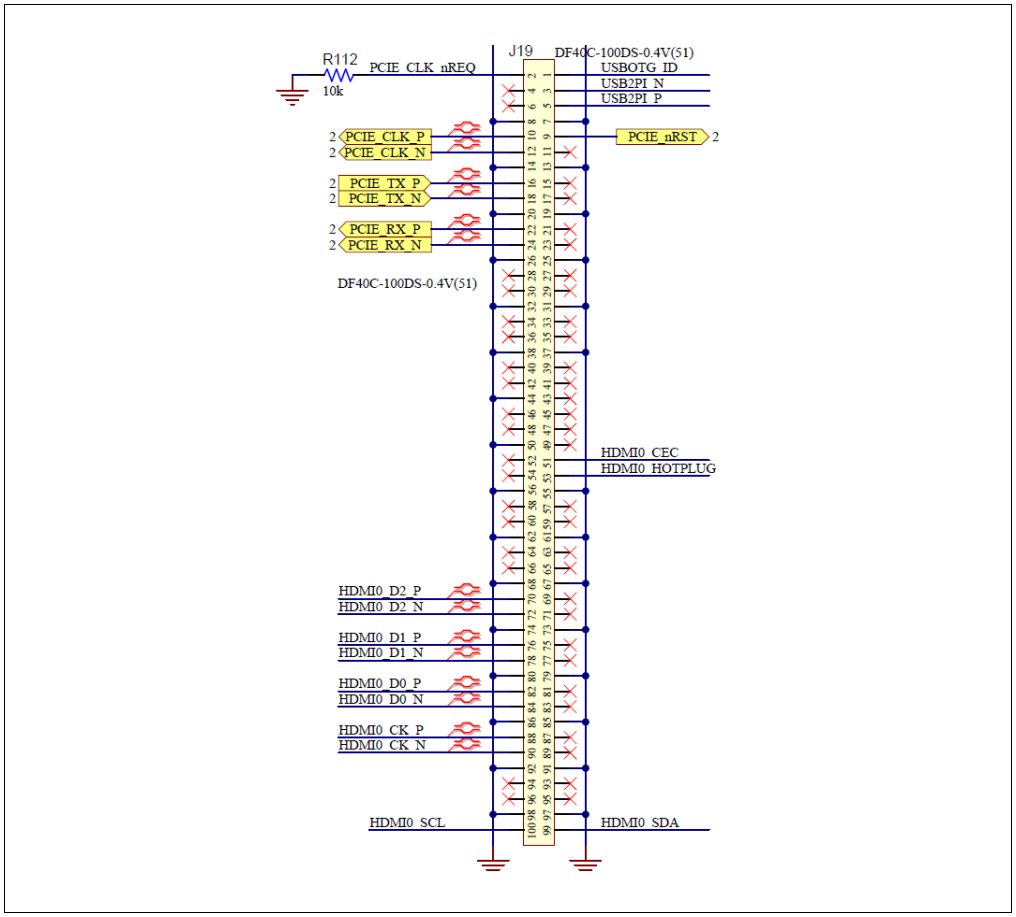
**TABLE 5-5: RPI CM4 CONNECTOR, J19 (CONTINUED)**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 7 | GND | 8 | GND |
| 9 | PCIE_nRST | 10 | PCIE_CLK_P |
| 11 | NC | 12 | PCIE_CLK_N |
| 13 | GND | 14 | GND |
| 15 | NC | 16 | PCIE_TX_P |
| 17 | NC | 18 | PCIE_TX_N |
| 19 | GND | 20 | GND |
| 21 | NC | 22 | PCIE_RX_P |
| 23 | NC | 24 | PCIE_RX_N |
| 25 | GND | 26 | GND |
| 27 | NC | 28 | NC |
| 29 | NC | 30 | NC |
| 31 | GND | 32 | GND |
| 33 | NC | 34 | NC |
| 35 | NC | 36 | NC |
| 37 | GND | 38 | GND |
| 39 | NC | 40 | NC |
| 41 | NC | 42 | NC |
| 43 | NC | 44 | GND |
| 45 | NC | 46 | NC |
| 47 | NC | 48 | NC |
| 49 | NC | 50 | GND |
| 51 | HDMI0_CEC | 52 | NC |
| 53 | HDMI0_HOTPLUG | 54 | NC |
| 55 | GND | 56 | GND |
| 57 | NC | 58 | NC |
| 59 | NC | 60 | NC |
| 61 | GND | 62 | GND |
| 63 | NC | 64 | NC |
| 65 | NC | 66 | NC |
| 67 | GND | 68 | GND |
| 69 | NC | 70 | HDMI0_D2_P |
| 71 | NC | 72 | HDMI0_D2_N |
| 73 | GND | 74 | GND |
| 75 | NC | 76 | HDMI0_D1_P |
| 77 | NC | 78 | HDMI0_D1_N |
| 79 | GND | 80 | GND |
| 81 | NC | 82 | HDMI0_D0_P |
| 83 | NC | 84 | HDMI0_D0_N |
| 85 | GND | 86 | GND |
| 87 | NC | 88 | HDMI0_CK_P |
| 89 | NC | 90 | HDMI0_CK_N |
| 91 | GND | 92 | GND |
| 93 | NC | 94 | NC |
| 95 | NC | 96 | NC |

**TABLE 5-5: RPI CM4 CONNECTOR, J19 (CONTINUED)**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 97 | GND | 98 | GND |
| 99 | HDMI0_SDA | 100 | HDMI0_SCL |

**FIGURE 5-8: RASPBERRY PI COMPUTE MODULE 4 INTERFACE CONNECTOR, J19**




### 5.7.1 PCIe® 2.0 Endpoint and SPI

The carrier board provides PCIe 2.0 and SPI access to the LAN9662 from the Raspberry Pi compute module 4, so the RPI can act as an external CPU system.

**Note:** The PCIe_CLK is biased to 0.6V using a 10 kΩ resistor divider.

### 5.7.2 CM4 USB 2.0 Host Ports

When operating as USB host, a USB switch located on the carrier board connects the Raspberry Pi 4 USB port to a USB hub, USB2512B-I/M2, to provide two USB 2.0 host ports. Figure 5-9 shows the use of the USB host hub.

**FIGURE 5-9: CM4 USB HOST HUB**

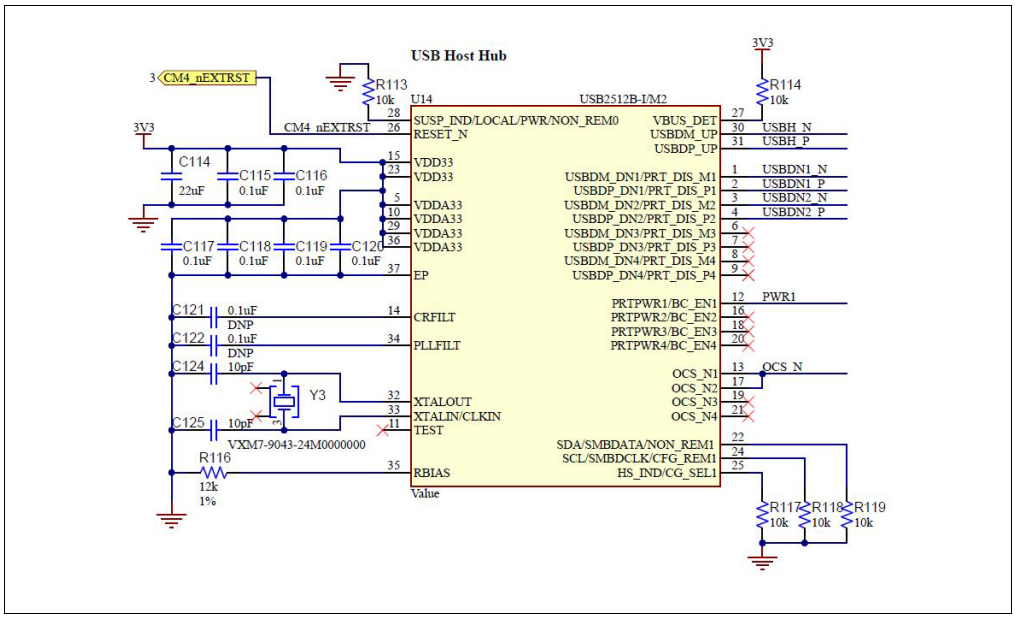
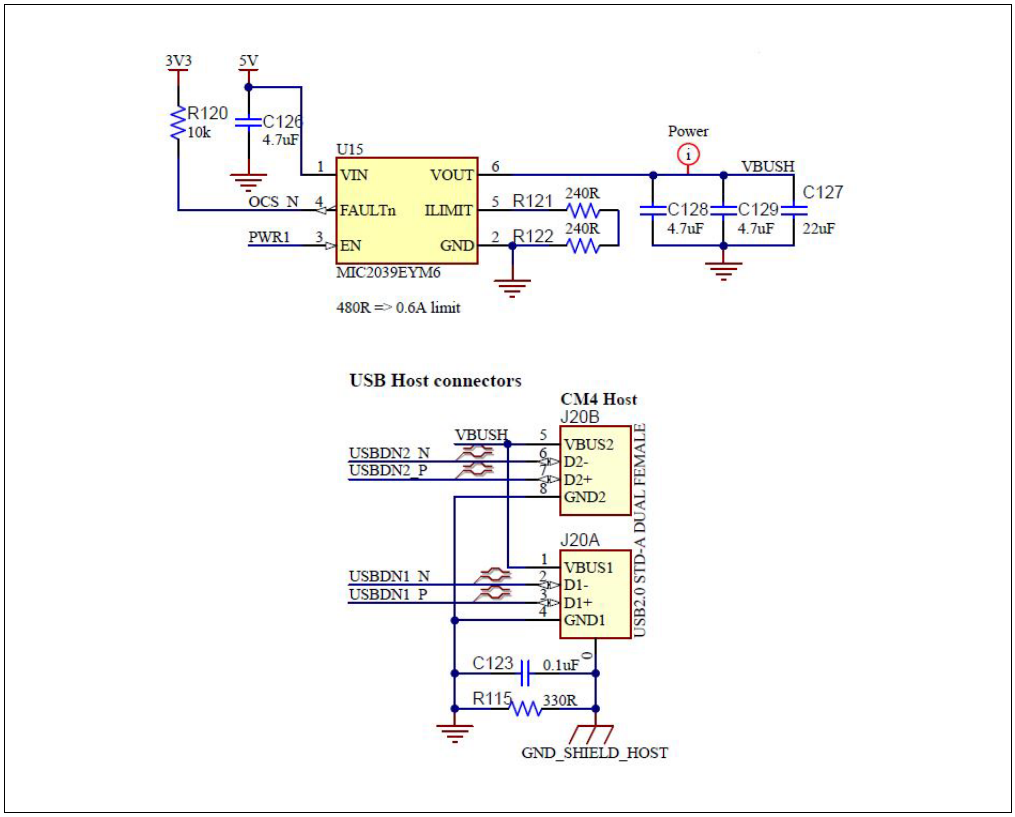



Figure 5-10 shows the use of a 2x1 USB type-A female connector, J20. The USB host ports are current limited to 600 mA by using MIC2039.

**FIGURE 5-10: CM4 USB HOST POWER AND CONNECTORS**

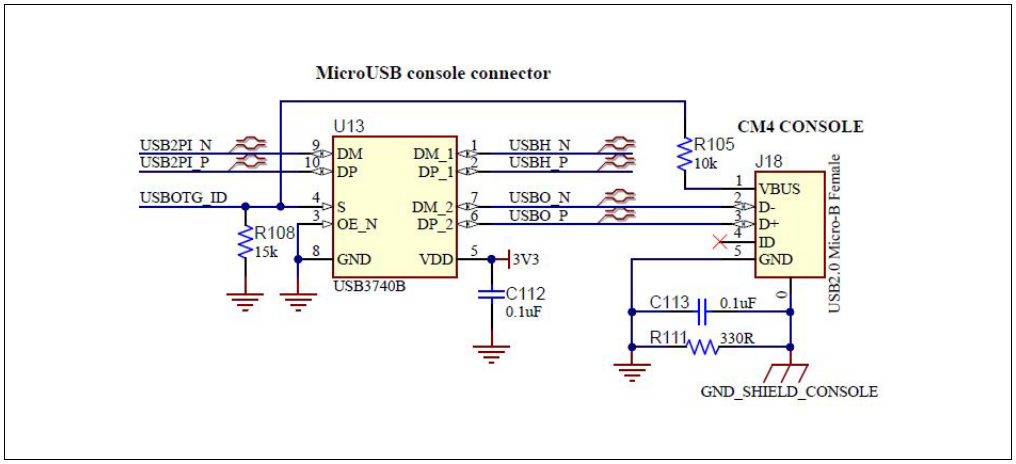


### 5.7.3 CM4 micro-USB Console Port

The carrier board provides a USB 2:1 switch, USB3740B, to automatically change between being a host or client interface. The client interface has precedence over the host interface.

When operating as a client, the USB switch connects directly to a 'console' port to the Raspberry Pi compute module 4 by offering a micro-USB type-A female connector, J18. Figure 5-11 shows the USB3740B and the micro-USB connector to access the Raspberry Pi compute module 4.

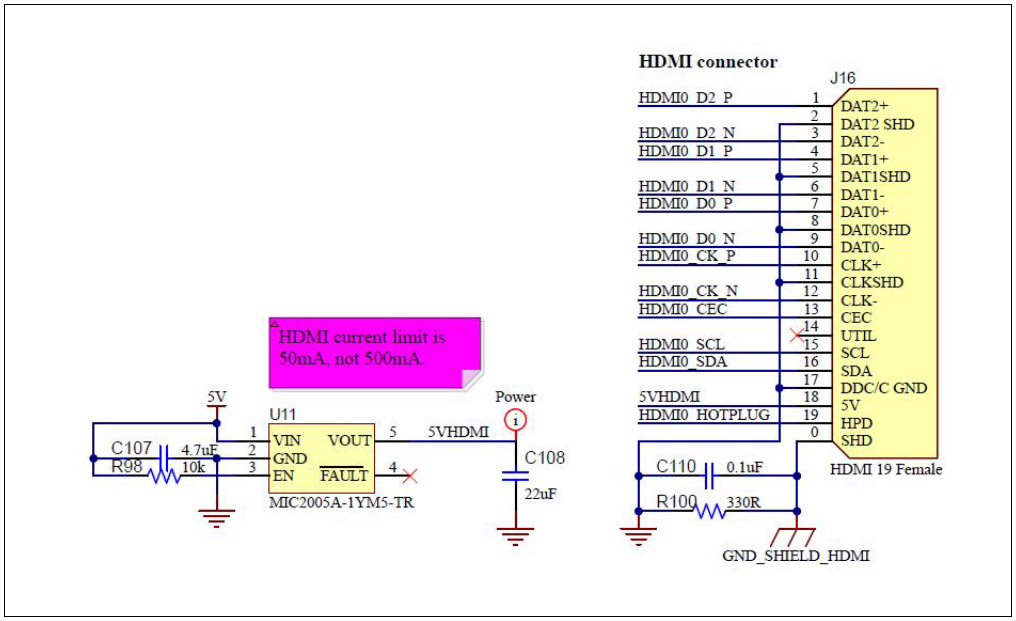
**FIGURE 5-11: CM4 MICRO-USB CONSOLE PORT**




### 5.7.4 CM4 HDMI Connector

Figure 5-12 shows the HDMI connector supported by the Raspberry Pi compute module 4. The HDMI is current limited to 50 mA by using MIC2005A.

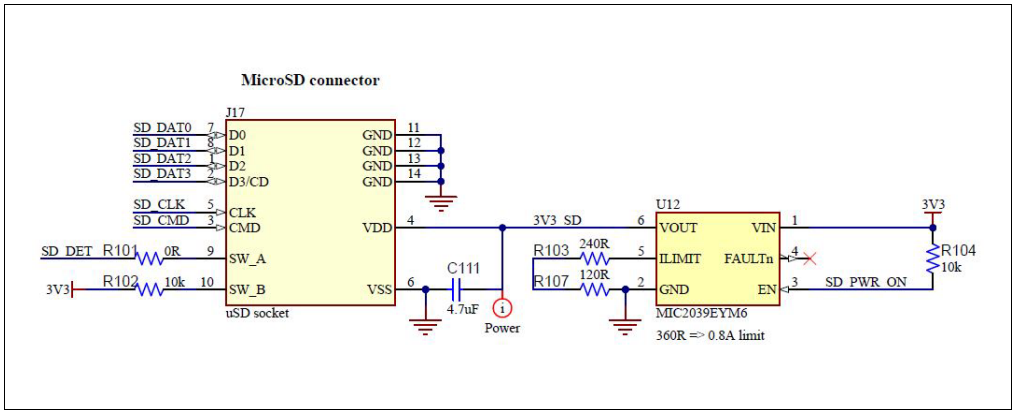
**FIGURE 5-12: CM4 HDMI CONNECTOR**



### 5.7.5 CM4 micro-SD Connector

Figure 5-13 shows the micro-SD connector supported by the Raspberry Pi compute module 4. The SD slot is current limited to 800 mA by using MIC2039.

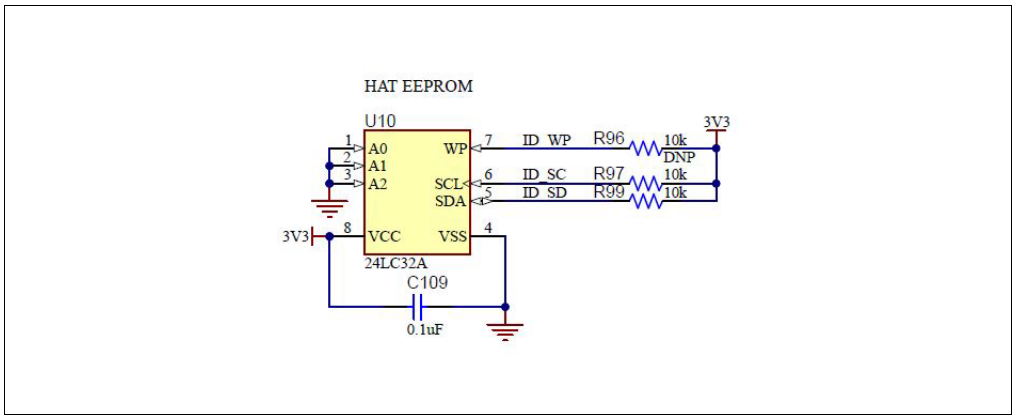
**FIGURE 5-13: CM4 MICRO-SD SLOT**




### 5.7.6 CM4 HAT ID EEPROM

Figure 5-14 shows the diagram of the on-board I$^2$C EEPROM, 24LC32A – 4KB, to support HAT function. This EEPROM will not initially be ID programmed.

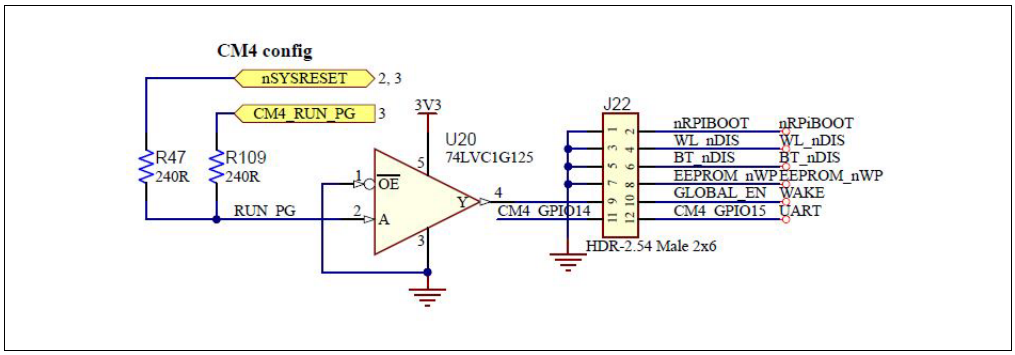
**FIGURE 5-14: CM4 HAT EEPROM**




### 5.7.7 CM4 Configuration Header

Figure 5-15 shows the 2x6-pin male header, J22, used for CM4 configuration. The CM4 configuration signals found here are: WL_nDIS, BT_nDIS, EEPROM_nWP, nRPI-BOOT, GLOBAL_EN, CM4_GPIO14, and CM4_GPIO15.

**FIGURE 5-15: CM4 CONFIGURATION HEADER**



## 5.8 OPTIONAL REFERENCE CLOCK

The carrier board can optionally be equipped with an external 125 MHz differential reference clock, Y1, like DSC1201 to source the LAN9662 SerDes macros. The reference clock is then provided through the SO-DIMM connector.

## 5.9 CONTROL OF BOARD RESET

The CM4 module can control the Reset of the full EVB-LAN9662 evaluation board through the PCIe_nRST. Optionally, the PCIe_nRST can be set to only reset the LAN9662 PCIe endpoint controller.

## 5.10 POWER DC INPUT AND LED

The carrier board is intended to be 12VDC/2A powered through a standard input jack. However, the on-board buck step-down regulator, MCP19035-BAABE/MF, U17 accepts 7.5V to 30V input range to deliver a 5V at 4.7A output to:

- EVB-LAN9662 End-Node module (1.0A)
- RPI CM4 module (1.8A)
- RPI CM4 USB Host (0.6A)
- RPI CM4 HDMI (0.1A)
- DC/DC converters on the carrier board (1.2A)

### 5.10.1 DC/DC Converters

The carrier board generates the following power supplies (worst-case currents):

- 1.20V at 1.2A use MIC23201 2A buck regulator. Powers FPGA.
- 2.50V at 0.2A use MIC23030 0.4A buck regulator. Powers FPGA.
- 3.30V at 1.0A use MIC23201 2A buck regulator. Powers FPGA (0.2A), SFP (0.6A) and miscellaneous (0.2A)

A single green LED (D43) indicates power-on using the 3.3V supply.

### 5.10.2 Power Supply Sequencing

The overall strategy for the switch power supply sequencing is not to let a higher-powered supply feeding lower-level powered grids through the internal protection diode network. The general power sequence is, therefore:

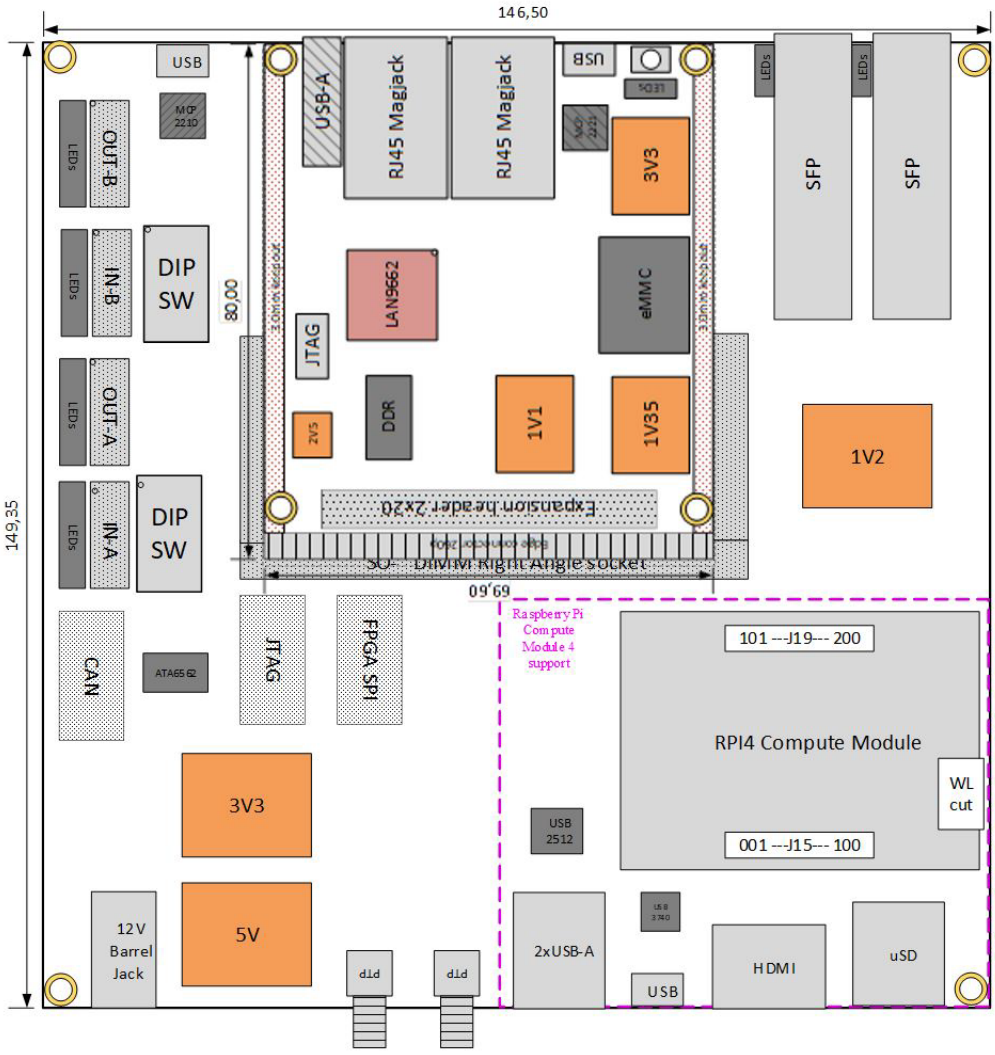
1V2 → 2V5/3V3

# Appendix A. PCB Layout and Silk Screens

## A.1 INTRODUCTION

Figure A-1 shows the outline of the EVB-LAN9662 End-Node module installed into the EVB-LAN9662-Carrier SO-DIMM connector to conform the full EVB-LAN9662 evaluation board. The EVB-LAN9662 End-Node dimensions are 80.00x69.60x1.20 mm. The EVB-LAN9662-Carrier dimensions are 149.35x146.50x1.60 mm.

**FIGURE A-1: EVB-LAN9662 AND EVB-LAN9662-CARRIER OUTLINE**




The LAN9662 package pinout is specifically optimized for low-cost PCB designs. As a result, the EVB-LAN9662 End-Node module has only four PCB layers, while the EVB-LAN9662-Carrier reference board has six PCB layers.

On the EVB-LAN9662 module, all signals are routed on the top and bottom layers, 1 and 4. Layer 2 is a solid ground plane, which is also used to remove heat from components, and it must (also for this reason) be ensured, that good connection between the outer layer ground fills and the ground planes are established.

On the EVB-LAN9662-Carrier, most signals are routed on the top and bottom layers, 1 and 6, but also layer 4 is used. Layers 2 and 5 are solid ground planes.

## A.2 EVB-LAN9662 END-NODE PCB LAYERS

Figure A-2 shows the overall placement of components on the EVB-LAN9662 End-Node module.

**FIGURE A-2: EVB-LAN9662 END-NODE TOP SILK SCREEN**

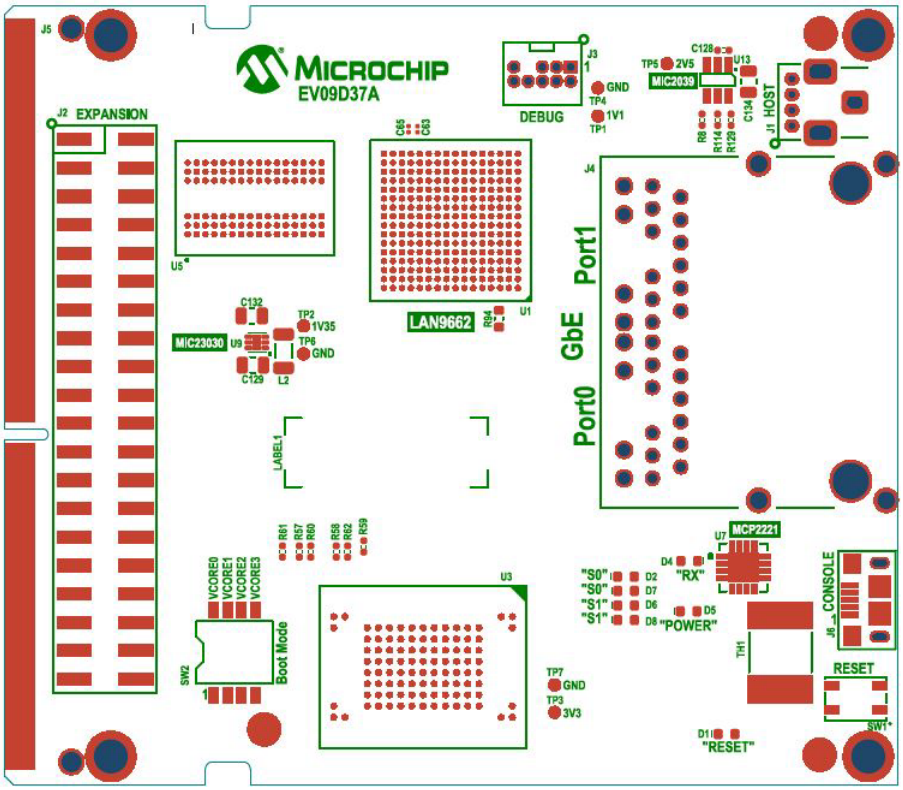



Table A-1 describes the different layers in the EVB-LAN9662 End-Node module.

**TABLE A-1: EVB-LAN9662 END-NODE PCB LAYERS AND DESCRIPTIONS**

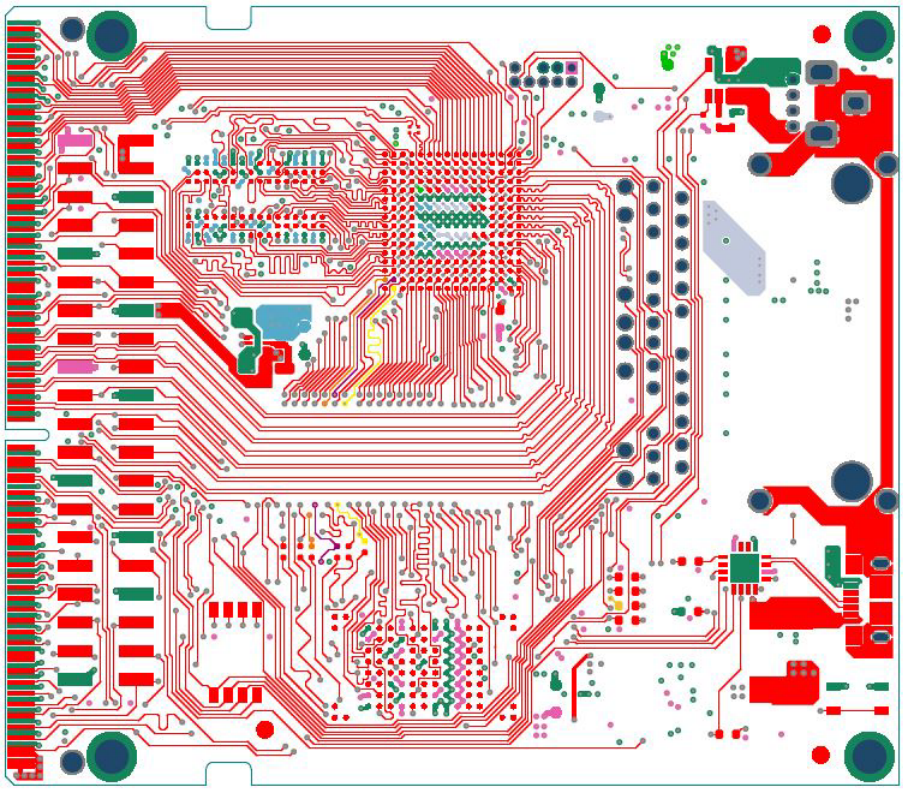
| Layer | Description |
|---|---|
| 1 (TOP) | LAN9662 signal traces for DDR3L and SerDes paths |
| 2 (GND) | Solid ground plane |
| 3 (POWER) | Power planes for LAN9662: 1.1V, 1.35V, 2.5V, 3.3V and 5V |
| 6 (BOTTOM) | LAN9662 signal traces for DDR3L |

The ground shield found on the top and bottom layers serves as 'quiet' ground for PHY copper media signals. It is connected via an RC network to the ground plane, providing a low-impedance return path for high-frequency noise.

### A.2.1 EVB-LAN9662 End-Node Layer 1 (TOP)

The EVB-LAN9662 End-Node layer 1 consists of mostly signal traces for DDR3L and SerDes macros, SFP slots.

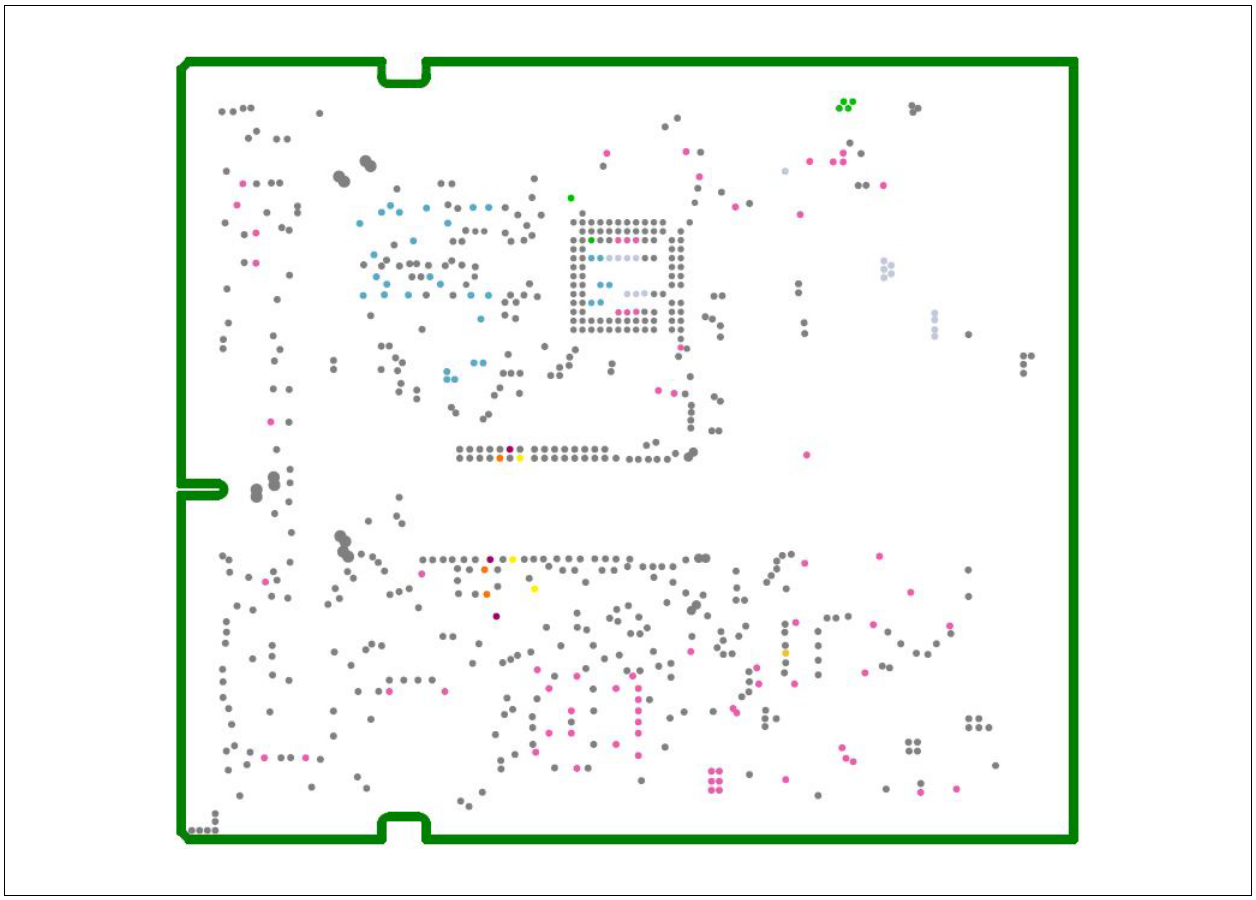
**FIGURE A-3: EVB-LAN9662 END-NODE LAYER 1**



### A.2.2 EVB-LAN9662 End-Node Layer 2 (GND)

The EVB-LAN9662 End-Node layer 2 is pure ground plane.

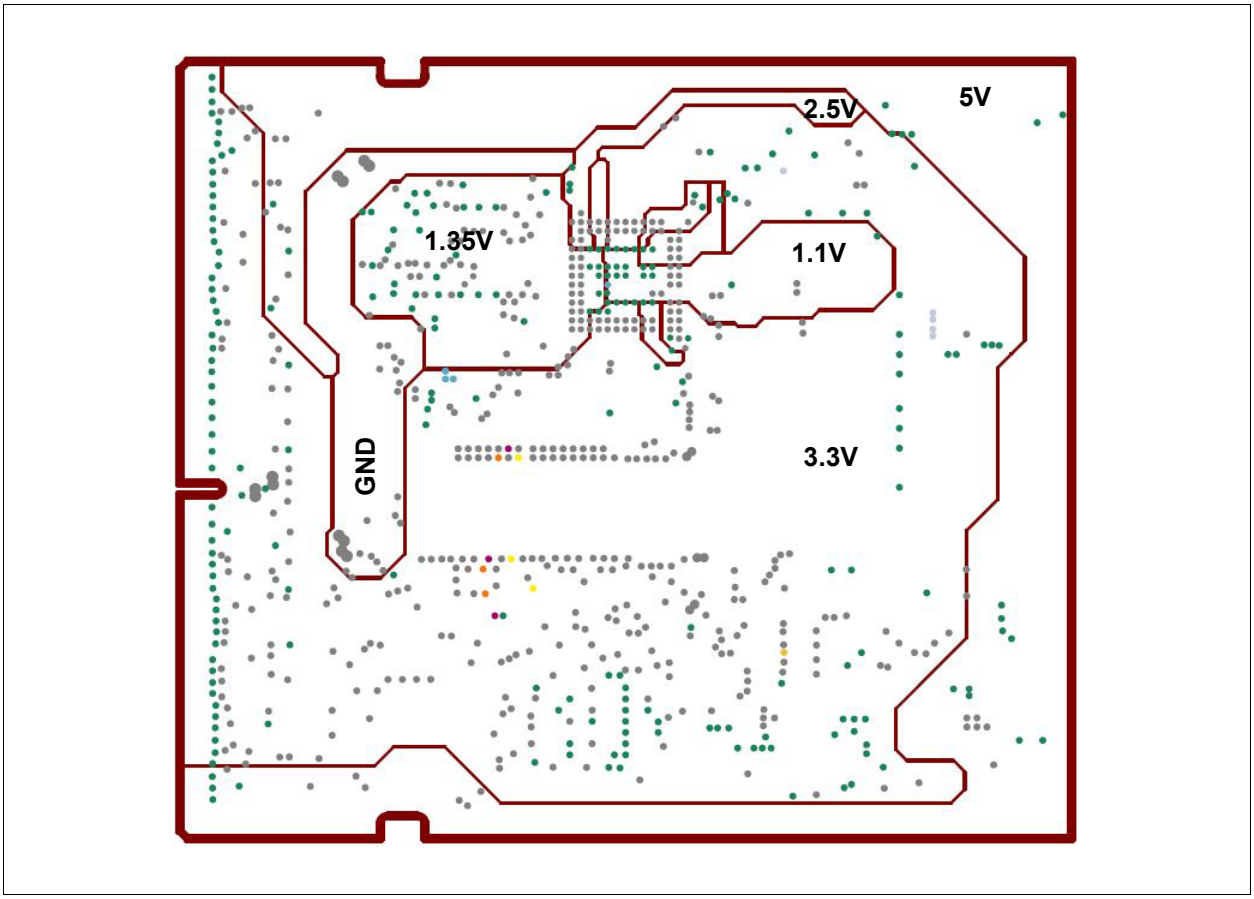
**FIGURE A-4: EVB-LAN9662 END-NODE LAYER 2**



### A.2.3 EVB-LAN9662 End-Node Layer 3 (POWER)

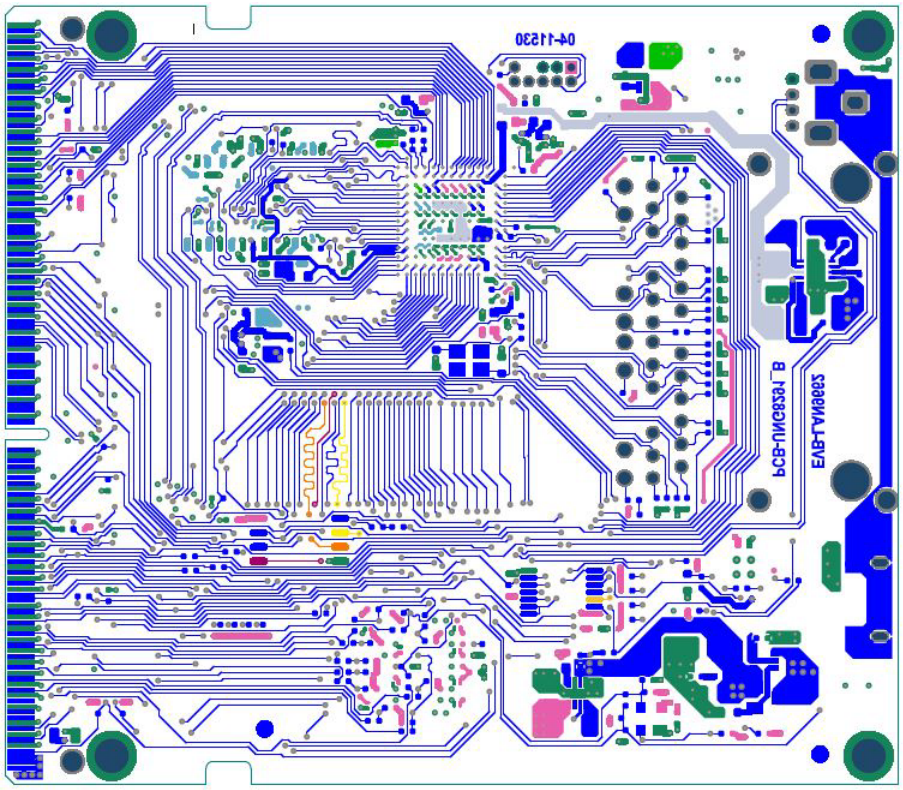
The EVB-LAN9662 End-Node layer 3 consists of power and ground planes.

**FIGURE A-5: EVB-LAN9662 END-NODE LAYER 3**



### A.2.4 EVB-LAN9662 End-Node Layer 4 (BOTTOM)

**FIGURE A-6: EVB-LAN9662 END-NODE LAYER 4**



### A.2.5 EVB-LAN9662 End-Node DDR3L Close Up

Refer to Figure A-7 and Figure A-8 to see how the DDR length matching is acquired.

**FIGURE A-7: EVB-LAN9662 END-NODE DDR3L CLOSE UP (TOP)**

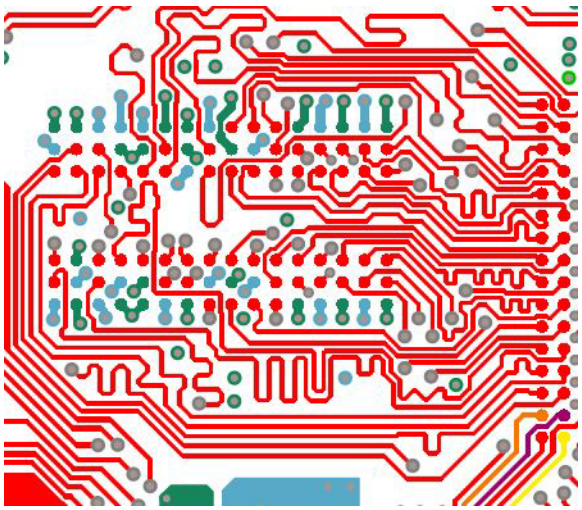
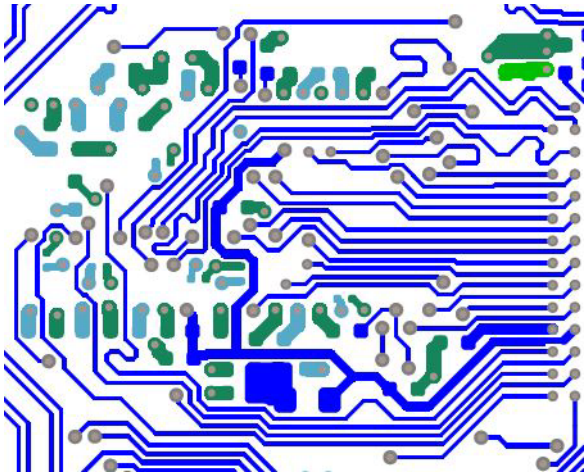


**FIGURE A-8: EVB-LAN9662 END-NODE DDR3L CLOSE UP (BOTTOM)**



### A.2.6 EVB-LAN9662 End-Node PCB Layer Stack-up

The EVB-LAN9662 End-Node module is a 4-layer impedance-controlled PCB. Figure A-9 shows the stack-up.

**FIGURE A-9: EVB-LAN9662 END-NODE PCB STACK-UP**

Board Stack Report

| Stack Up | | Layer Stack | | | |
|---|---|---|---|---|---|
| Layer | Board Layer Stack | Name | Material | Thickness | Constant |
| 1 | | Top Paste | | | |
| 2 | | Top Overlay | | | |
| 3 | | Top Solder | LPI-Green | 0,39mil | 3,5 |
| 4 | | Top Layer 1 | Copper | 2,01mil | |
| 5 | | Dielectric1 | PP-370HR-1080_71 | 3,58mil | 3,81 |
| 6 | | Inner Layer 2 | Copper | 1,38mil | |
| 7 | | Dielectric 2 | CR-370HR-5x7628 | 35,00mil | 4,36 |
| 8 | | Inner Layer 3 | Copper | 1,38mil | |
| 9 | | Dielectric 1 | PP-370HR-1080_71 | 3,58mil | 3,81 |
| 10 | | Bottom Layer | Copper | 2,01mil | |
| 11 | | Bottom Solder | LPI-Green | 0,39mil | 3,5 |
| 12 | | Bottom Overlay | | | |
| 13 | | Bottom Paste | | | |
| | Height : 49,73mil | | | | |

## A.3 EVB-LAN9662-CARRIER PCB LAYERS

Figure A-10 shows the overall placement of components on the EVB-LAN9662-Carrier board.

**FIGURE A-10: EVB-LAN9662-CARRIER TOP SILK SCREEN**

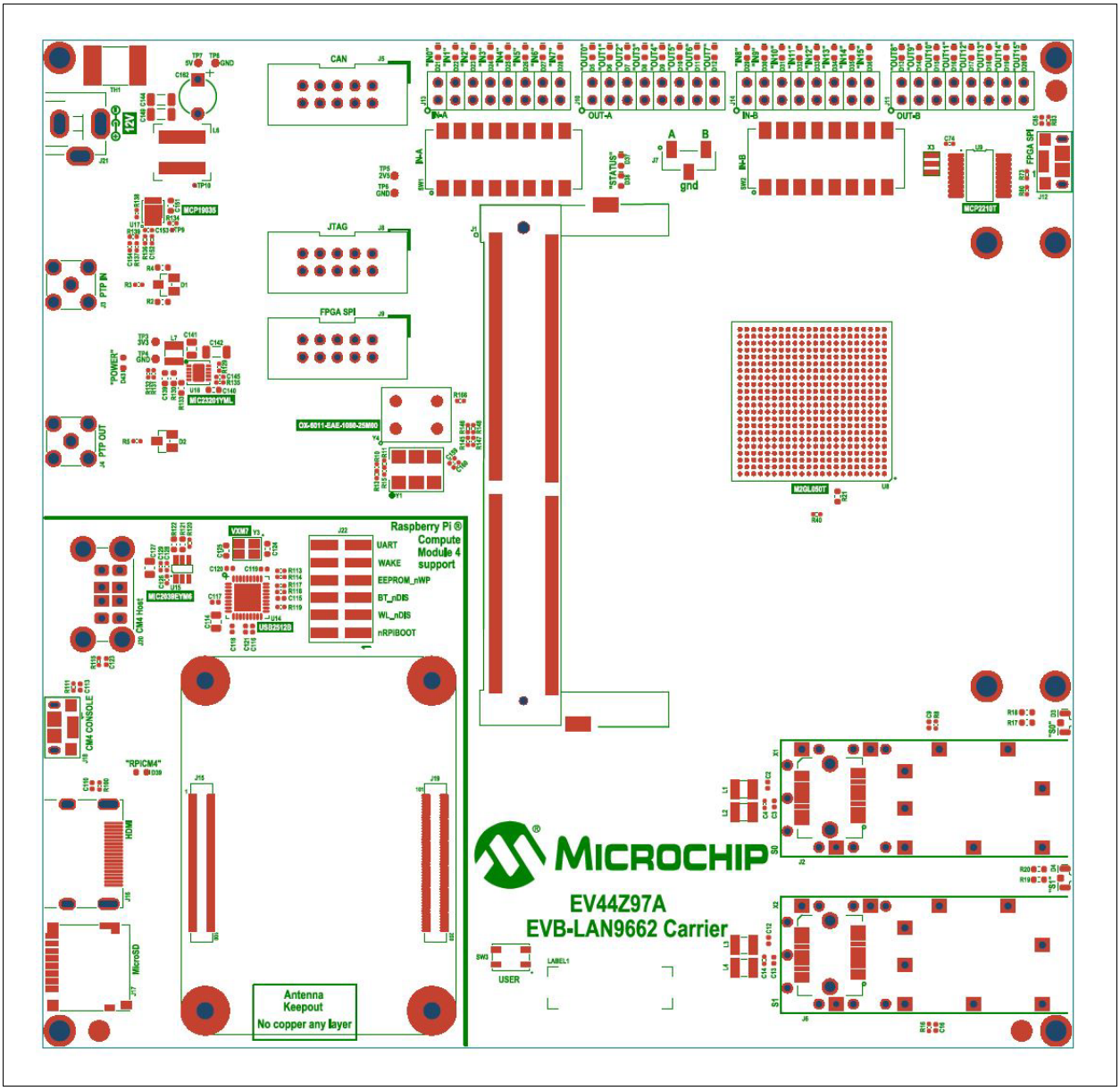



Table A-2 describes the different layers in the EVB-LAN9662-Carrier board.

**TABLE A-2: EVB-LAN9662-CARRIER PCB LAYERS AND DESCRIPTIONS**

| Layer | Description |
|---|---|
| 1 (TOP) | IO-FPGA signal traces and SerDes paths. Solder side for the SO-DIMM connector. |
| 2 (GND) | Solid ground plane |
| 3 (POWER) | Power planes for IO-FPGA: 2.5V and HDMI. Additional ground plane. |
| 4 (POWER) | Power planes for IO-FPGA: 3.3V and 2.5V |
| 5 (GND) | Solid ground plane |
| 6 (BOTTOM) | IO-FPGA signal traces. Serial GPIO signals. HDMII SerDes signals. |

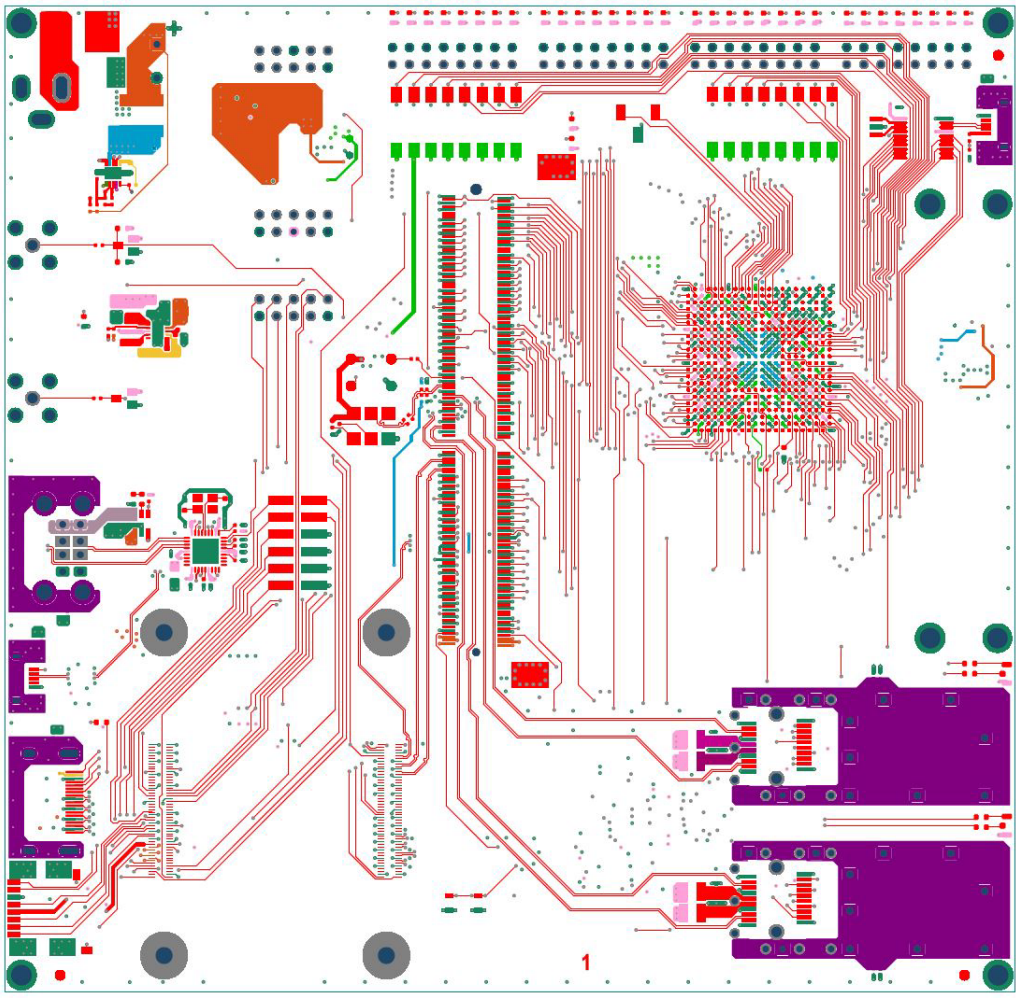
### A.3.1 EVB-LAN9662-Carrier Layer 1 (TOP)

The EVB-LAN9662-Carrier layer 1 consists of the following:

- SerDes signals to SFP slots
- UM4 Debug and control signals to Config header, J22
- UM4 USB Switch, USB2512B
- Digital input, dip-switch SW1 and SW2 to IO-FPGA
- SPI header to IO-FPGA
- Purple shielding around connectors

The shielding serves as 'quiet' ground for the signals in each connector. It is connected via an RC network to the ground plane, providing a low-impedance return path for high-frequency noise.

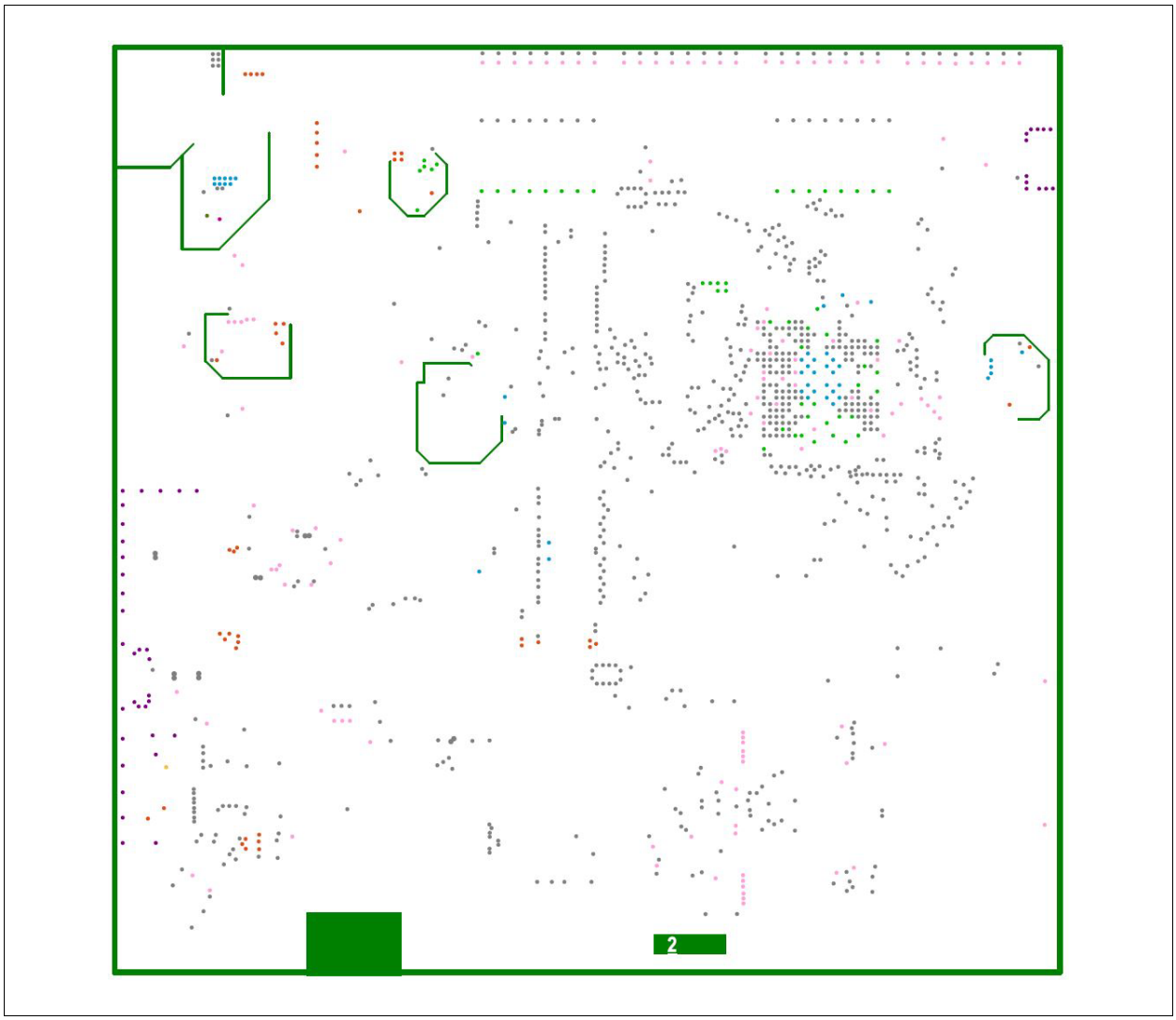
**FIGURE A-11: EVB-LAN9662-CARRIER LAYER 1**



### A.3.2 EVB-LAN9662-Carrier Layer 2 (GND)

The EVB-LAN9662-Carrier layer 2 is pure ground plane with cutout around the DC/DC power supplies.

**FIGURE A-12: EVB-LAN9662-CARRIER LAYER 2**

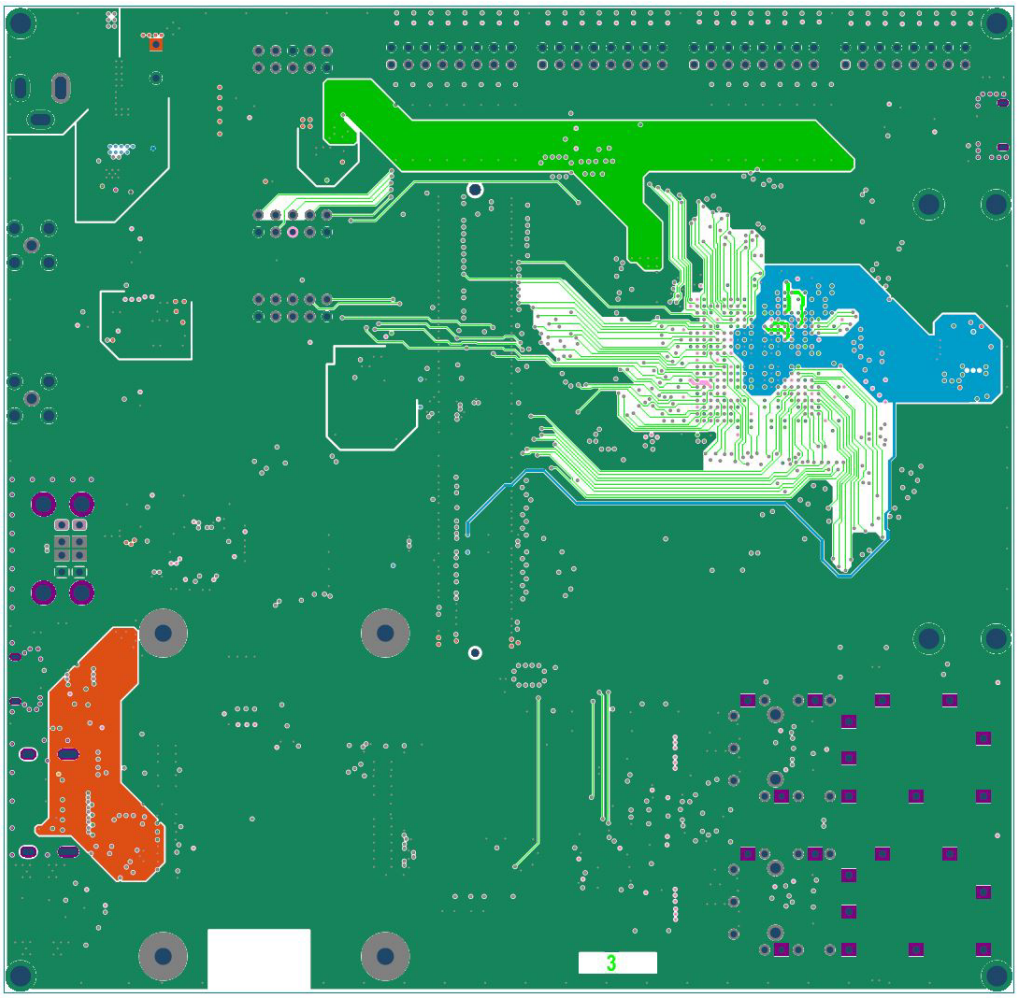


### A.3.3 EVB-LAN9662-Carrier Layer 3 (POWER)

The EVB-LAN9662-Carrier layer 3 consists of:

- Dark green ground
- Red 5V HDMI
- Blue 1.2V for IO-FPGA
- Light green for IO-FPGA Digital I/O

**FIGURE A-13: EVB-LAN9662-CARRIER LAYER 3**

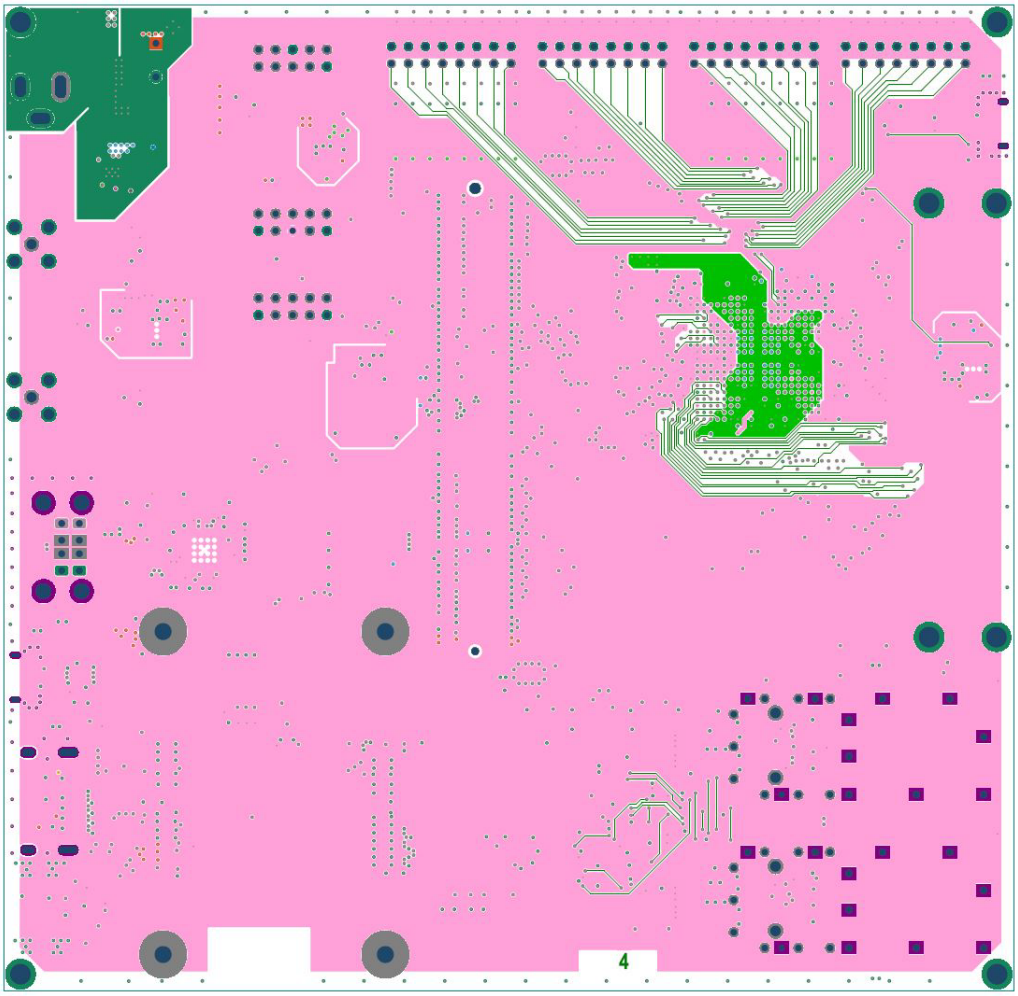


### A.3.4 EVB-LAN9662-Carrier Layer 4 (POWER)

The EVB-LAN9662-Carrier layer 4 consists of:

- Power planes
- Pink is 3.3V, light green is 2.5V to IO-FPGA
- Dark green is ground for the 12V supply input
- Digital I/O from IO-FPGA to pin headers: J10, J11, J13, and J14.

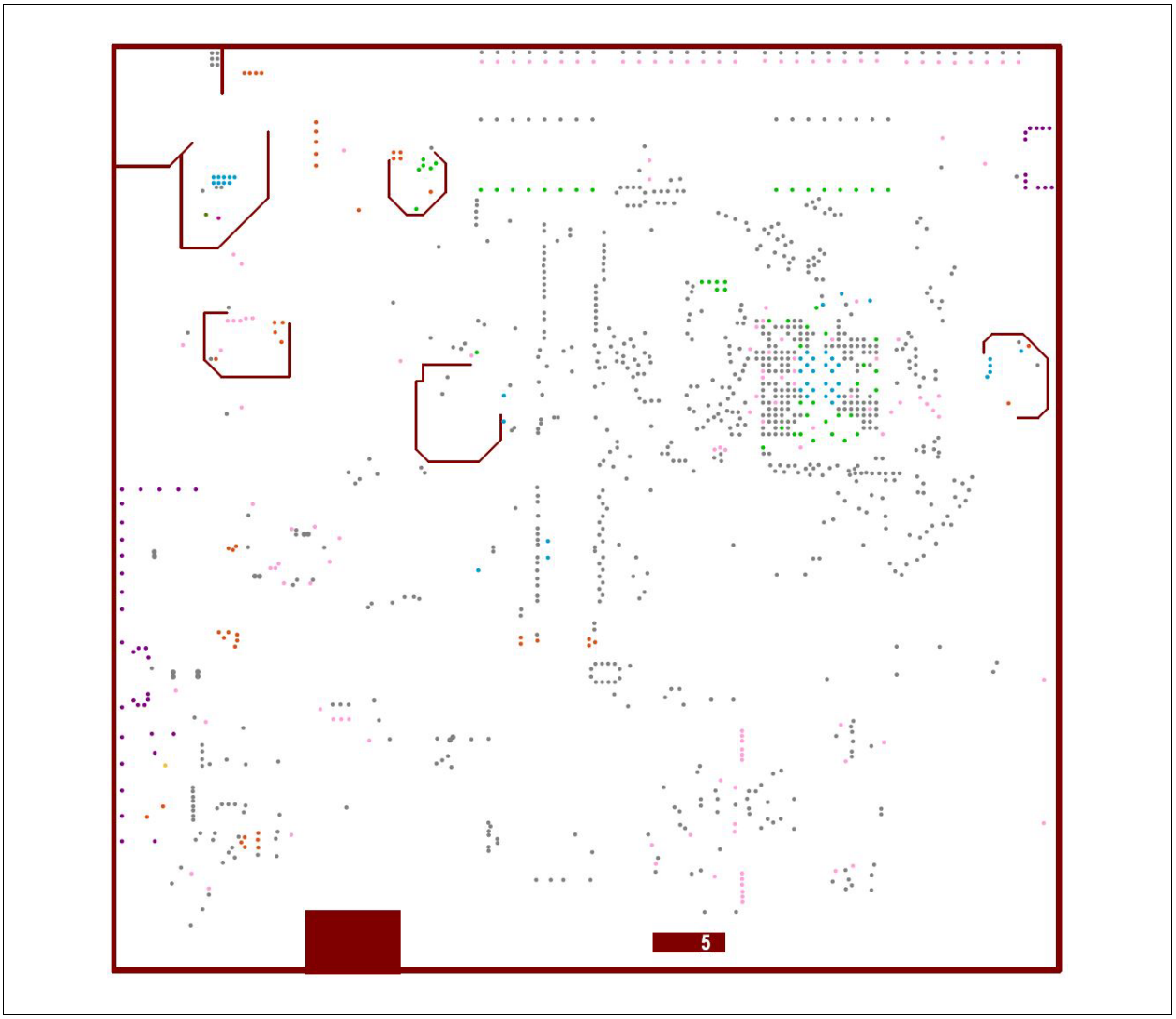
**FIGURE A-14: EVB-LAN9662-CARRIER LAYER 4**



### A.3.5 EVB-LAN9662-Carrier Layer 5 (GND)

The EVB-LAN9662-Carrier layer 5 consists of pure ground plane with cutout around the DC/DC power supplies.

**FIGURE A-15: EVB-LAN9662-CARRIER LAYER 5**

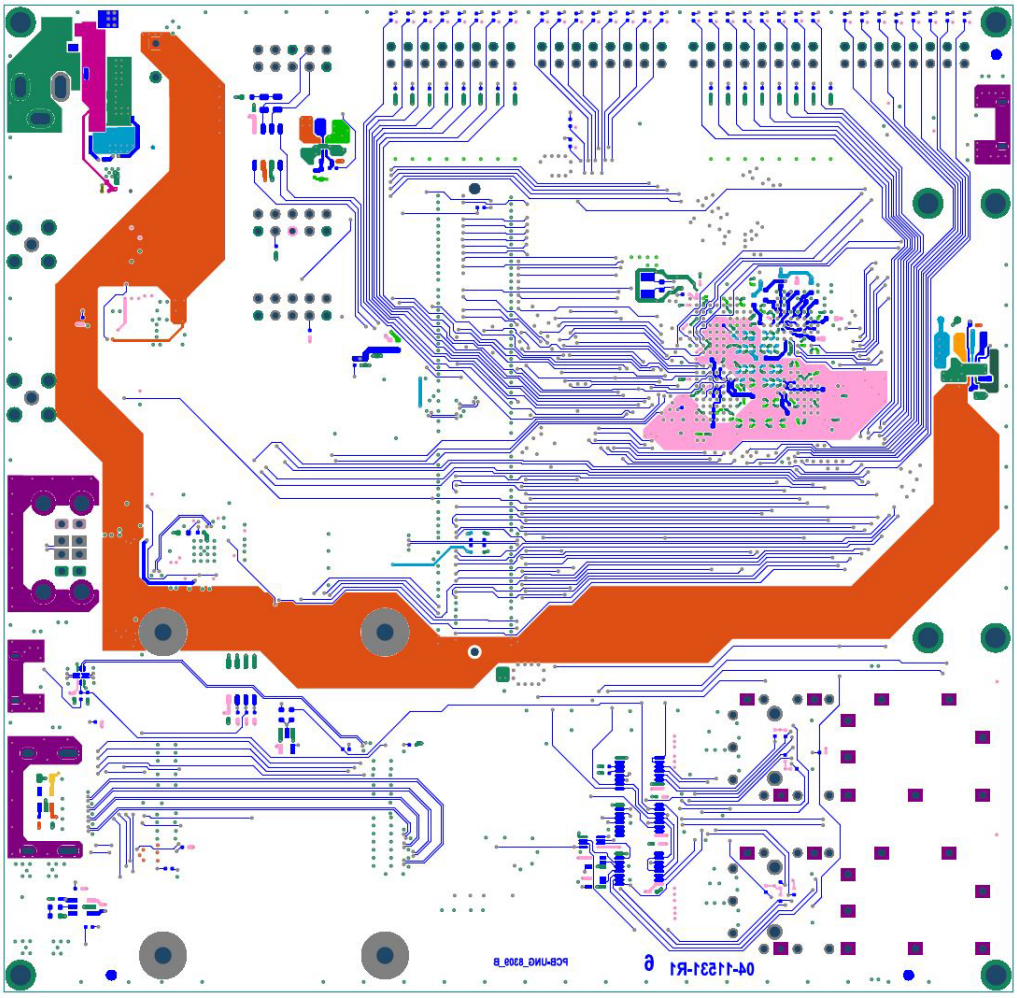


### A.3.6 EVB-LAN9662-Carrier Layer 6 (BOTTOM)

The EVB-LAN9662-Carrier layer 6 consists of:

- 12-30V DC, power and ground to MCP19035 for 5V DC generation
- SO-DIMM GPIO signals from LAN9662 to FPGA
- Digital I/O from IO-FPGA to pin header: J10, J11, J13 and J14
- 5V power distribution to U16 MIC23201YML, 1.2V to IO-FPGA
- FPGA micro-USB shield
- UM4 Host USB connector and shielding
- UM4 micro-USB, USB3740B and shielding
- UM4 HAT EEPROM, 24LC32AT
- UM4 HDMI SerDes and shielding
- Serial GPIO: U1, U4 and U6

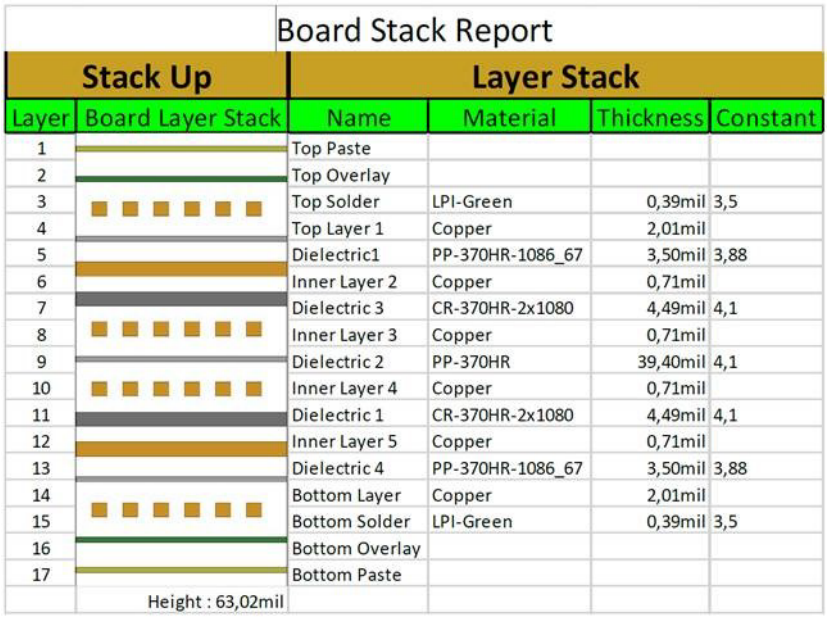
**FIGURE A-16: EVB-LAN9662-CARRIER LAYER 6**



### A.3.7 EVB-LAN9662-Carrier PCB Layer Stack-Up

The EVB-LAN9662-Carrier board is a 6-layer impedance-controlled PCB. Figure A-17 shows the stack-up.

**FIGURE A-17: EVB-LAN9662-CARRIER PCB STACK-UP**



Board Stack Report

| Stack Up | | Layer Stack | | | |
|---|---|---|---|---|---|
| Layer | Board Layer Stack | Name | Material | Thickness | Constant |
| 1 | | Top Paste | | | |
| 2 | | Top Overlay | | | |
| 3 | | Top Solder | LPI-Green | 0,39mil | 3,5 |
| 4 | | Top Layer 1 | Copper | 2,01mil | |
| 5 | | Dielectric1 | PP-370HR-1086_67 | 3,50mil | 3,88 |
| 6 | | Inner Layer 2 | Copper | 0,71mil | |
| 7 | | Dielectric 3 | CR-370HR-2x1080 | 4,49mil | 4,1 |
| 8 | | Inner Layer 3 | Copper | 0,71mil | |
| 9 | | Dielectric 2 | PP-370HR | 39,40mil | 4,1 |
| 10 | | Inner Layer 4 | Copper | 0,71mil | |
| 11 | | Dielectric 1 | CR-370HR-2x1080 | 4,49mil | 4,1 |
| 12 | | Inner Layer 5 | Copper | 0,71mil | |
| 13 | | Dielectric 4 | PP-370HR-1086_67 | 3,50mil | 3,88 |
| 14 | | Bottom Layer | Copper | 2,01mil | |
| 15 | | Bottom Solder | LPI-Green | 0,39mil | 3,5 |
| 16 | | Bottom Overlay | | | |
| 17 | | Bottom Paste | | | |
| | Height : 63,02mil | | | | |

## A.4 PCB TRACE WIDTHS AND CLEARANCE

- EVB-LAN9662 End-Node module thickness: 1.2 mm ±10%
- EVB-LAN9662-Carrier board thickness: 1.6 mm ±10%
- Characteristic impedance single-ended: 50Ω or 60Ω
- Characteristic impedance differential USB signals: 90Ω
- Single-ended trace width: 150 µm and 125 µm
- Single-ended trace-to-trace clearance: 400 µm
- 100 ohm differential trace width: 125 µm
- 100 ohm differential trace-to-trace spacing: 220 µm

**TABLE A-3: NET IMPEDANCE AND LENGTH MATCHING**

| Net Group Name | Type | Impedance | Length Matching | Tolerance (mm) | Max Vias | Via Type | Layers | Notes |
|---|---|---|---|---|---|---|---|---|
| Clock | Single-ended | 50Ω | None | — | 4 | All | All | — |
| SI | Single-ended | 50Ω | None | — | 4 | All | All | Daisy-chain |
| DDR_ CMD_LANE | SE/DIFF | 60Ω | Within lane | 1 | 2 | All | All | See Note 2 |
| DDR_ DQ_LANE0 | SE/DIFF | 60Ω | Within lane | 1 | 2 | All | All | See Note 2 |
| DDR_ DQ_LANE1 | SE/DIFF | 60Ω | Within lane | 1 | 2 | All | All | See Note 2 |
| USB | Differential | 90Ω | P/N only | 1 | 2 | All | All | — |
| DiffClock | Differential | 100Ω | P/N only | 1 | 2 | All | All | — |
| SerDes | Differential | 100Ω | P/N only | 0 | 2 | — | Outer | See Note 1 |
| Sense | Analog | — | — | — | — | All | All | — |
| Power | Power | — | — | — | — | — | - | — |
| Static | Single-ended | — | — | — | — | — | All | See Note 3 |
| Unspecified | Single-ended | 60Ω | — | — | — | — | All | See Note 4 |

**Note 1:** Differential signal on outer layers.

**2:** DDR SE impedance 60Ω between devices.

**3:** No impedance => 4mil trace on any layer.

**4:** Any unspecified nets should be routed as 60Ω.

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