EVB-LAN8841 Evaluation Board User's Guide

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-LAN8841 Evaluation Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN8841 as a development tool for the LAN8841 Gigabit Ethernet Transceiver with RGMII. The manual layout is as follows:

- **Chapter 1. "Overview"** – This chapter provides a brief description of the EVB-LAN8841 evaluation board.
- **Chapter 2. "Getting Started"** – This chapter provides information about setup and operation of the EVB-LAN8841.
- **Chapter 3. "Hardware Configuration"** – This chapter provides information about setup of the EVB-LAN8841 hardware.
- **Chapter 4. "PTP4L Demo Using EVB-LAN8841"** – This chapter provides a demonstration of PTP4L using the EVB-LAN8841.
- **Appendix A. "Schematics"** – This appendix shows the EVB-LAN8841 schematics.
- **Appendix B. "Bill of Materials"** – This appendix includes the EVB-LAN8841 bill of materials.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file.o`*`, where `*`file`*` can be any valid filename`
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Compilers** – The latest information on Microchip C compilers, assemblers, linkers and other language tools. These include all MPLABCC compilers; all MPLAB assemblers (including MPASM™ assembler); all MPLAB linkers (including MPLINK™ object linker); and all MPLAB librarians (including MPLIB™ object librarian).
- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICkit™ 2 and 3.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003442B (05-17-23)	**Chapter 2. "Getting Started"**	Added an important note under Figure 2-1.
	Chapter 4. "PTP4L Demo Using EVB-LAN8841"	Added this new chapter.
DS50003442A (11-17-22)	Initial release	

Chapter 1. Overview

1.1 INTRODUCTION

The EVB-LAN8841 evaluation board is a plug-in daughter card that interfaces directly with a mating Microchip host processor or controller board, such as the SAMA5D3 Ethernet Development System (EDS) board, as well as a USB bridge board (EVB-LAN7801-EDS) and a PCIe® bridge board (EVB-LAN7431-EDS). It features the LAN8841, a highly integrated networking device that incorporates a 10/100/1000BASE-T physical layer transceiver (PHY). The board's PHY port is connected to an RJ45 Ethernet jack with integrated magnetics, and the PHY's RGMII connections are brought out to a high-speed (HS) multi-pin connector.

Together, the EVB-LAN8841 and the EDS base board provide a highly flexible platform for evaluation of PHY features using their internal memory registers and the management interface.

This document describes the EVB-LAN8841 setup and its user interface features.

A simplified block diagram of the board is shown in Figure 1-1.

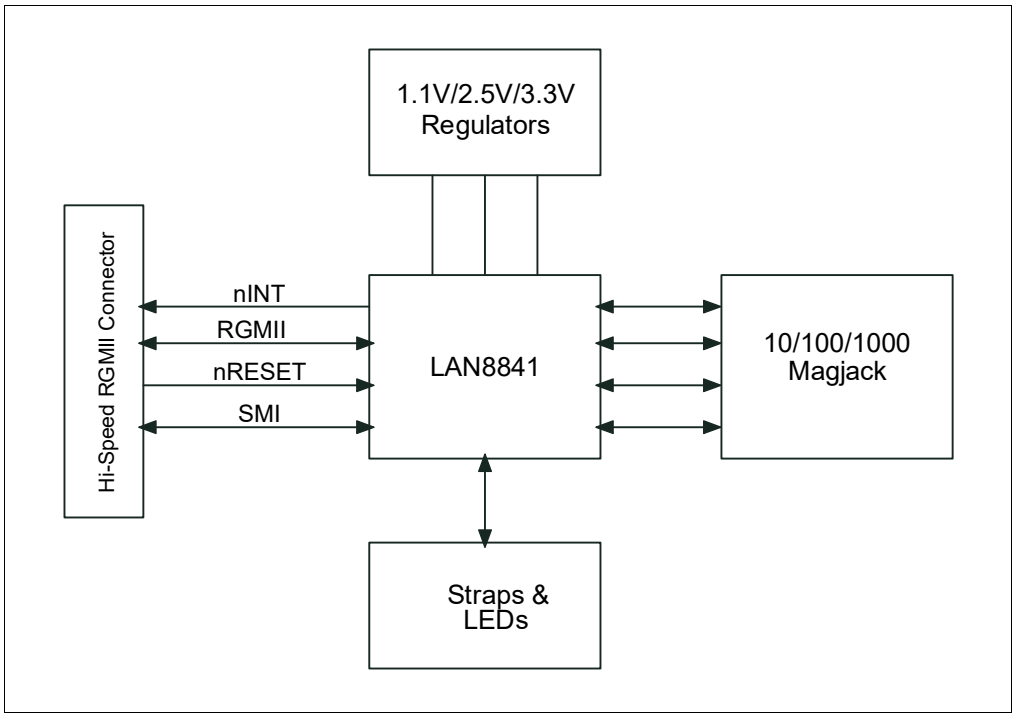
1.2 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *LAN8841 Data Sheet*
- *EVB-LAN8841 Schematics*
- *LAN8841 Hardware Design Checklist*
- *SAMA5D3 Ethernet Development System Schematics*
- *SAMA5D3 Ethernet Development System Board User's Guide*
- *EVB-LAN7801 Ethernet Development System Schematics*
- *EVB-LAN7801 Ethernet Development System User's Guide*
- *EVB-LAN7431 Ethernet Development System Schematics*
- *EVB-LAN7431 Ethernet Development System User's Guide*
- *MIC33153 Data Sheet*
- *MIC5207 Data Sheet*

1.3 BLOCK DIAGRAM

FIGURE 1-1: EVB-LAN8841 BLOCK DIAGRAM



Chapter 2. Getting Started

2.1 INTRODUCTION

The EVB-LAN8841 evaluation board is designed as a plug-in card to interface directly with a mating Microchip host processor or controller board, such as the SAMA5D3-EDS board, that supplies full power and provides full register access and configuration via MDIO/MDC bus management.

2.2 DEFAULT JUMPER SETTINGS

The EVB-LAN8841 ships with the necessary jumpers installed for basic operation.These are:

- J1: Shunt installed between pins [2-3]
- J2: Shunt installed between pins [2-3]
- J4: Shunt installed between pins [1-2]

See Figure 3-1 for an image of these default shunt installations.

See Section 3.4 "Connectors" for a full list of connector/header descriptions and directions for use.

2.3 POWER SOURCE

The EVB-LAN8841 can be completely bus-powered from its mating Microchip host processor or control board. Alternatively, the EVB-LAN8841 can be powered with an external 3.3V supply.

Refer to Figure 3-1 and the board schematics in Figure A-2 for details.

2.3.1 EDS-Powered Operation

For EDS-powered operation, J1 needs a jumper on the pins [2-3], and J2 needs a jumper on the VDDIO pins [2-3] as shown in Figure 3-1.

2.3.2 External-Powered Operation

For external-powered operation, J1 needs a jumper on pins [1-2], while J2 needs a jumper on either 2.5V pins [1-2] or VDDIO pins [2-3]. An external 3.3V power source should be connected to TP1.

2.4 CLOCK

The EVB-LAN8841 utilizes a 25 MHz crystal to generate input reference clock for the LAN8841 device. Refer to Figure A-3 for details.

2.5 RESET CIRCUIT

2.5.1 Power-On Reset—EDS Reset

The SAMA5D3-EDS can provide the LAN8841 Reset when a jumper is placed on EVB-LAN8841, J4 pins [1-2] (EDS Reset).

2.5.2 Manual Reset

The EVB-LAN8841 SW1 can be pressed and released to provide LAN8841 Reset after device power-up. The EVB-LAN8841 J4 must have a jumper between pins [2-3] (Reset) to utilize this manual Reset.

2.6 USING THE EVB-LAN8841

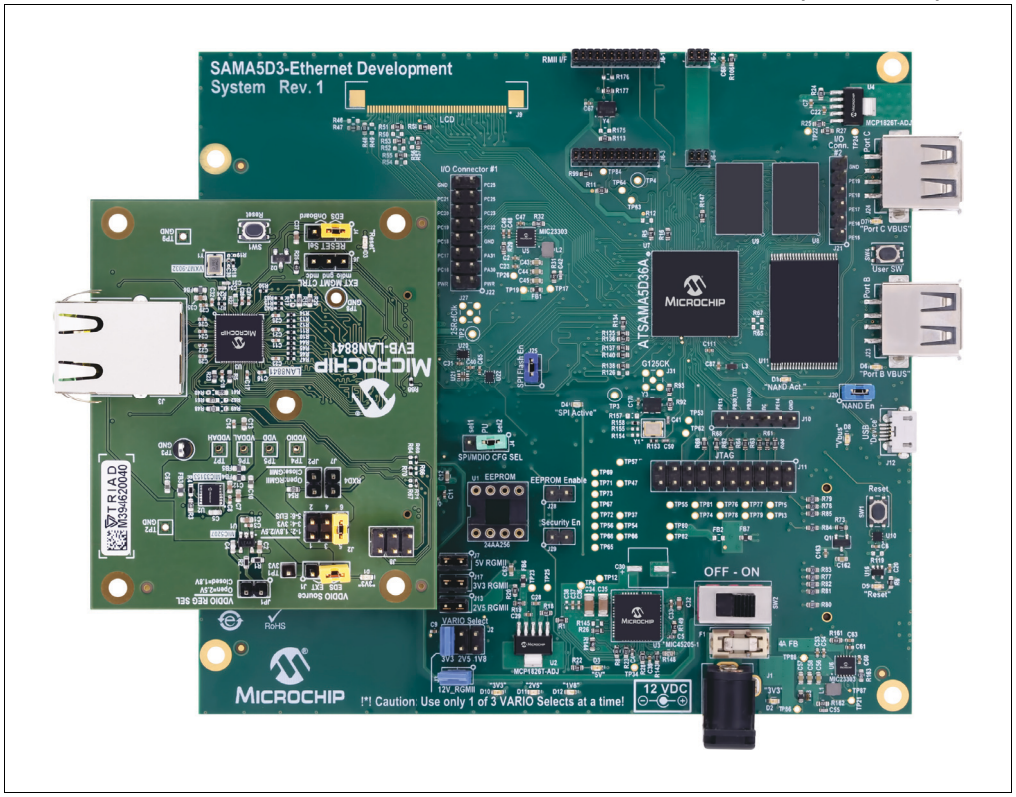
2.6.1 With SAMA5D3-EDS

The EVB-LAN8841 directly plugs into a mating Microchip host controller or processor board, such as the SAMA5D3-EDS, that can deliver full power and provide full register access and configuration via MDIO/MDC bus management.

Together, the EVB-LAN8841 and the SAMA5D3-EDS enable 10/100/1000 Mbps Ethernet traffic through RGMII and the PHY port of the EVB-LAN8841 device, with the RGMII port connecting to the SAMA5D3 processor and the PHY port connecting via copper Ethernet cable (CAT-5 UTP or better) to external Ethernet devices.

All LAN8841 registers are accessible via MDIO/MDC bus management from the SAMA5D3-EDS board, enabling full evaluation and firmware for all LAN8841 features. MDIO/MDC pins are also available for external control at header J6. Refer to the SAMA5D3 Ethernet Development System Board User's Guide. Figure 2-1 shows the EVB-LAN8841 connected to the SAMA5D3-EDS board.

FIGURE 2-1: EVB-LAN8841 AND SAMA5D3-EDS BOARD (TOP VIEW)



Note: It is important to note that if RGMII is used with the SAMA5D3-EDS, the EVB-LAN8841 must be configured so that the R43 resistor is DNP.

2.6.2 With EVB-LAN7801-EDS and EVB-LAN7431-EDS

To work with EVB-LAN7801-EDS and EVB-LAN7431-EDS with the EVB-LAN8841, a specific EEPROM image for LAN7801/LAN7431 should be programmed onto the EVB baseboard. This is necessary to ensure that RGMII TXC and RXC delays settings are appropriately configured, and the 125 MHz clock source is enabled internal to the LAN7801/LAN7431.

A `readme` file that describes the detailed configuration and the binary files used to program the EEPROM on the bridge boards are available on the EVB-LAN8841 evaluation board product page.

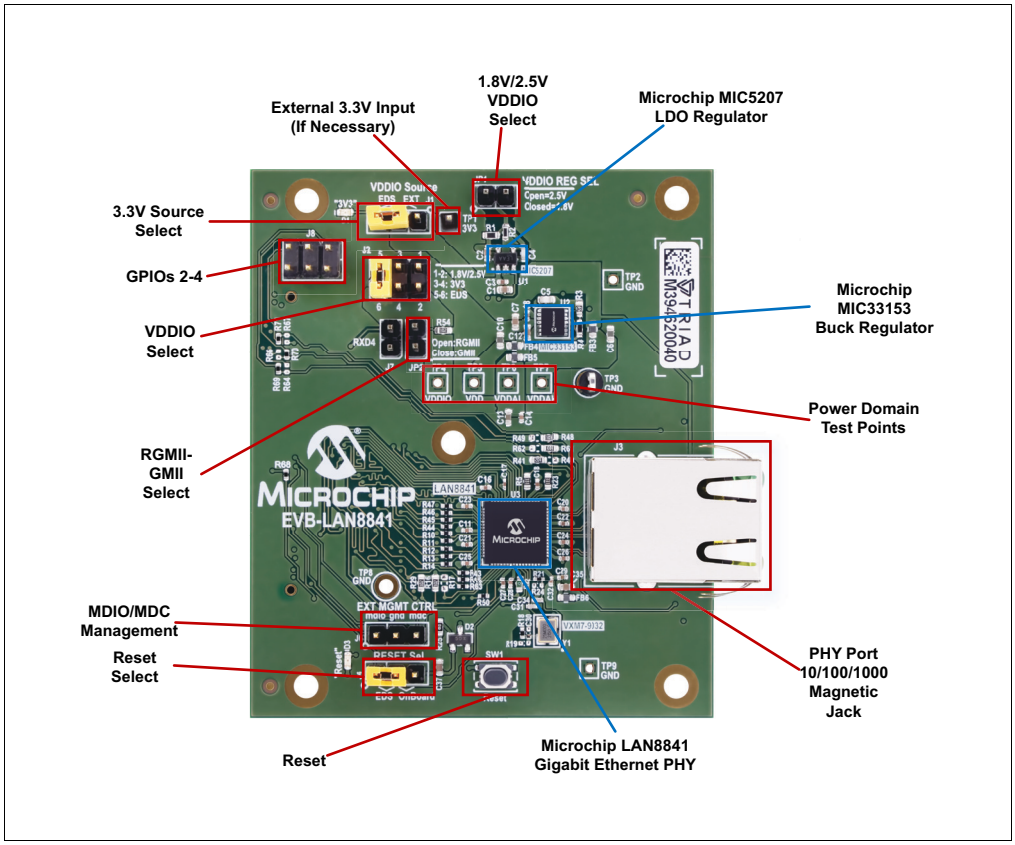
NOTES:

Chapter 3. Hardware Configuration

3.1 HARDWARE CONFIGURATION OPTIONS

Figure 3-1 shows the top view of the EVB-LAN8841.

FIGURE 3-1: EVB-LAN8841 TOP VIEW WITH CALLOUTS



3.2 PHY PORT

PHY port (J3) supports 10BASE-T/100BASE-TX/1000BASE-T with both auto-negotiation enabled and Auto-MDI/MDI-X enabled as the power-up defaults.

3.3 TEST POINTS

Table 3-1 lists the test points on the EVB-LAN8841:

TABLE 3-1: TEST POINTS

Test Point	Description
TP1	3V3
TP2	GND
TP3	GND
TP4	VDDIO
TP5	VDD
TP6	VDDAL
TP7	VDDAH
TP8	GND
TP9	GND

3.4 CONNECTORS

Table 3-2 lists the connectors on the EVB-LAN8841:

TABLE 3-2: CONNECTORS

Connector Reference Designator	Function	Options
J1	VDDIO Source Selection	Shunt pins [1-2]: External VDDIO applied on TP1. Shunt pins [2-3]: VDDIO comes from MAC (EDS).
J2	VDDIO Voltage Selection	Shunt pins [1-2]: VDDIO is from MAC. Shunt pins [3-4]: VDDIO is 3.3V. Shunt pins [5-6]: VDDIO is 1.8V/2.5V.
J3	Ethernet RJ45 Connector	N/A
J4	Reset Select	Shunt pins [1-2]: Reset comes from MAC (EDS) device. Shunt pins [2-3]: Reset comes from local reset button (SW1).
J5	Board to Board Connector	N/A
J6	MDIO Probe Header	For probe only. Do not connect shunt across any pins on J6. Pin 1: MDC Pin 2: GND Pin 3: MDIO
J7	RXD4 Header	In RGMII mode, this pin must remain open. In GMII mode, these pins must be shunted.

TABLE 3-2: CONNECTORS (CONTINUED)

Connector Reference Designator	Function	Options
J8	GPIO Test Reference	GPIO/IEEE1588 (PTP) Reference Pins. These GPIOs are pin-shared with unused LED pins. These GPIOs can be configured as a PTP Reference Clock Input, a PTP Reference Clock Output or a GPIO depending on register settings. Pin 1: GPIO2 Pin 3: GPIO3 Pin 5: GPIO4 Do not connect a shunt between J8 pins.
JP1	1.8V/2.5V VDDIO Select	Open: VDDIO is 2.5V. Closed: VDDIO is 1.8V.
JP2	RGMII/GMII Configuration Strap	Open: LAN8841 in RGMII mode Closed: LAN8841 in GMII/MII mode

NOTES:

Chapter 4. PTP4L Demo Using EVB-LAN8841

4.1 CONNECTION SETUP

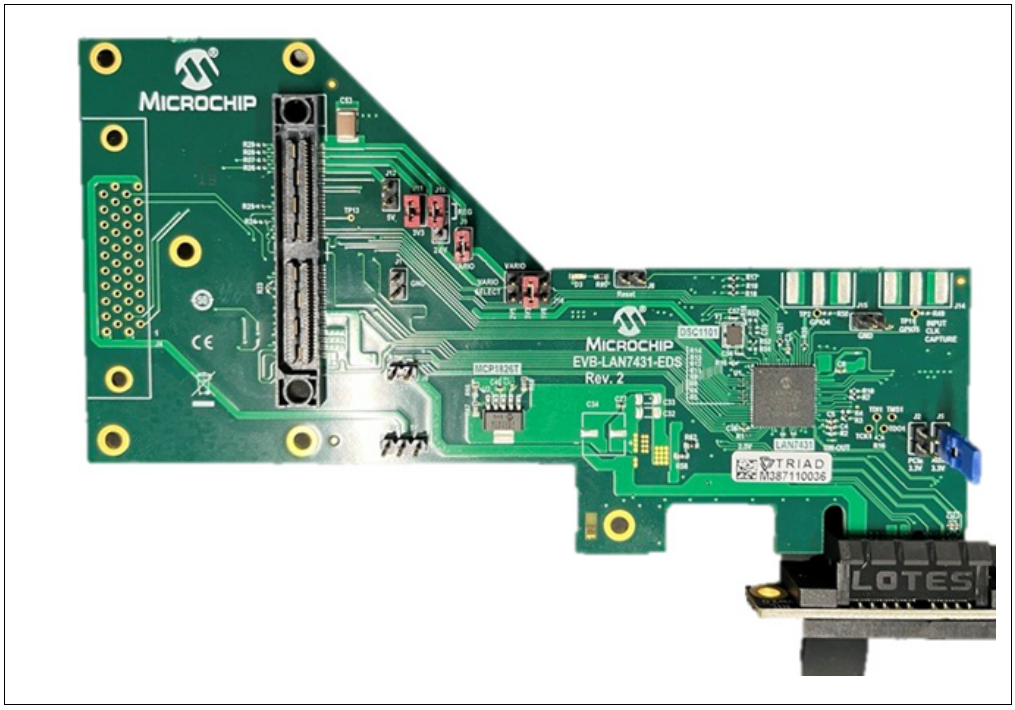
4.1.1 PTP Demo Board Configuration

Note: The LAN8841 and LAN7431 (EDS) are used together in this demo. Specific steps or settings are slightly different if a different EDS platform is used.

To configure the PTP demo board:

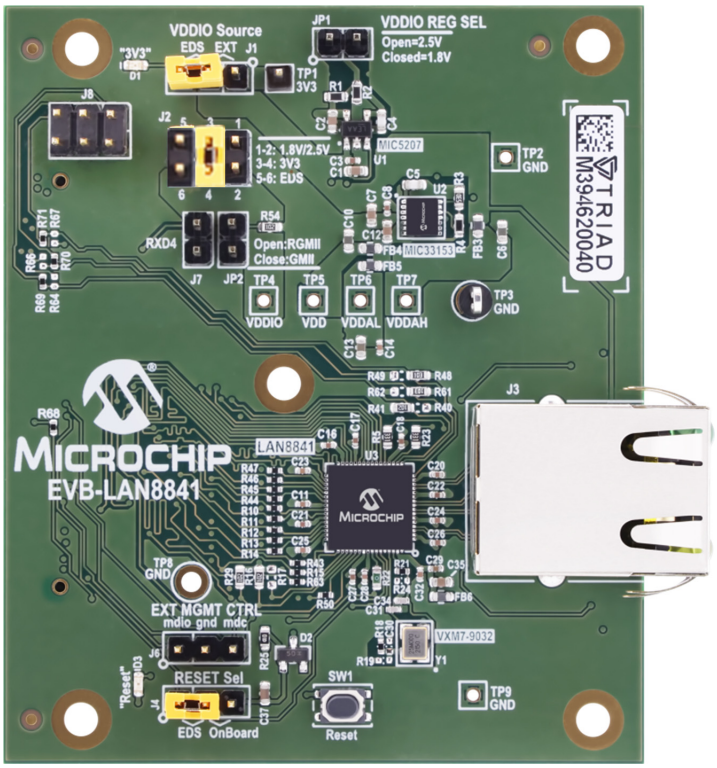
1. Verify the straps on LAN7431:
   - Jumpers J5, J9, J10 (shunt pins 1-2, hence VARIO = 3.3V) and J11 are mounted.
   - Middle jumper of J16 is mounted.

FIGURE 4-1: LAN7431 STRAPS



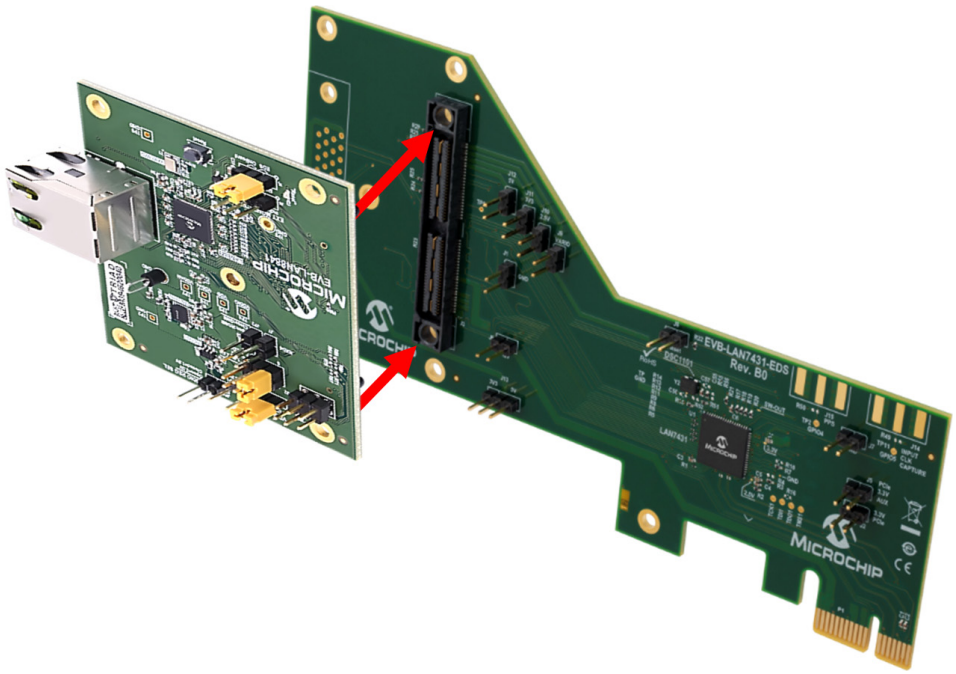
2. Verify straps on LAN8841:
   - Jumpers J1 (shunt pins 2-3), J2 (shunt pins 3-4) and J4 (shunt pins 1-2) are mounted.

FIGURE 4-2: LAN8841 STRAPS



3. Plug the EVB-LAN8841 into the RGMII interface of the EVB-LAN7431 using SAMTEC connector.

FIGURE 4-3: CONNECTING EVB-LAN8841 TO EVB-LAN7431



Note: The EVB-LAN7431 shown in this illustration is not the latest revision of the board.

4. Connect the LAN7431 to a host computer's PCIe bus using a PCIe extension cable (Figure 4-4).

FIGURE 4-4: PCIE® EXTENSION CABLE

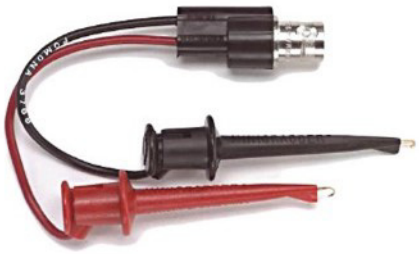
4.1.2 Calnex Paragon-X Connections

1. Connect to the EVB J8 header's pin 1 (GPIO2) to the Upper AUX port on the front panel of the Paragon-X using the Paragon-X supplied cable (black BNC) (Figure 4-5).

FIGURE 4-5: CALNEX-SUPPLIED CABLE

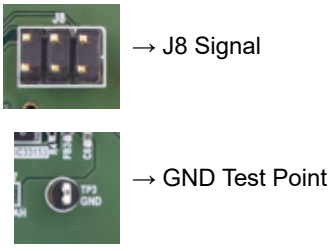
The black BNC coaxial connector can be adapted to the 0.100 stake header J8.1 using a female BNC-Microclip adapter (see Figure 4-6).

FIGURE 4-6: FEMALE BNC-MICROCLIP ADADPTER



The TP3 GND test point can be connected to the BNC cable's outer shield (black clip of the BNC-Microclip). See Figure 4-7 for pictures of the J8 signal header and the GND test point.

FIGURE 4-7: J8 SIGNAL HEADER AND GND TEST POINT



2. Connect the EVB-LAN8841 RJ45 port to the Paragon-X Ethernet Port 1 (see Figure 4-8).

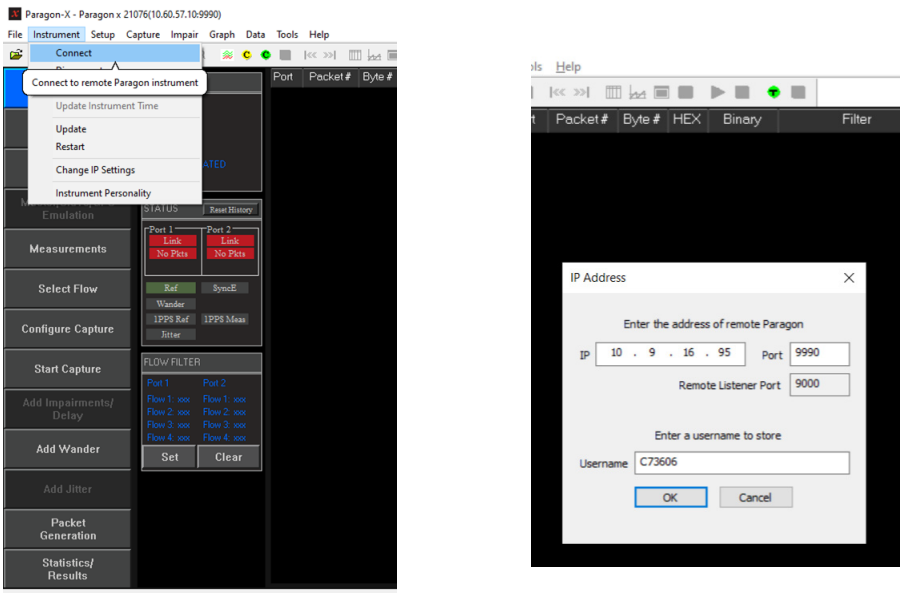
FIGURE 4-8: PARAGON-X

Note: Use a short CAT5e (<1.5m) to use the same compensation values and measure approximately the same path delays as shown in the example in **Section 4.7 “Confirming Offset from Master in PTP4L”**.

4.1.3 Verifying Control of Paragon

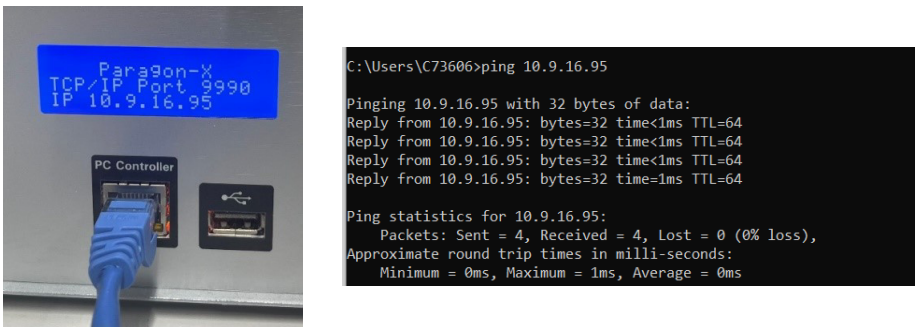
1. Connect a PC/laptop to the Paragon-X “PC Controller” port with an RJ45 cable.
2. Launch the Paragon-X application on your computer. Click **Connect** in the **Instrument** tab to pair with the Paragon-X. Enter the Paragon-X IP address observed on its control display when prompted (see Figure 4-9).

FIGURE 4-9: PARAGON-X APPLICATION VIEW



3. Set the computer’s IP address to a number that is within the same subnet as the Paragon-X IP address (or vice versa).
4. Issue a ping command from your computer to the Paragon-X to confirm that the devices are communicating over the control port. Replies indicate that the command works. (See Figure 4-10.)

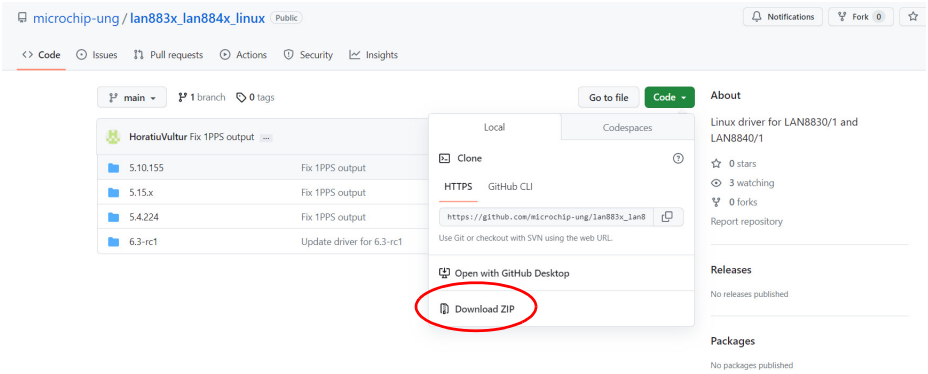
FIGURE 4-10: PARAGON-X DISPLAY PORT AND COMMAND PROMPT



4.2 CUSTOM DRIVER INSTALLATION

1. Extract the custom driver source code from the zip file provided by Microchip at: https://github.com/microchip-ung/lan883x_lan884x_linux

FIGURE 4-11: DRIVER SOURCE CODE GITHUB LINK



2. After extracting the source code, copy the files to their default path within the Kernel that is used. (It is recommend to use 6.3-rc1 because it is where most of this demo was tested.)
   a) Copy and overwrite.

`net-next-6.3-rc1/drivers/net/ethernet/microchip/lan743x_main.h`

   b) Copy and overwrite.

`net-next-6.3-rc1/drivers/net/ethernet/microchip/lan743x_main.c`

   c) Copy and overwrite.

`net-next-6.3-rc1/include/linux/micrel_phy.h`

   d) Copy and overwrite.

`net-next-6.3-rc1/drivers/net/phy/micrel.c`

3. Compile drivers at the root of the Linux source tree.
   a) `make drivers/net/ethernet/microchip/lan743x.ko`
   b) `make drivers/net/phy/micrel.ko`

Note: Errors should not be seen.

4. Unload the existing drivers.
   a) `sudo rmmod lan743x`
   b) `sudo rmmod micrel`

Note: Micrel module may not be loaded at default.

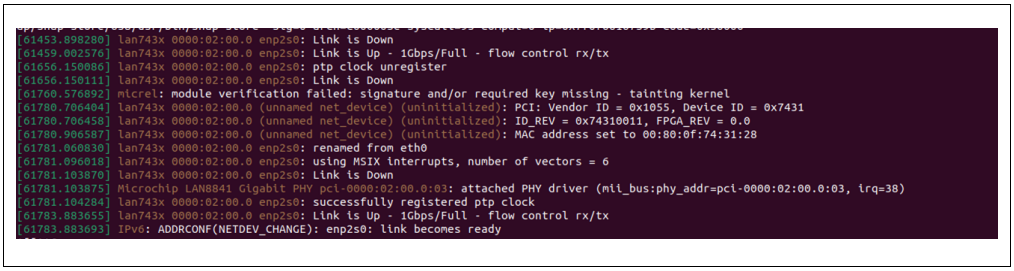
5. Load the new drivers in order.
   a) `sudo insmod drivers/net/phy/micrel.ko`
   b) `sudo insmod drivers/net/ethernet/microchip/lan743x.ko`

   Note: Rebooting the PC loads the original in-kernel drivers. Hence, after reboot, repeat steps 4 and 5.

6. To see the driver kernel log, open a separate terminal window then run `sudo dmesg` to see if the drivers are loaded correctly, as well as the status of link up/link down, speed, duplex, and more. Manufacturer and device name could vary. (See Figure 4-12.)

   Note: For every new driver patch, all the steps in **Section 4.2 “Custom Driver Installation”** should be followed.

FIGURE 4-12: DMESG LOG

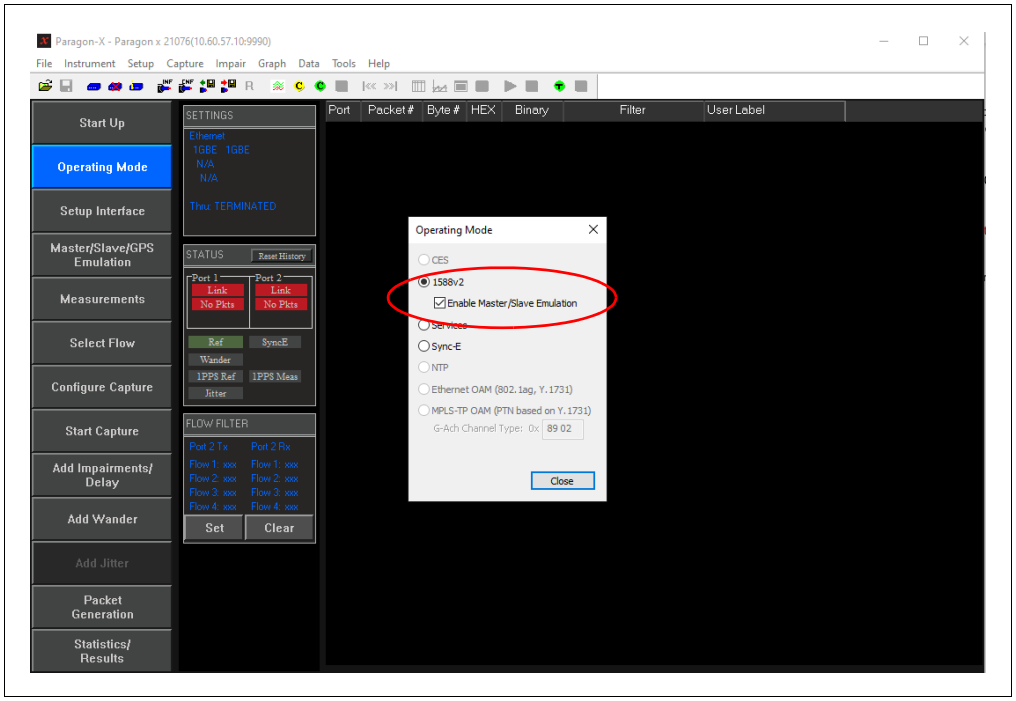


4.3 CALNEX PTP MASTER SETUP

Only the settings that are required to change are shown in the following. In the Paragon-X Control GUI for the Calnex, configure the following:

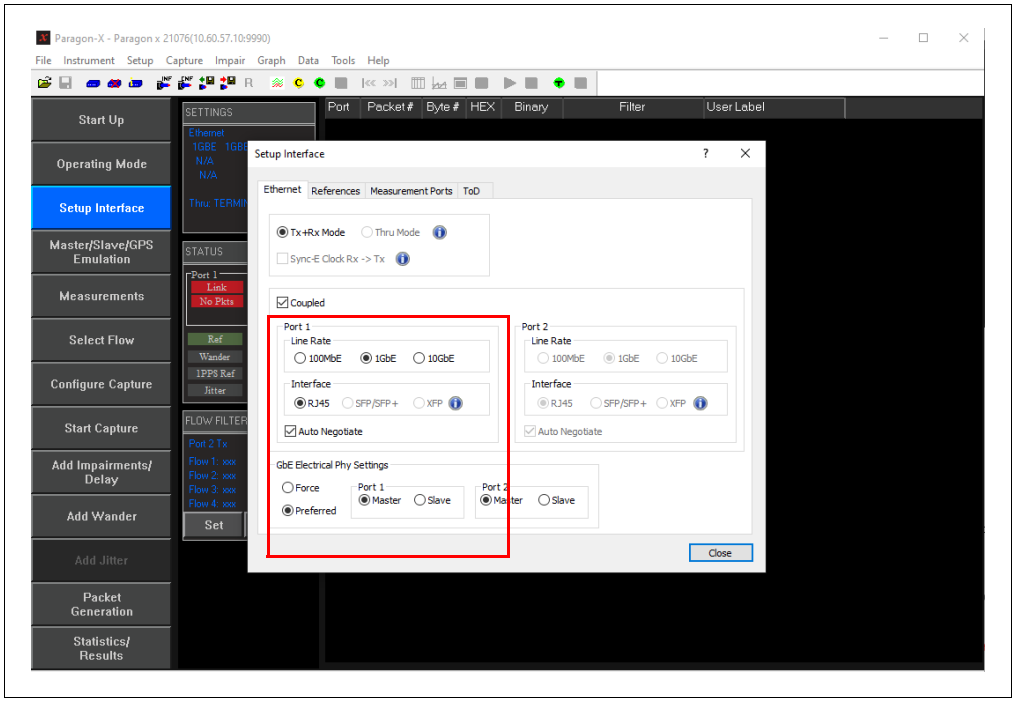
1. Select the “Operation Mode” option and change the operating mode to “1588v2” and enable the “Master/Slave Emulation” check box as in Figure 4-13.

FIGURE 4-13: OPERATING MODE



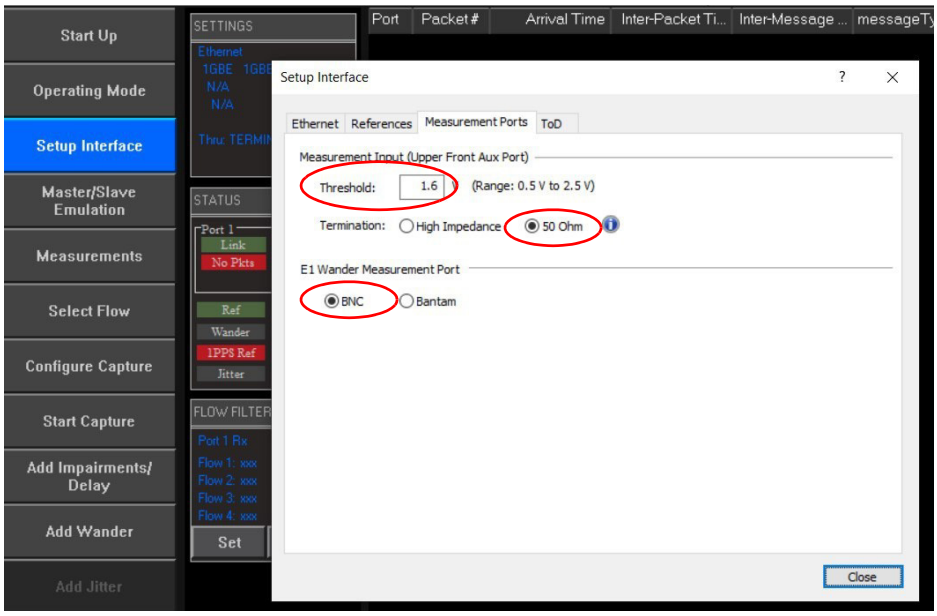
2. Select the "Setup Interface" option to set up the interface settings. This opens the Setup Interface window.
   a) In the **Ethernet** tab, select "1GbE" port speed and "RJ45" interface. Ensure that the "Auto Negotiate" check box is enabled and that "Preferred" is selected along with both ports chosen as "Master". (See Figure 4-14.)

FIGURE 4-14: SETUP INTERFACE>ETHERNET



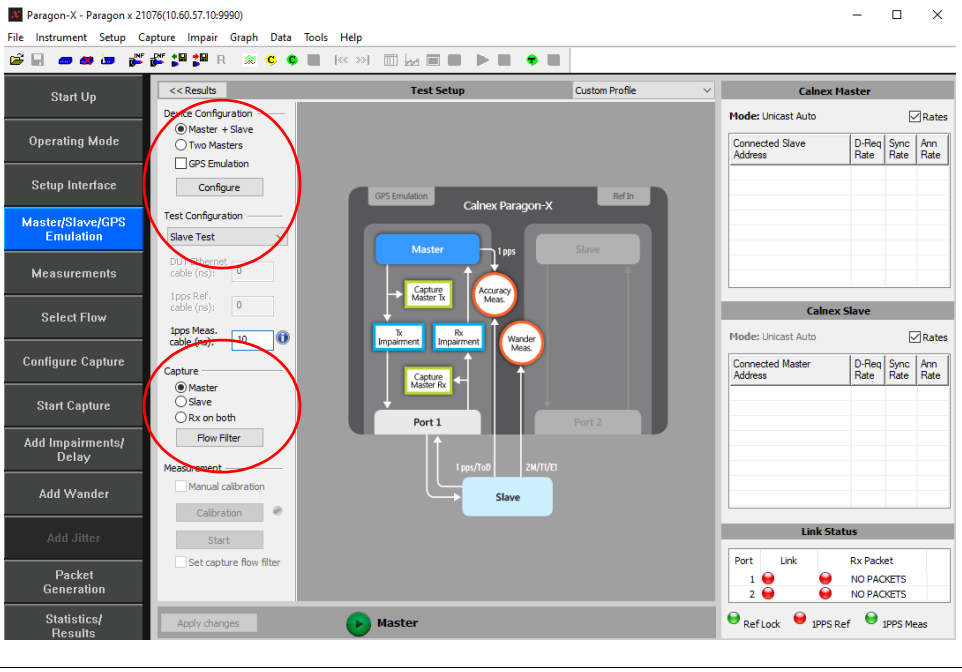
   b) In the **Measurement Ports** tab, set the threshold voltage to 1.6V. Ensure that the "Termination" field is set to "50 Ohm" and the "E1 Wander Measurement Port" is set to "BNC". (See Figure 4-15.)

FIGURE 4-15: SETUP INTERFACE>MEASUREMENTS PORTS



3. From the “Master/Slave Emulation” option, set the “Device Configuration” to “Master + Slave” and “Test Configuration” to “Slave test” (to test DUT as a slave). Make sure the “Capture” field is set to “Master”. (See Figure 4-16.)

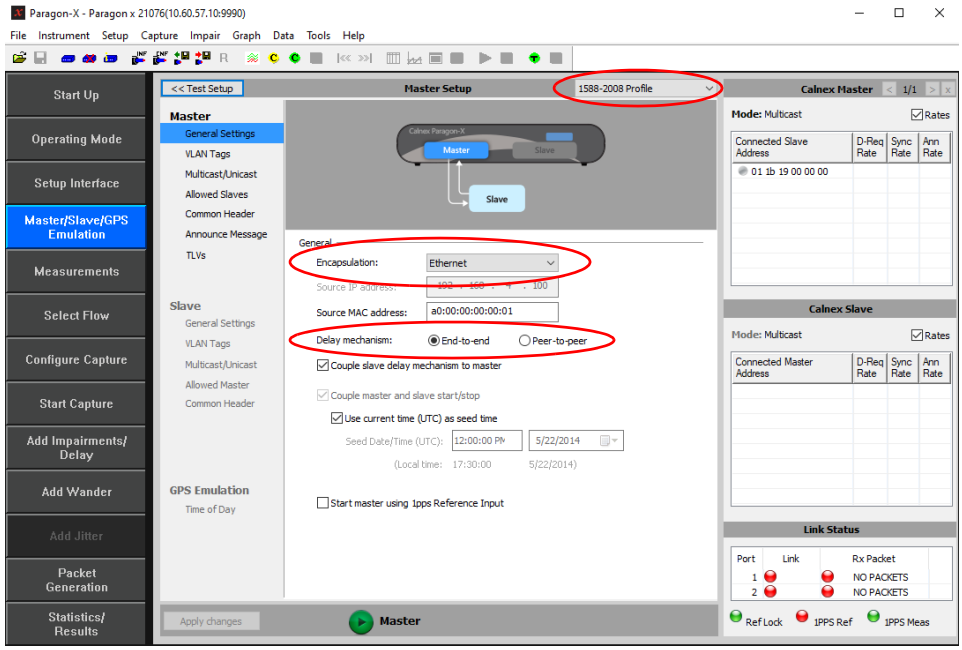
FIGURE 4-16: MASTER/SLAVE EMULATION OPTION



4. Click the **Configure** button in Figure 4-16 to view the Master Setup window (Figure 4-17). At the top of the window, change the test profile to “1588-2008 Profile” as highlighted in Figure 4-17.

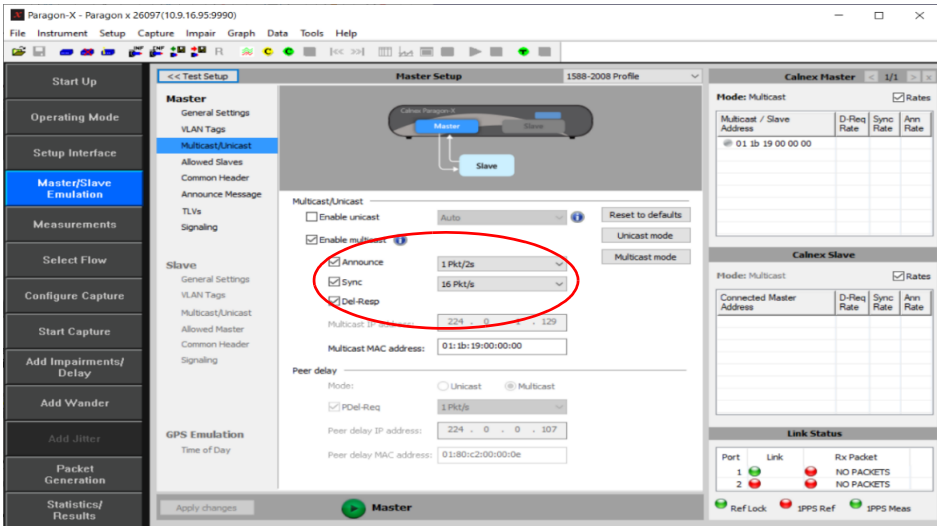
5. Configure the Master.
   a) In the "General Settings" section, set "Encapsulation" to "Ethernet" and "Delay Mechanism" to "End-to-end".

FIGURE 4-17: MASTER SETUP WINDOW



   b) In the "Multicast/Unicast" section, enable the "Enable multicast", "Announce", "Sync", and "Del-Resp" check boxes. Ensure that the packet rates match. (See Figure 4-18.)

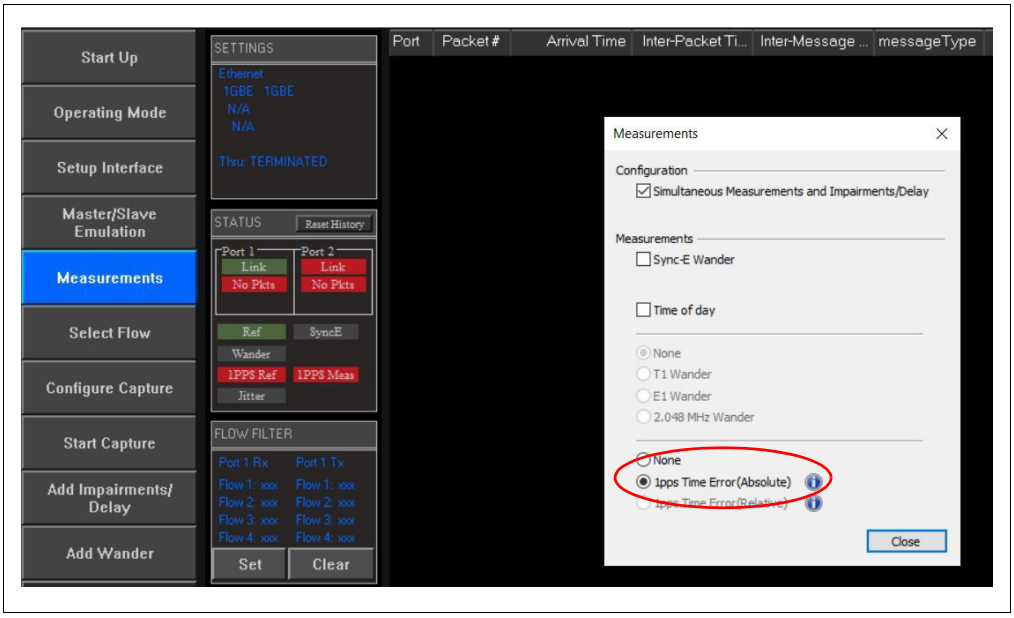
FIGURE 4-18: MASTER SETUP>MULTICAST/UNICAST



   c) Keep the configurations in the "Common Header" and "Announce Message" sections at default.

6. From the "Measurements" option, select the "1pps Time Error (Absolute)" setting. (See Figure 4-19.)

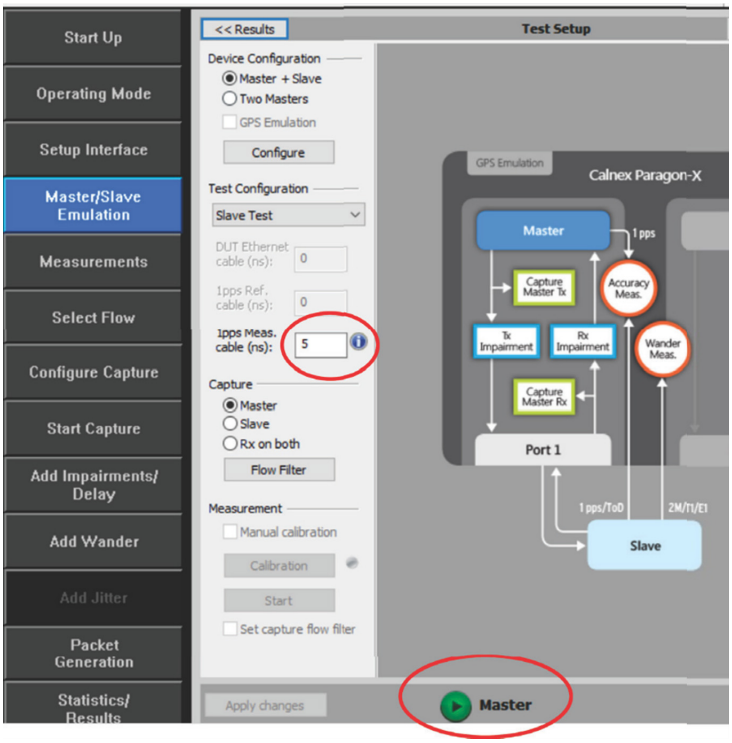
FIGURE 4-19: MEASUREMENTS WINDOW



Note: Before clicking the play button, enter the delay compensation for the 1PPS measurement cable (BNC cable). Paragon-X recommends ~5 nanoseconds/meter of BNC.

7. Return to the “Master/Slave Emulation” setup panel and start the Master emulation by clicking the green play button as shown in Figure 4-20. It turns red after clicking it.

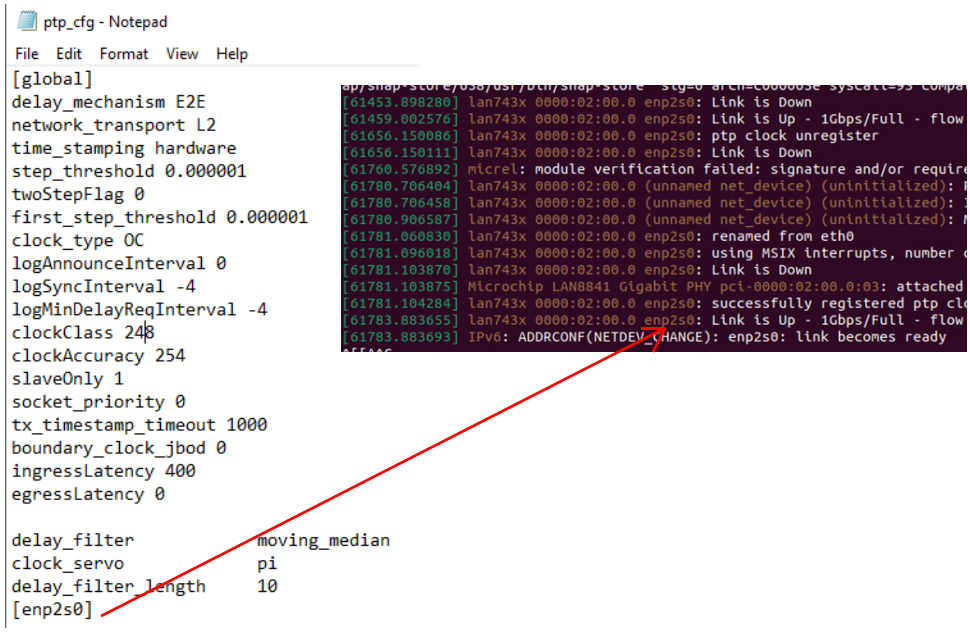
FIGURE 4-20: STARTING MASTER EMULATION



4.4 CONFIGURING THE PTP PORT AND PTP APPLICATION

1. Write a static configuration file out to specify the 1588 clock setup. In the `ptp_cfg` file in Example 4-1, the `[enp2s0]` designation refers to how the device enumerates in your console. A `dmesg` log highlights this relationship.

EXAMPLE 4-1: PTP_CFG FILE AND DMESG CONSOLE OUTPUT



Note 1: In this example, the device under test (DUT) enumerates as whatever NIC-capable device is the nearest connection in the system. In this case, a system with the LAN8841 plugs into a LAN7431 bridge card, which then connects to the host computer. Since the LAN7431 is the closest to the PC, it is the device where the commands are issued.

2: The ingress value may need to be adjusted slightly for a perfectly centered PPS signal.

2. Set the IP address of the enumerated device.

```
# sudo ip addr add dev enp2s0 192.168.10.1/24
```

3. Configure the device as an uplink.

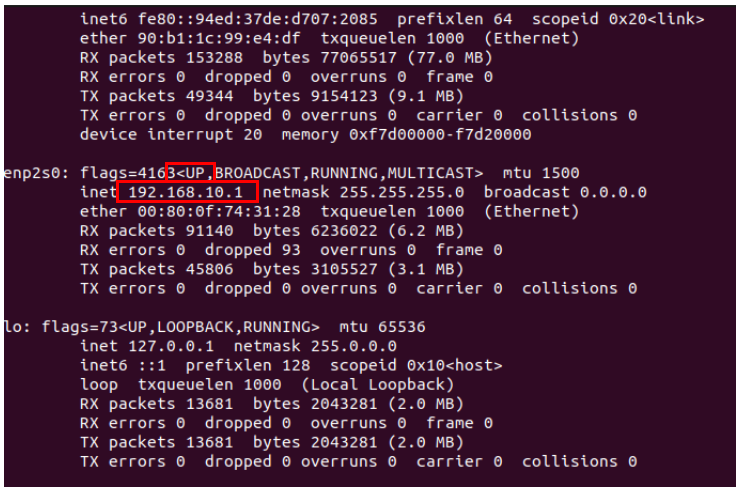
```
# sudo ip link set enp2s0 up
```

4. Check the link status. The device should display the set IP and indicate an uplink. (See Figure 4-21.)

```
# ifconfig
```

Note: Ensure that the 1G link is always connected and the link remains up. If the link drops during testing, then the 1PPS output disappears and cannot be re-enabled. (A PC restart would be required.)

FIGURE 4-21: IFCONFIG OUTPUT

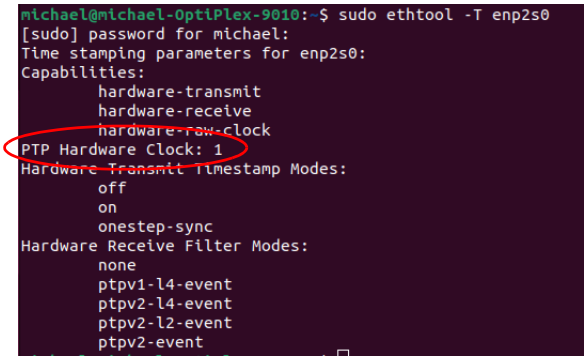


4.5 ENABLING THE 1PPS TIMING OUTPUT FROM LAN8841

1. Use ethtool to identify the PTP Hardware Clock (PHC) ID (see Figure 4-22). Note that this number can vary and could be 1, 2, 3, and so on.

```
# sudo ethtool -T enp2s0
```

FIGURE 4-22: PHC ID



2. Starting from the Kernel root, navigate to the directory `/tools/testing/selftests/ptp`.
3. Compile the testptp application.

```
# sudo make
```

4. Check for the testptp object (see Figure 4-23).

FIGURE 4-23: TESTPTP OBJECT

5. Navigate back to the root of the kernel directory and enable the 1PPS GPIO pin with the testptp object. (If the PHC ID is 1, then the active PHC is ptp1. The ID can be any number.)

```
# sudo tools/testing/selftests/ptp/testptp -d /dev/ptp1 -L 2,2
```

6. Set the duty cycle and pulse width for the 1PPS signal.

```
# sudo tools/testing/selftests/ptp/testptp -d /dev/ptp1 -p 1000000000
-w 200000000
```

4.6 STARTING PTP4L

1. Run the EVB-LAN8841 as a PTP follower node with the following command (see Figure 4-24):

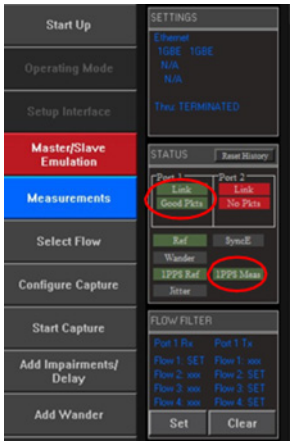
```
# sudo ptp4l -msf ptp_cfg
```

FIGURE 4-24: PTP4L OUTPUT

```
ptp4l[13392.296]: rms    2 max    3 freq  -8237 +/-   3 delay  7024 +/-   0
ptp4l[13393.296]: rms    2 max    4 freq  -8236 +/-   4 delay  7024 +/-   1
ptp4l[13394.296]: rms    3 max    5 freq  -8240 +/-   4 delay  7024 +/-   1
ptp4l[13395.296]: rms    2 max    4 freq  -8235 +/-   2 delay  7025 +/-   0
ptp4l[13396.296]: rms    2 max    3 freq  -8238 +/-   2 delay  7024 +/-   0
ptp4l[13397.296]: rms    2 max    4 freq  -8235 +/-   2 delay  7024 +/-   1
ptp4l[13398.296]: rms    2 max    3 freq  -8233 +/-   2 delay  7024 +/-   1
ptp4l[13399.296]: rms    2 max    3 freq  -8235 +/-   3 delay  7024 +/-   0
ptp4l[13400.296]: rms    2 max    5 freq  -8230 +/-   3 delay  7024 +/-   0
ptp4l[13401.296]: rms    2 max    3 freq  -8232 +/-   3 delay  7023 +/-   0
ptp4l[13402.296]: rms    2 max    3 freq  -8234 +/-   2 delay  7024 +/-   0
ptp4l[13403.296]: rms    1 max    3 freq  -8233 +/-   2 delay  7024 +/-   0
ptp4l[13404.296]: rms    2 max    4 freq  -8231 +/-   3 delay  7024 +/-   0
ptp4l[13405.296]: rms    1 max    3 freq  -8232 +/-   2 delay  7024 +/-   0
ptp4l[13406.296]: rms    2 max    3 freq  -8234 +/-   3 delay  7024 +/-   1
Sptp4l[13407.296]: rms    1 max    3 freq  -8233 +/-   2 delay  7023 +/-   1
ptp4l[13408.296]: rms    3 max    5 freq  -8228 +/-   3 delay  7023 +/-   0
ptp4l[13409.296]: rms    1 max    2 freq  -8229 +/-   2 delay  7024 +/-   1
ptp4l[13410.296]: rms    2 max    3 freq  -8228 +/-   2 delay  7024 +/-   1
ptp4l[13411.296]: rms    2 max    4 freq  -8231 +/-   3 delay  7024 +/-   0
ptp4l[13412.296]: rms    2 max    3 freq  -8232 +/-   2 delay  7024 +/-   1
ptp4l[13413.296]: rms    2 max    5 freq  -8228 +/-   4 delay  7024 +/-   0
```

2. Select *Flow>Capture Packets* to perform a dummy capture of PTP packets.
3. Check that there are "Good" PTP packets and the 1PPS output from DUT is valid at the Paragon-X PTP Master. See Figure 4-25.

FIGURE 4-25: PARAGON-X STATUS



Note: Circled states indicate valid PTP traffic flow and valid 1PPS input to the Calnex front panels.

Note: Allow 10 minutes for the oscillator to warm completely and for the PTP4L software delay filter to settle.

The PTP4L output message format is:

```
ptp4l[message timestamp in seconds]
rms: time offset in nanoseconds, root-mean-squared max:
maximum (worst-case) time offset, in nanoseconds freq:
frequency offset, in part-per-billion with ± tolerance delay:
path delay, in nanoseconds with ± tolerance
```

The path delay increases with CAT5e cable length and will include the intrinsic path delay of Paragon test equipment. Paragon-X intrinsic delay is approximately 6.7 microseconds.

4.7 CONFIRMING OFFSET FROM MASTER IN PTP4L

1. Leave the PTP4L application running, and open a new terminal.
2. Check PTP4L statistics with the following command:

```
# pmc -u -b 0 'GET CURRENT_DATA_SET'
```

The output appears as follows:

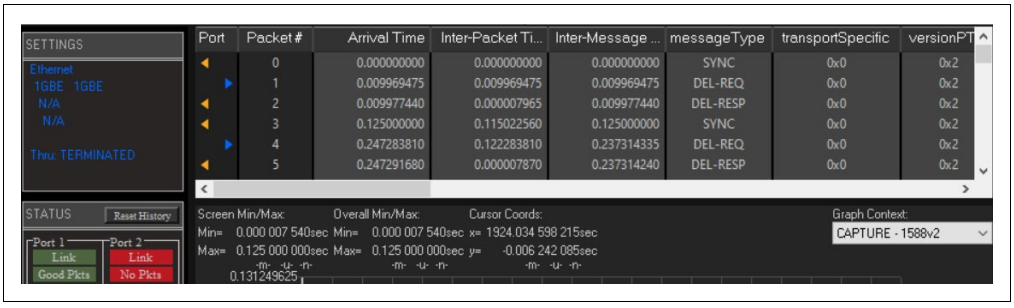
```
sending: GET CURRENT_DATA_SET
06823a.fffe.8caa74-0 seq 0 RESPONSE MANAGEMENT CURRENT_DATA_SET
stepsRemoved     1
offsetFromMaster 0.0
meanPathDelay    6721.0
```

Note: The offsetFromMaster is the key performance metric reported by the PTP4L application. It drifts within a peak-to-peak range of ±8 nanoseconds.

4.8 PERFORMING 1588 1PPS MEASUREMENTS USING PARAGON-X

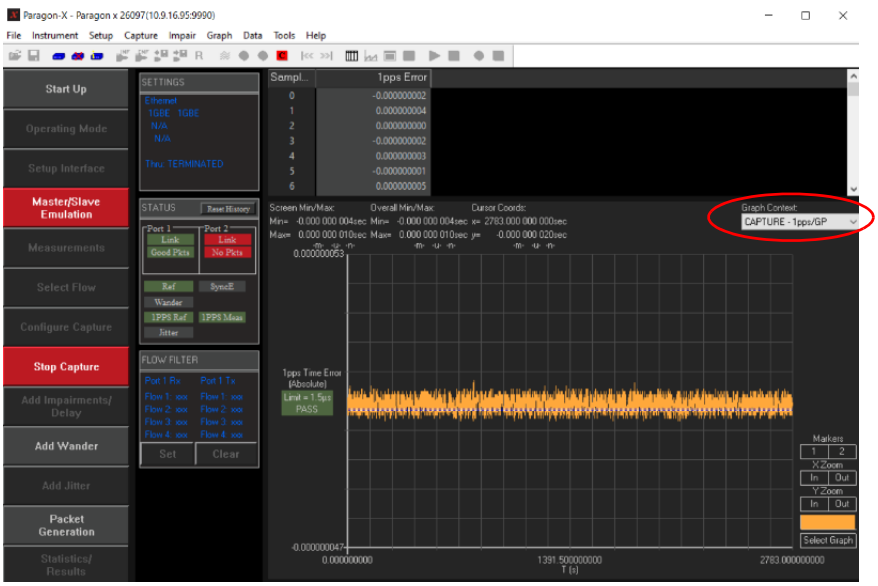
1. Select **Start Capture**. Two-way (Sync + Delay_req/Delay_resp) messages should be scrolling in the Paragon-X Capture window, as shown in the upper-right tile of Figure 4-26.

FIGURE 4-26: PARAGON-X CAPTURE WINDOW MESSAGES



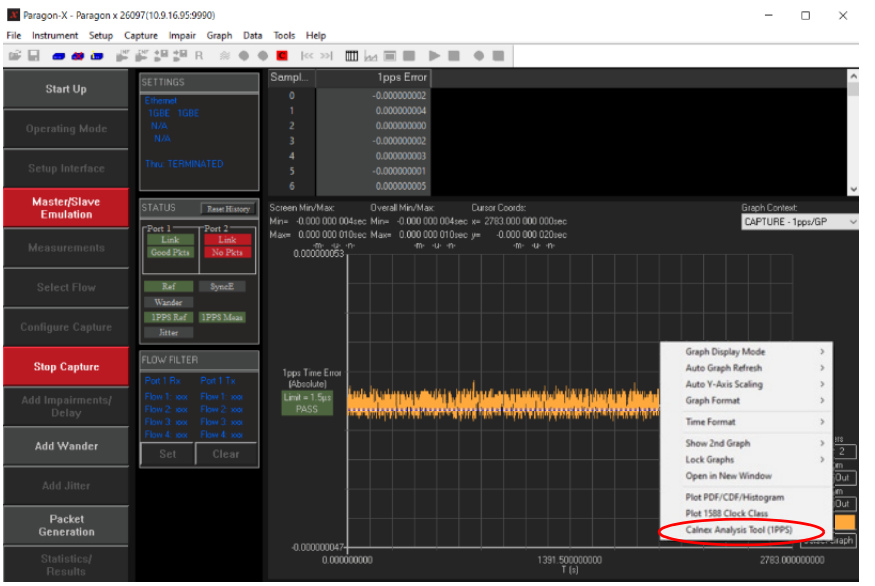
2. Select “CAPTURE - 1pps/GP” in the “Graph Context” field when the time error graph appears. See Figure 4-27.

FIGURE 4-27: GRAPH CONTEXT FIELD



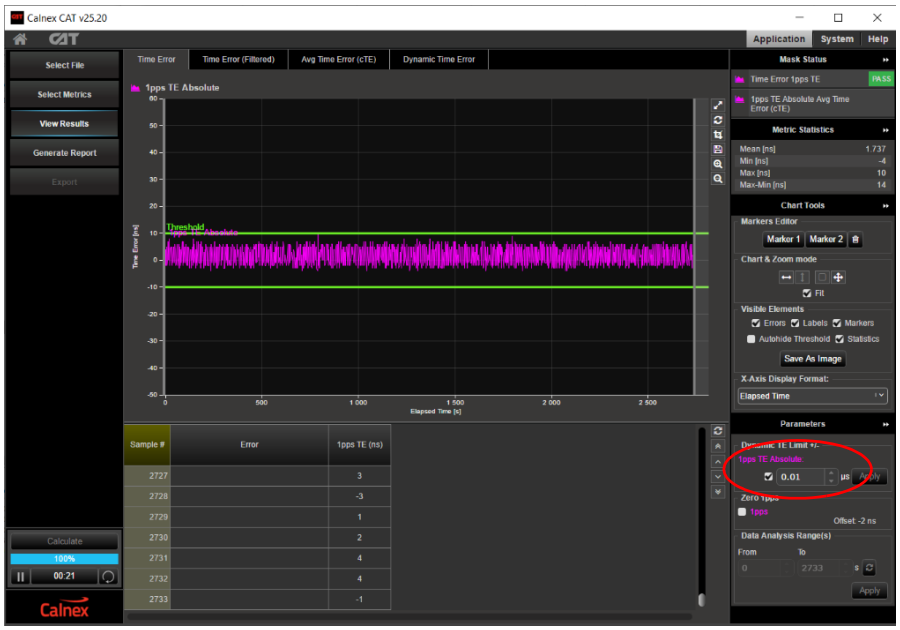
3. Select **Graph** in the lower right-hand corner of the same screen, and then select **Calnex Analysis Tool (1PPS)**. See Figure 4-28.

FIGURE 4-28: SELECTING CALNEX ANALYSIS TOOL (1PPS)



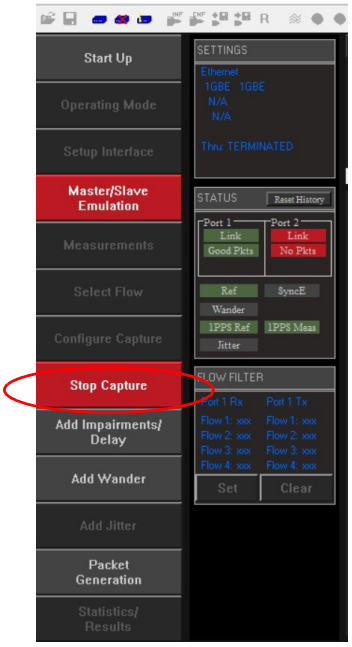
4. Once the CAT application finishes loading, click **View Results**. The Time Error dynamic plot appears.
5. Set the "Dynamic TE Limit +/–" field to the minimum allowable value (±0.01 microseconds) and click **Apply**. See Figure 4-29.

FIGURE 4-29: DYNAMIC TE LIMIT



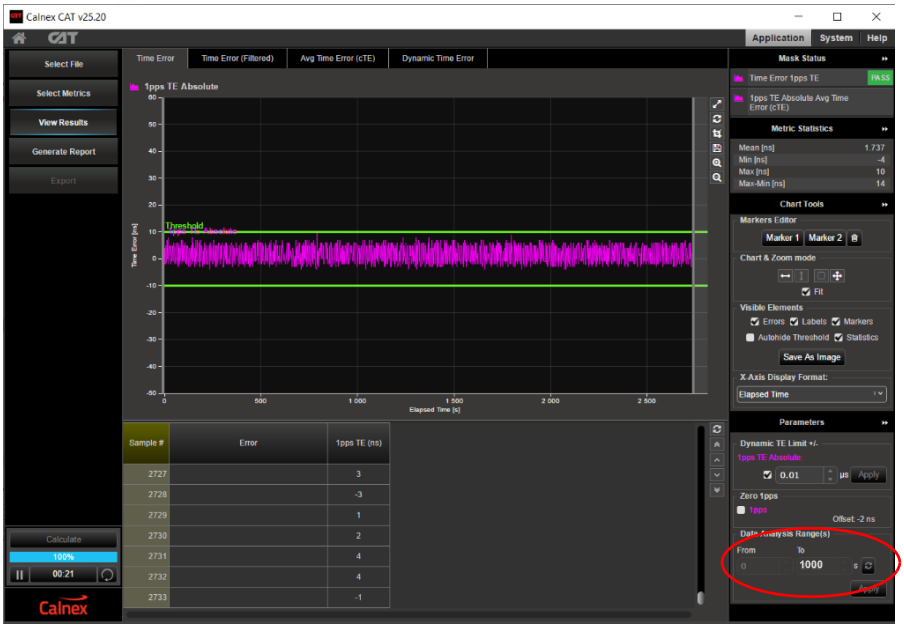
6. Allow sufficient time to capture the number of 1588 packet as well as 1PPS measurements for your desired observation interval. Once the desired interval has elapsed, return to the main Paragon-X window and click **Stop Capture**. See Figure 4-30.

FIGURE 4-30: STOP CAPTURE



7. Once capture has stopped, zoom to the desired observation window as shown in the lower right-hand circle in Figure 4-31.

FIGURE 4-31: SETTING AN OBSERVATION WINDOW



Note: A typical observation window for 1588-related performance metrics is 1000 seconds. The graphing toolbar allows zoom-to-range and ensures the x-axis plot of the TE metric matches the interval of calculated statistics.

The 1PPS Metric Statistics minimum/maximum has been verified to within ±8 ns for this EVB over a 1000 second observation window, which can be verified in the Metric Statistics reported in the above window. (The Dynamic TE Limit resolution limitation is ±10 ns.)

8. As desired, the average time error tab can be selected to dynamically view cTE calculations. Refer to Figure 4-32 and Figure 4-33. (This chart updates every 60 seconds, by default, and continues to draw updated cTE calculations in the x-dimension via the purple line.)

FIGURE 4-32: AVERAGE TIME ERROR (CTE)

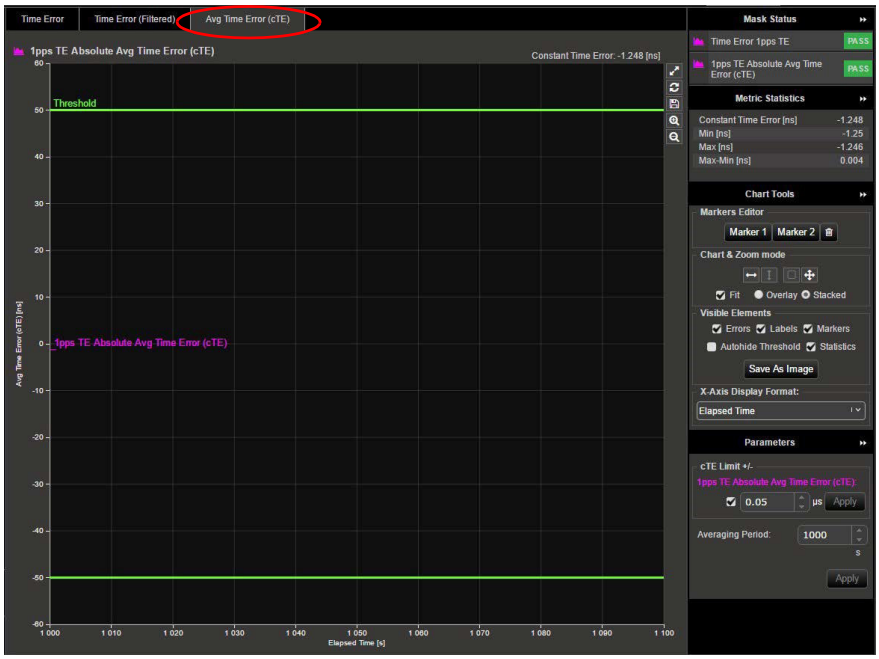


FIGURE 4-33: AVERAGE TIME ERROR (CTE) AFTER ELAPSED TIME

NOTES:

Appendix A. Schematics

A.1 INTRODUCTION

This appendix shows the EVB-LAN8841 schematic.

FIGURE A-1: EVB-LAN8841 SCHEMATIC 1

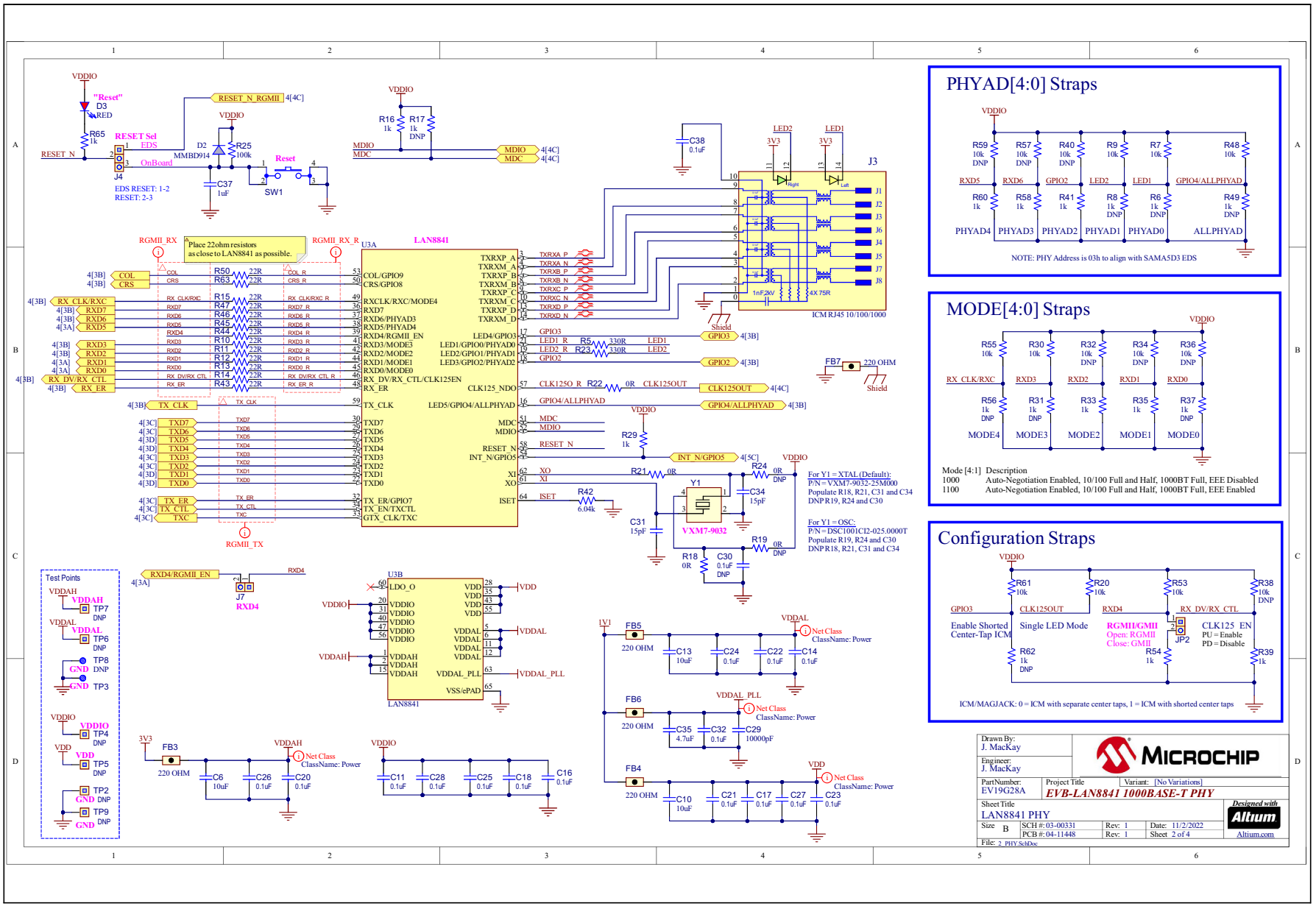


FIGURE A-2: EVB-LAN8841 SCHEMATIC 2

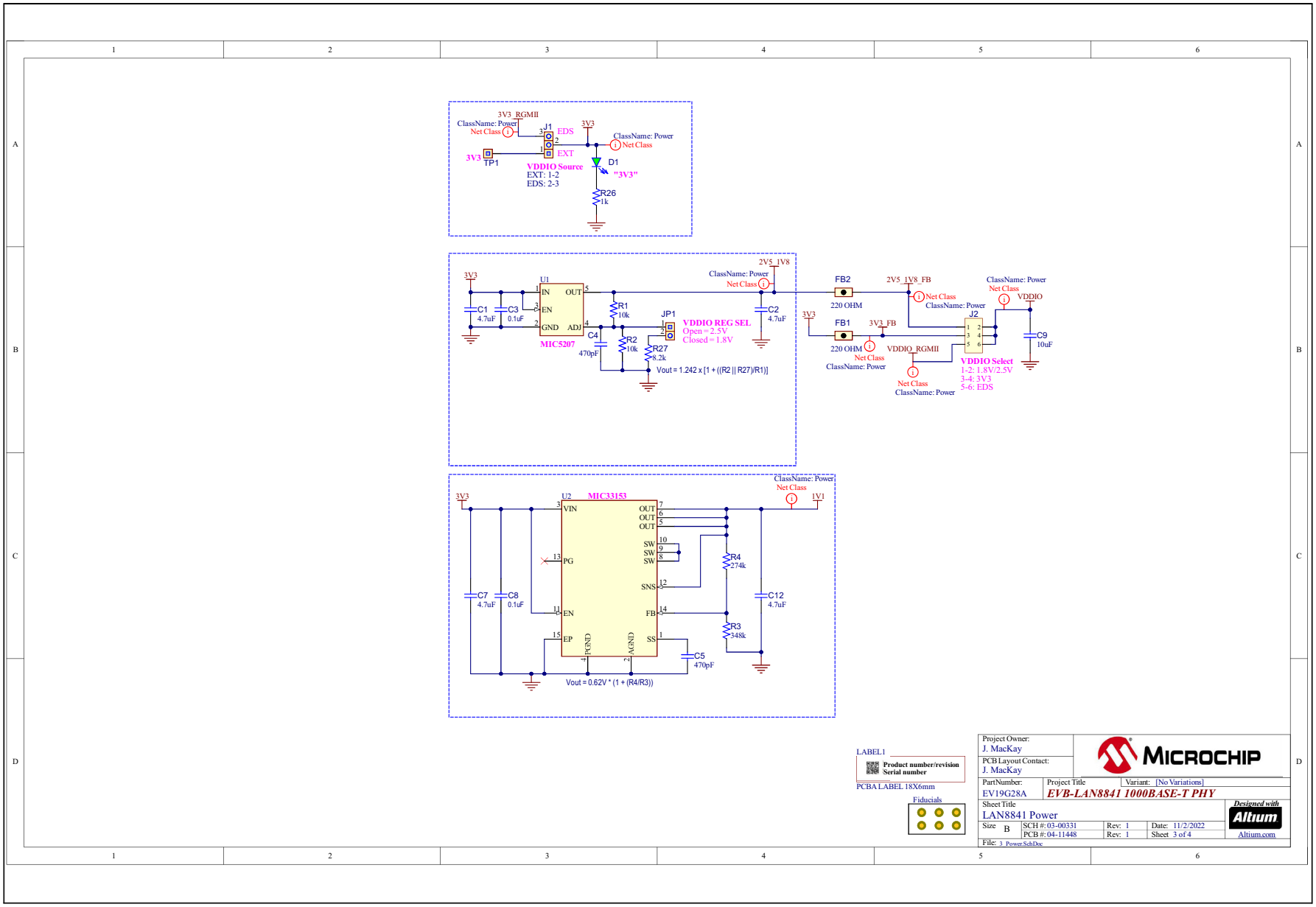
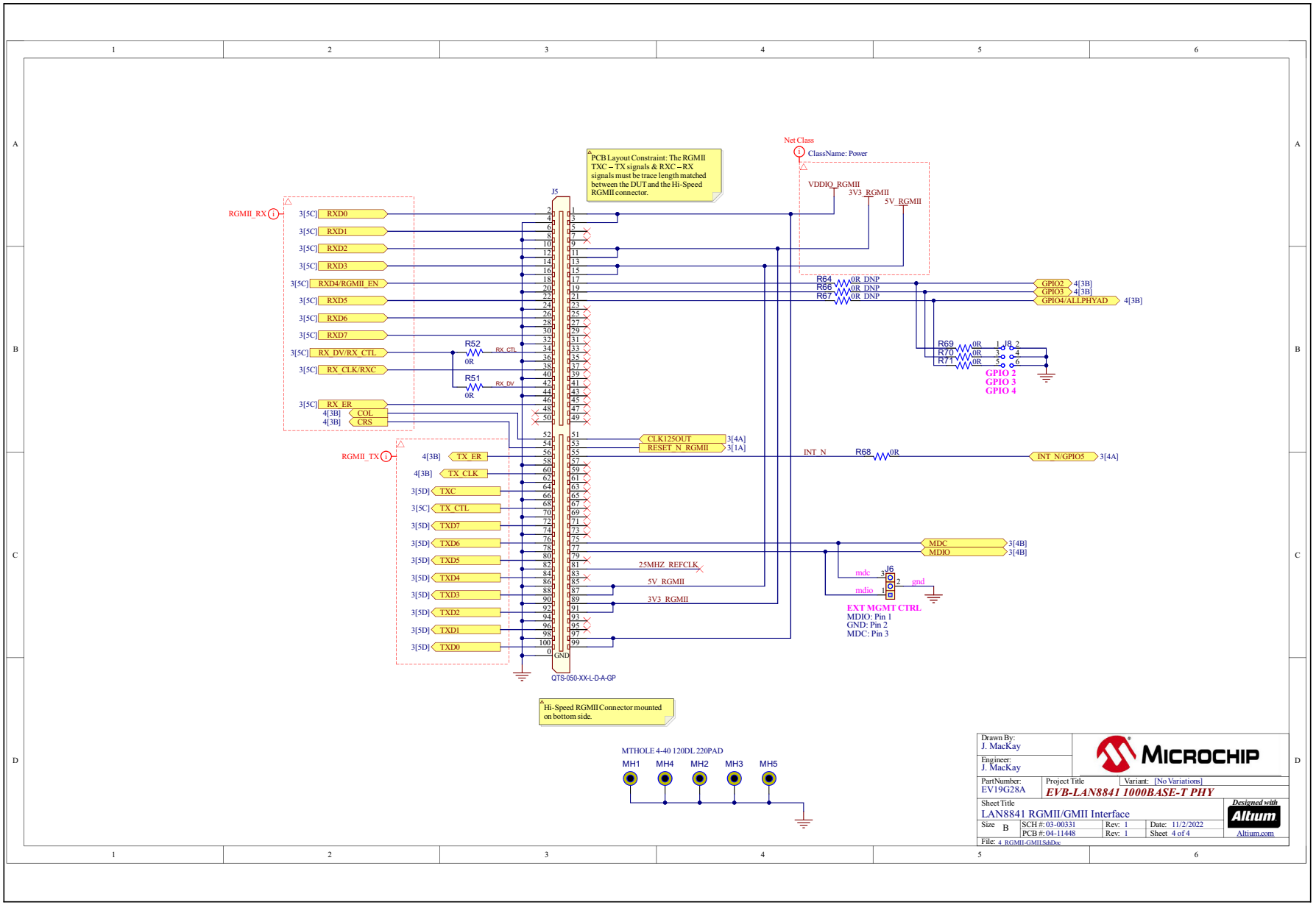


FIGURE A-3: EVB-LAN8841 SCHEMATIC 3



Appendix B. Bill of Materials

B.1 INTRODUCTION

This appendix contains the EVB-LAN8841 Bill of Materials (BOM).

TABLE B-1: EVB-LAN8841 BILL OF MATERIALS

Item	Qty	Designator	Description	Populated	Manufacturer	Manufacturer Part Number
1	5	C1, C2, C7, C12, C35	CAP CER 4.7uF 10V 10% X5R SMD 0603	YES	Yageo	CC0603MRX5R5BB475
2	18	C3, C8, C11, C14, C16, C17, C18, C20, C21, C22, C23, C24, C25, C26, C27, C28, C32, C38	CAP CER 0.1uF 50V 10% X7R SMD 0402	YES	TDK Corporation	C1005X7R1H104K050BB
3	2	C4, C5	CAP CER 470pF 25V 5% NP0 SMD 0603	YES	AVX	06033A471JAT2A
4	4	C6, C9, C10, C13	CAP TANT 10uF 20V 10% 2.1Ohm SMD B	YES	AVX	06036D106MAT2A
5	1	C29	CAP CER 10000pF 16V 10% X7R SMD 0402	YES	KEMET	C0402C103K4RACTU
6	2	C31,C34	CAP CER 15pF 50V 5% NP0 SMD 0402	YES	Johanson Technology Inc	500R07S150JV4T
7	1	C37	CAP CER 1uF 16V 10% X5R SMD 0603	YES	AVX	0603YD105KAT2A
8	1	D1	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603	YES	Lite-On Inc	LTST-C191KGKT
9	1	D2	DIO RECT MMBD914LT1G 1V 10mA 100V SMD SOT-23-3	YES	ON Semiconductor	MMBD914LT1G
10	1	D3	DIO RED 2V 20mA 54mcd CLEAR SMD 0603	YES	Lite-On Inc.	LTST-C191KRKT
11	7	FB1, FB2, FB3, FB4, FB5, FB6, FB7	FERRITE 500mA 220R SMD 0603	YES	Murata Electronics North America	BLM18AG221SN1D
12	3	J1, J4, J6	CON HDR-2.54 Male 1x3 Gold 5.84MH TH VERT	YES	FCI	68000-103HLF
13	1	J2	CON HDR-2.54 Male 2x3 Gold 5.84MH TH VERT	YES	Samtec	TSW-103-07-S-D
14	1	J3	CONN MAGJACK 1PORT 1000 BASE-T	YES	Pulse Electronics Network	JD1-0001NL
15	1	J5	CON STRIP High Speed Stacker 5mm Male 2x50 SMD VERT	YES	Samtec	QTS-050-01-L-D-A-GP
16	1	J7, JP1, JP2	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	YES	Wurth Electronics Inc.	61300211121
17	1	J8	CON HDR-2.54 Male 2x3 Tin 5.84MH TH VERT	YES	FCI	67996-406HLF
18	2	R1, R2	RES TKF 10k 1% 1/10W SMD 0603	YES	Panasonic	ERJ-3EKF1002V
19	1	R3	RES TKF 348k 1/10W 1% SMD 0603	YES	Stackpole Electronics Inc	RMCF0603FT348K
20	1	R4	RES TKF 274K 1% 1/10W SMD 0603	YES	Panasonic	ERJ-3EKF2743V
21	2	R5, R23	RES TKF 330R 5% 1/10W SMD 0603	YES	Stackpole Electronics Inc	RMCF0603JT330R
22	8	R7, R9, R20, R30, R48, R53, R55, R61	RES TKF 10k 5% 1/10W SMD 0603	YES	Panasonic	ERJ-3GEYJ103V
23	13	R10, R11, R12, R13, R14, R15, R43, R44, R45, R46, R47, R50, R63	RES TKF 22R 1% 1/20W SMD 0402	YES	Panasonic	ERJ-2RKF22R0X
24	11	R16, R26, R29, R33, R35, R39, R41, R54, R58, R60, R65	RES TKF 1k 5% 1/10W SMD 0603	YES	Panasonic	ERJ-3GEYJ102V
25	8	R18, R21, R51, R52, R68, R69, R70, R71	RES TKF 0R 1/16W SMD 0402	YES	Yageo	RC0402JR-070RL

TABLE B-1: EVB-LAN8841 BILL OF MATERIALS (CONTINUED)

Item	Qty	Designator	Description	Populated	Manufacturer	Manufacturer Part Number
26	1	R22	RES TKF 0R 1/10W SMD 0603	YES	Panasonic	ERJ-3GSY0R00V
27	1	R25	RES TKF 100k 1% 1/10W SMD 0603	YES	Stackpole Electronics Inc	RMCF0603FT100K
28	1	R27	RES TKF 8.2k 1% 1/10W SMD 0603	YES	Panasonic	ERJ-3EKF8201V
29	1	R42	RES TKF 6.04k 1% 1/10W SMD 0603	YES	Vishay/Dale	CRCW06036K04FKEA
30	1	SW1	SWITCH TACT SPST-NO 16V 0.05A PTS810 SMD	YES	C&K Components	PTS810 SJM 250 SMTR LFS
31	7	TP1	CON HDR-2.54 Male 1x1 Gold 5.84MH TH VERT	YES	TE Connectivity	5-146280-1
32	2	TP3	CON TP LOOP Black TH	YES	Keystone	5011
33	1	U1	MCHP ANALOG LDO ADJ MIC5207YM5 SOT-23-5	YES	Microchip	MIC5207YM5-TR
34	1	U2	MCHP ANALOG SWITCHER Buck 0.6V to 3.6V MIC33153YHJ-TR VFDFN-14	YES	Microchip	MIC33153YHJ-TR
35	1	U3	MCHP INTERFACE ETHERNET LAN8841 QFN-64	YES	Microchip	LAN8841/Q2A
36	1	Y1	MCHP CRYSTAL 25Mhz +/-20ppm 10pF SMD L3.2W2.5H0.8	YES	Microchip	VXM7-9032-25M0000000

NOTES:

NOTES:

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