MCP998X/MCP9933
MCP998XD/MCP9933D

2-Wire, ±1.0°C Accurate Multichannel Automotive Temperature Monitor

Features Overview

Temperature Measurement

- Up to Four External Temperature Monitors
  - ±1°C max. accuracy ($-40°C < T_{DIODE} < +125°C$)
  - 0.125°C resolution
- Internal Temperature Monitor
  - ±1°C accuracy
  - 0.125°C resolution
- Anti-Parallel Diodes for Extra Diode Support
- Advanced measurement techniques:
  - Automatic beta compensation
  - Ideality factor correction
  - Resistance error correction

Communications

- SMBus 3.1/I^2C Compatible
- Up to 1 MHz Clock Rate
  - Supports block mode reads and writes for faster access
  - Temperature registers duplicated in a separate, contiguous block for easy access
- Maskable $\overline{ALERT}/\overline{THERM}$ pin
  - Maskable with register control
  - Set point controlled by I^2C register write (+85°C default)
  - I^2C compliant $\overline{ALERT}$
- Compatible with EIA/JEDEC 8-7 standard for 1.8V and 3.3V logic levels
- Non-Maskable $\overline{THERM}/\overline{ADDR}$ and $\overline{SYS\_SHDN}$ Pins
  - Set point controlled by pull-up resistor option available (MCP998XD only)
  - Acts in either Interrupt or Comparator mode

Other Features

- Resistor Programmable System Shutdown Temperature (MCP998XD only)
- Operating voltage: 1.7V to 3.6V
- Low Power Operation - Standby Current Less Than 30 µA typical, 85 µA maximum
- ESD Protection > 4 kV HBM
- Temperature Range: -40°C to +125°C
- Pin Compatible with EMC18XX Products

Packages

- 8-Lead MSOP
- 10-Lead MSOP
- 10-Lead VDFN
- 8-Lead WDFN

Description

The MCP998X/MCP9933/MCP998XD/MCP9933D family of devices is a high-accuracy, low-cost, 2-wire communication protocol (I^2C/SMBus) temperature sensor.

The MCP998X/MCP9933/MCP998XD/MCP9933D family can monitor up to five temperature channels. Advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model) and automatic diode type detection combine to provide a robust solution for complex environmental monitoring applications.

Resistance Error Correction automatically eliminates the temperature error caused by series resistance allowing greater flexibility in routing thermal diodes. Beta Compensation eliminates temperature errors caused by low, variable beta transistors common in today's fine geometry processors. The automatic beta detection feature monitors the external diode/transistor and determines the optimum sensor settings for accurate temperature measurements regardless of processor technology. This frees the user from providing unique sensor configurations for each temperature monitoring application.

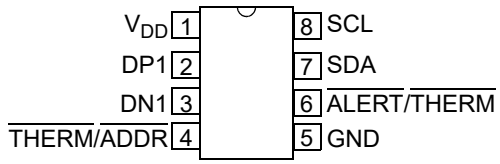
These advanced features and the ±1°C measurement accuracy for both external and internal diode temperatures provide a low-cost, highly flexible and accurate solution for critical temperature monitoring applications.

I^2C communications are compatible with the EIA/JEDEC 8-7 standard for 1.8V and 3.3V levels. The I^2C address may be a fixed-address or set via a pull-up resistor.

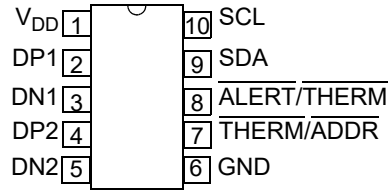
Package Types

Note: See **Section 3.0 "Pinout and Pin Descriptions"**.

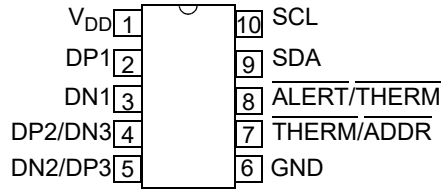
MCP9982
(2 x2 mm WDFN, MSOP-8)



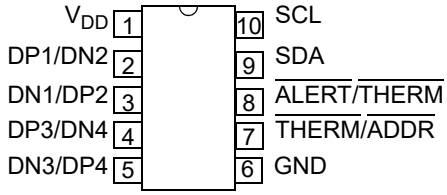
MCP9983
(2 x 2.5 mm VDFN, MSOP-10)



MCP9984
(2 x 2.5 mm VDFN, MSOP-10)



MCP9985
(2 x 2.5 mm VDFN, MSOP-10)



MCP9933
(2 x 2 mm WDFN, MSOP-8)

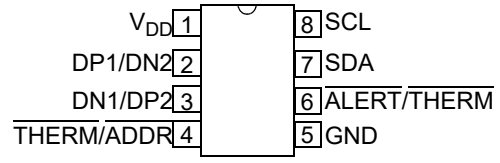
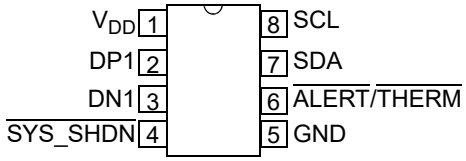
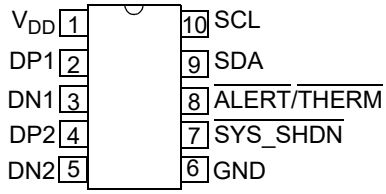


FIGURE 1: *MCP9982/83/84/85/33 Pin Diagrams.*

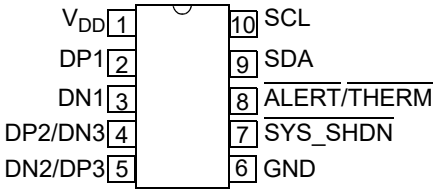
MCP9982D
(2 x2 mm WDFN, MSOP-8)



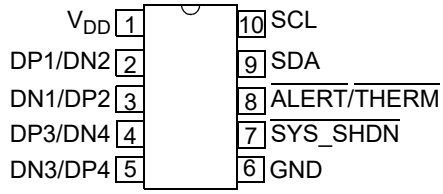
MCP9983D
(2 x 2.5 mm VDFN, MSOP-10)



MCP9984D
(2 x 2.5 mm VDFN, MSOP-10)



MCP9985D
(2 x 2.5 mm VDFN, MSOP-10)



MCP9933D
(2 x 2 mm WDFN, MSOP-8)

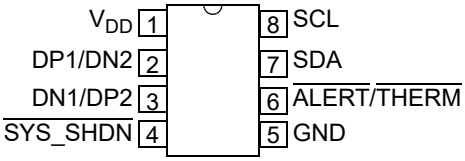


FIGURE 2: *MCP9982D/3D/4D/5D and MCP9933D Pin Diagrams.*

Functional Block Diagrams

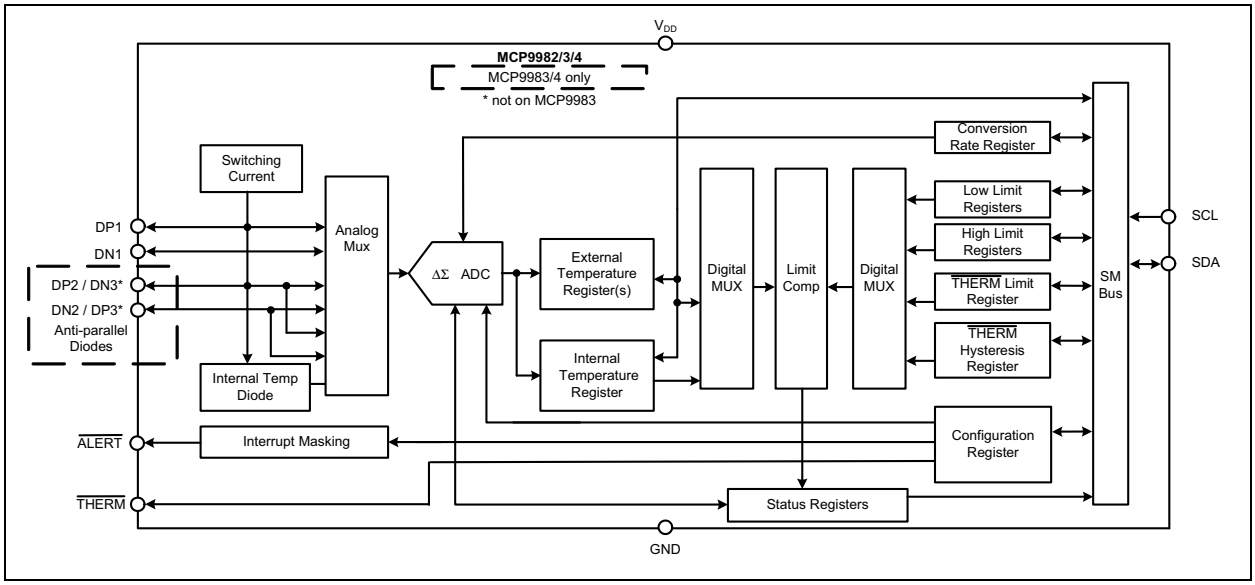


FIGURE 3: *MCP9982/3/4 Functional Block Diagram.*

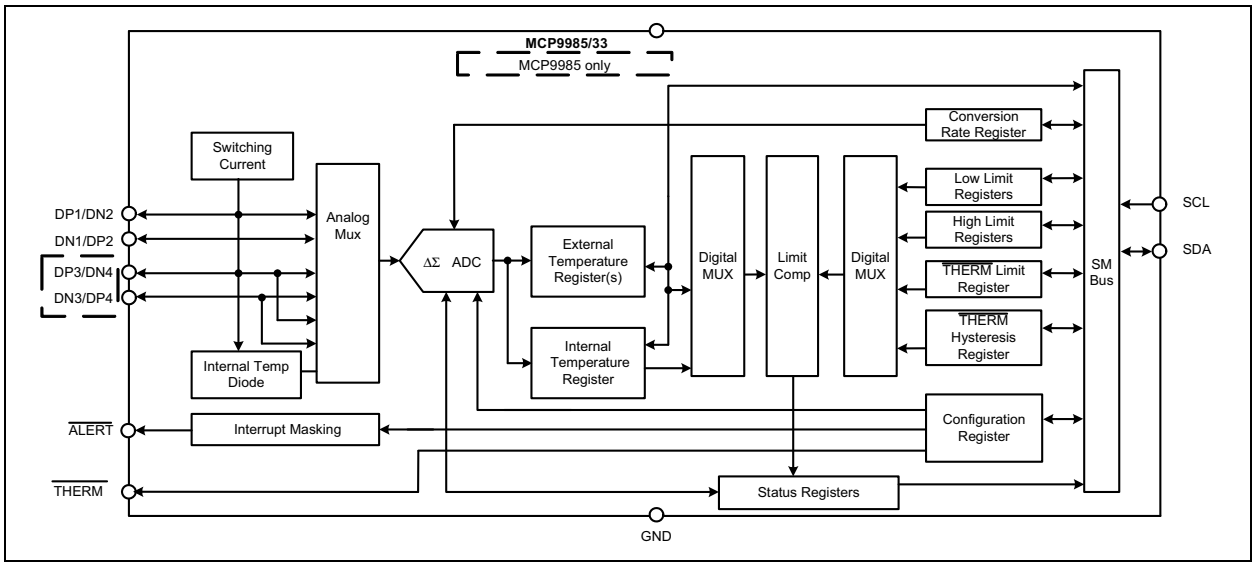


FIGURE 4: *MCP9985 and MCP9933 Functional Block Diagram.*

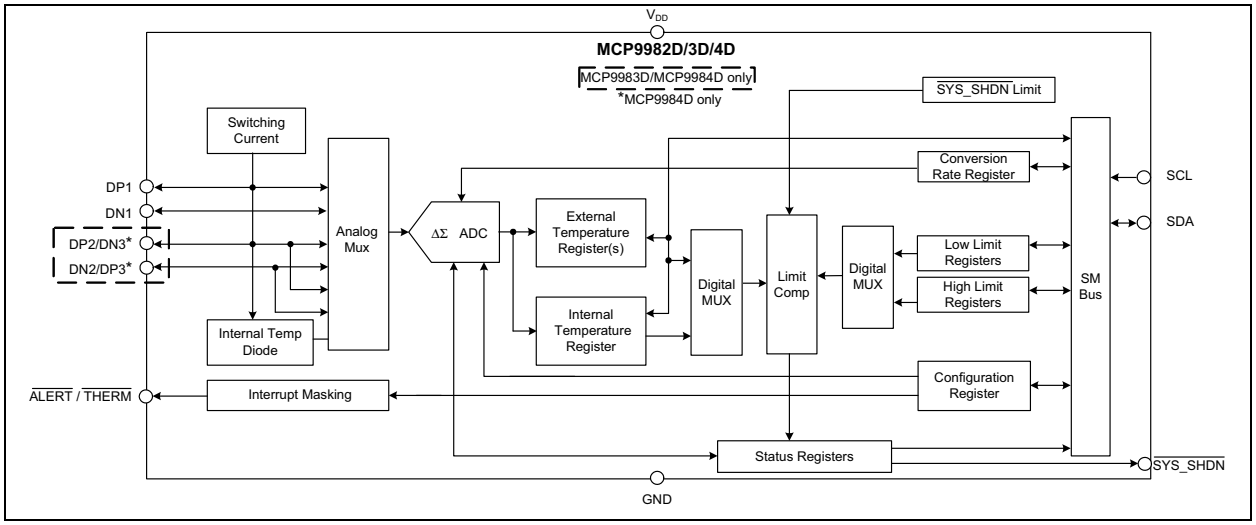


FIGURE 5: *MCP9982D/3D/4D Functional Block Diagram.*

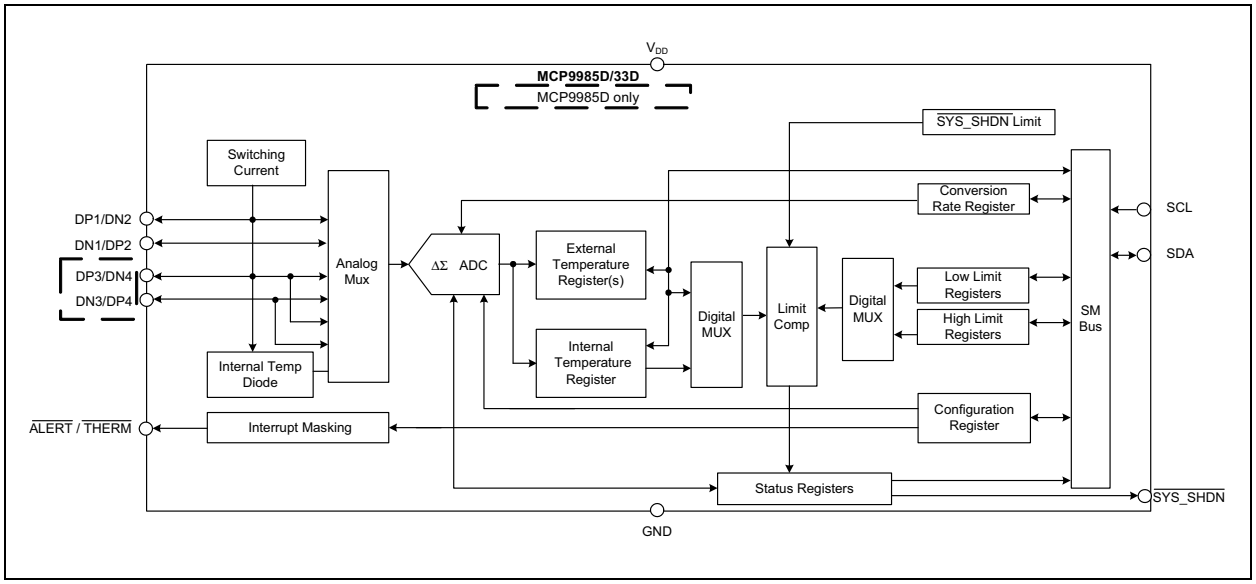


FIGURE 6: *MCP9985D and MCP9933D Functional Block Diagram.*

1.0 ELECTRICAL CHARACTERISTICS

1.1 Electrical Specifications

Absolute Maximum Ratings †

V_{DD} 4.0V
Voltage at All Input/Output Pins ..... GND – 0.3V to 4.0V
Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied ..... -40°C to +125°C
Junction Temperature (T_J) ..... +150°C
ESD Protection on All Pins (HBM, CDM) ..... (4 kV, ±750V)
Latch-Up Current at Each Pin ..... ±105 mA

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

Operating Conditions: Unless otherwise indicated, 1.7V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C.							
No.	**Parameters**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
P1	Supply Voltage	V_{DD}	1.7	—	3.6	V	
P2	Supply Current	I_{DD}	—	40	—	µA	0.0625 conversions/second, dynamic averaging disabled (**Note 1**)
P3				140	—		1 conversion/second, dynamic averaging disabled (**Note 1**)
P4				450	—		4 conversion/second, dynamic averaging disabled (**Note 1**)
P5				900	1115		≥ 16 conversions/second, dynamic averaging enabled, averaged over 150 ms
P6	Standby Supply Current	I_{DD_SB}	—	30	85	µA	Device in Stand-by mode, no active I^2C communications, $\overline{\text{ALERT}}/\text{THERM}$ and $\text{THERM}/\overline{\text{ADDR}}$ pins not asserted, V_{DD} = 3.3V (**Note 2**)
P7	Power-on Reset (POR) Release Voltage	PORR	—	1.45	—	V	Rising V_{DD}
P8	Power-up Timer	t_{PWRT}	—	10	—	ms	
Internal Temperature Monitor							
P9	Temperature Accuracy		—	±0.2 ±0.4	±1.0 ±2.5	°C	+20C < T_A < +85°C, V_{DD} = 3.3V -40C < T_A < +125°C, V_{DD} = 3.3V
P10	Temperature Resolution		—	0.125	—	°C	
External Temperature Monitor							
P11	Temperature Accuracy		—	±0.2	±1.0	°C	+20C < T_A < +85C, -40C < T_{DIODE} < +125C, V_{DD} = 3.3V
				±0.4	±2.5		-40C < T_A < +125C, -40C < T_{DIODE} < +125C, V_{DD} = 3.3V
P12	Temperature Resolution		—	0.125	—	°C	

Note 1: Characterized by design; not tested by production.
2: MCP998XD devices cannot enter Standby Mode.

TABLE 1-1: DC CHARACTERISTICS (CONTINUED)

Operating Conditions: Unless otherwise indicated, 1.7V ≤ V_{DD} ≤ 3.6V at -40°C ≤ T_A ≤ +125°C.							
No.	**Parameters**	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Timing and Capacitive Filter							
P13	Time to First Communications	t_{INT_T}	—	15	—	ms	Time after power-up before device is ready to begin communications and measurements
P14	Conversion Time per Channel	t_{CONV}	—	25	—	ms	Default settings
P15	Time to First Conversion from Standby	t_{CONV1}	—	125	—	ms	Default settings
$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ Pins							
P16	Output Low Voltage	V_{OL}	—	—	0.4	V	I_{SINK} = 3 mA
P17	Leakage Current	I_{LEAK}	—	—	±5	µA	$\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ and $\overline{\text{THERM}}$/ADDR or $\overline{\text{SYS\_SHDN}}$ pins, device powered or unpowered, pull-up voltage ≤ 3.6V
SCL and SDA Pins							
Input							
P18	High-Level Voltage	V_{IH}	0.7 × V_{DD}	—	—	V	
P19	Low-Level Voltage	V_{IL}	—	—	0.3 × V_{DD}		
P20	Input Current	I_{IN}	—	—	±5	µA	SDA and SCL pins only
Output (SDA pin only)							
P21	Low-Level Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3 mA
P22	High-Level Current (leakage)	I_{OH}	—	—	5	µA	V_{OH} = V_{DD}
P23	Low-Level Current	I_{OL}	—	—	3	mA	V_{OL} = 0.4V, V_{DD} = 2.2V to 3.6V
P24	Capacitance	C_{IN}	—	5	—	pF	
SDA and SCL Inputs							
P25	Hysteresis	V_{HYST}	—	0.05	—	V	
P26	Spike Suppression	t_{SP}	—	50	—	ns	

Note 1: Characterized by design; not tested by production.

2: MCP998XD devices cannot enter Standby Mode.

TABLE 1-2: SMBUS SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, 1.7V < V_{DD} < 3.6V, T_A = -40°C to +125°C and C_L = 80 pF.					
Parameters	**Sym.**	**Min.**	**Max.**	**Units**	**Notes**
2-Wire SMBus Interface					
Clock Frequency	f_{SMB}	10	1000	kHz	
Bus Free Time Stop to Start	t_{BUF}	0.5	-	µs	
Start Setup Time	$t_{SU:STA}$	0.26	-	µs	
Start Hold Time	$t_{HD:STA}$	0.26	-	µs	
Stop Setup Time	$t_{SU:STO}$	0.26	-	µs	
Data Hold Time	$t_{HD:DAT}$	0	-	µs	When transmitting to the host
Data Hold Time	$t_{HD:DAT}$	0	-	µs	When receiving from the host
Data Setup Time	$t_{SU:DAT}$	50	-	ns	
Clock Low Period	t_{LOW}	0.5	-	µs	
Clock High Period	t_{HIGH}	0.26	50	µs	
Clock/Data Fall Time	t_{FALL}	-	120	ns	Min = 20+0.1C_{LOAD} ns
Clock/Data Rise Time	t_{RISE}	-	120	ns	Min = 20+0.1C_{LOAD} ns
Capacitive Load	C_{LOAD}	-	400	pF	Per bus line
Timeout	$t_{TIMEOUT}$	25	35	ms	

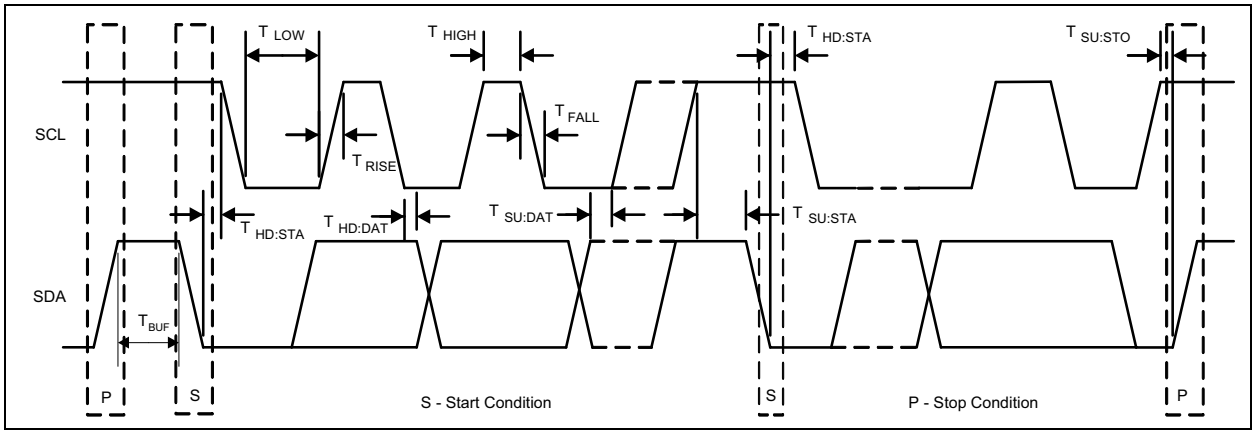


FIGURE 1-1: *SMBus Timing Diagram.*

NOTES:

2.0 TYPICAL OPERATING CURVES

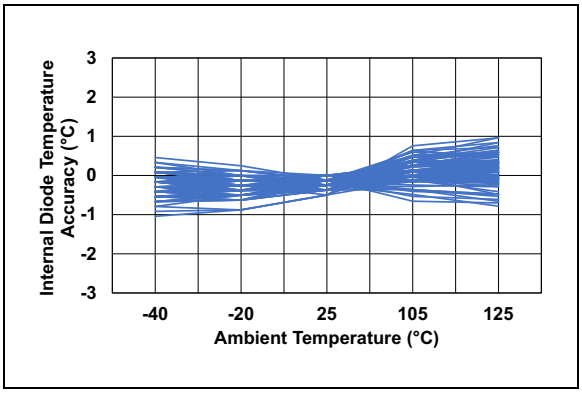


FIGURE 2-1: *Internal Temperature Monitor Accuracy vs. Ambient Temperature (120 units).*

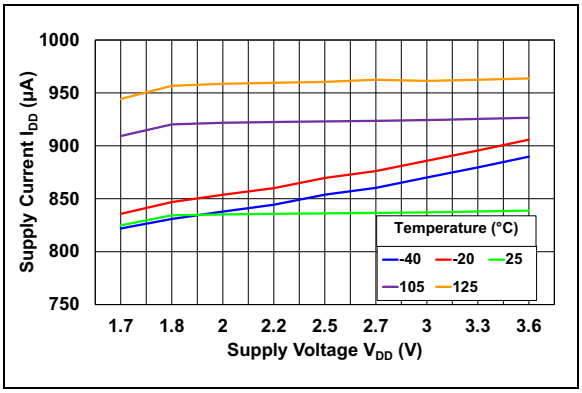


FIGURE 2-4: *Supply Current I_{DD} vs. Supply Voltage V_{DD} Across Temperature.*

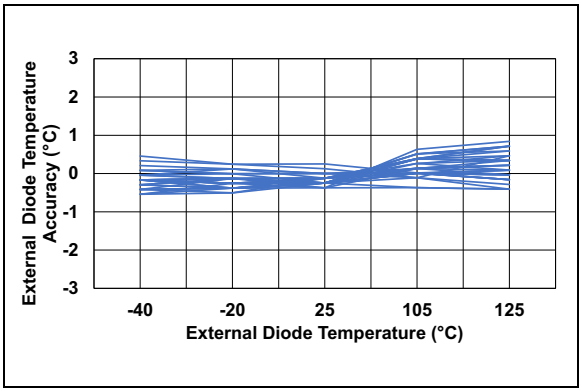


FIGURE 2-2: *External Temperature Accuracy vs. Diode Temperature (V_{DD} = 3.3V, 116 units, T_{AMB} = T_{ext}).*

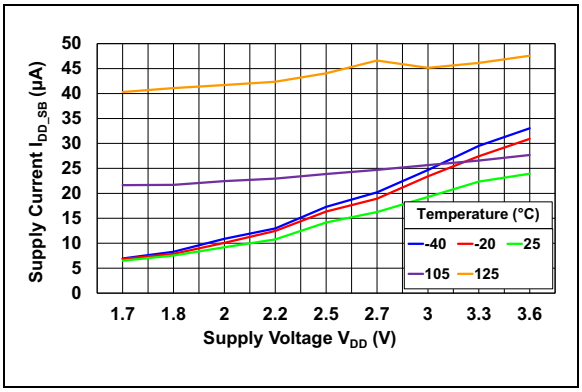


FIGURE 2-5: *Standby Supply Current I_{DD_SB} vs. Supply Voltage V_{DD} Across Temperature.*

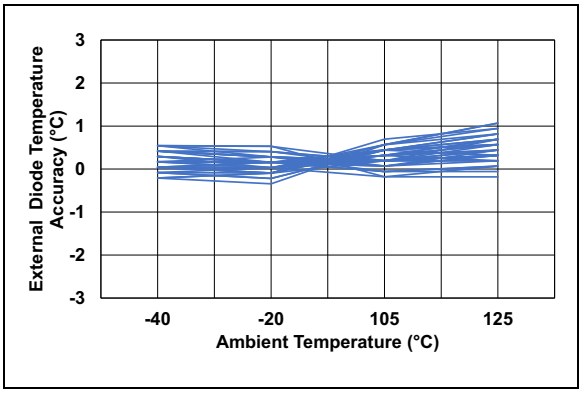


FIGURE 2-3: *External Temperature Accuracy vs. Ambient Temperature (V_{DD} = 3.3V, 116 units, T_{DIODE} = +25°C).*

3.0 PINOUT AND PIN DESCRIPTIONS

The pinout is described in Table 3-1.

TABLE 3-1: MCP998X/MCP9933/MCP998XD/MCP9933D FAMILY PINOUT DESCRIPTION

Pin Name	MCP 9982	MCP 9983	MCP 9984	MCP 9985	MCP 9933	MCP 9982D	MCP 9983D	MCP 9984D	MCP 9985D	MCP 9933D	Pin Type	Pin Description
V_{DD}	1	1	1	1	1	1	1	1	1	1	P	Power
GND	5	6	6	6	5	5	6	6	6	5	P	Ground
$\overline{\text{ALERT}}$/$\overline{\text{THERM}}$	6	8	8	8	6	6	8	8	8	6	OD	I^2C Alert Pin
$\overline{\text{THERM}}$/$\overline{\text{ADDR}}$	4	7	7	7	4	—	—	—	—	—	OD	Thermal Alert
$\overline{\text{SYS\_SHDN}}$	—	—	—	—	—	4	7	7	7	4	OD	System Shutdown
SDA	7	9	9	9	7	7	9	9	9	7	OD	I^2C Data
SCL	8	10	10	10	8	8	10	10	10	8	OD	I^2C Clock
DP1	2	2	2	—	—	2	2	2	—	—	A	Diode 1 Connection
DN1	3	3	3	—	—	3	3	3	—	—	A	Diode 1 Connection
DP2	—	4	—	—	—	—	4	—	—	—	A	Diode 2 Connection
DN2	—	5	—	—	—	—	5	—	—	—	A	Diode 2 Connection
DP2/DN3	—	—	4	—	—	—	—	4	—	—	A	Diode 2/3 Connection
DN2/DP3	—	—	5	—	—	—	—	5	—	—	A	Diode 2/3 Connection
DP1/DN2	—	—	—	2	2	—	—	—	2	2	A	Diode 1/2 Connection
DN1/DP2	—	—	—	3	3	—	—	—	3	3	A	Diode 1/2 Connection
DP3/DN4	—	—	—	4	—	—	—	—	4	—	A	Diode 3/4 Connection
DN3/DP4	—	—	—	5	—	—	—	—	5	—	A	Diode 3/4 Connection

Legend:	P = Power	A = Analog Pin	OD = Open-Drain Pin

3.1 Pin Configurations

The MCP998X/MCP9933/MCP998XD/MCP9933D family has ten variants that include features unique to each device. Refer to Table 3-1 to determine the applicability of the pin descriptions below:

3.1.1 V_{DD} PIN

This pin is used to supply power to the device.

3.1.2 GND PIN

This pin is used to ground the device.

3.1.3 $\overline{ALERT}$/$\overline{THERM}$ - ALERT AND THERM PINS

Open-drain output with a pull-up resistor to determine the Hardware Thermal Shutdown Limit on the MCP998XD devices. This pin functions as either an ALERT output or a THERM output, depending on the configuration settings, and deasserts when the appropriate status register is read and when the condition is removed (see **Section 4.7 "ALERT/THERM Output"**). A pull-up resistor on this pin is recommended regardless of usage.

3.1.4 $\overline{THERM}$/$\overline{ADDR}$ - THERM FUNCTION PIN

Open-drain output which needs a pull-up resistor. With address decode devices (product names ending in "-A"), this pull-up resistor determines the I^2C/SMBus client address. This pin functions as a $\overline{THERM}$ output and deasserts when the condition is removed. A pull-up resistor on this pin is recommended regardless of usage.

3.1.5 $\overline{SYS\_SHDN}$ - HARDWARE SYSTEM SHUTDOWN PIN

The MCP998XD devices contain a hardware configured temperature limit circuit that controls the $\overline{SYS\_SHDN}$ pin. The threshold temperature is determined by the pull-up resistors on both the $\overline{SYS\_SHDN}$ and $\overline{ALERT}$/$\overline{THERM}$ pins.

Note:	Standby and One-Shot modes cannot be enabled in device configurations including system shutdown functionality.

The final temperature decode is the responsibility of the digital block. The overall decode is shown in Table 4-5.

The hardware shutdown circuitry measures the External Diode 1 channel and compares it against the hardware thermal shutdown limit. The $\overline{THERM}$ consecutive alert counter (set to four by default for the $\overline{SYS\_SHDN}$ pin) applies to this comparison. If the temperature meets or exceeds the limit for the set number of consecutive measurements, the $\overline{SYS\_SHDN}$ pin is asserted. The $\overline{SYS\_SHDN}$ pin remains asserted until the temperature drops below the limit minus 10°C. While the Therm limit hysteresis is configurable, the $\overline{SYS\_SHDN}$ hysteresis is locked to 10°C. All of the measurement channels (including the External Diode 1 channel) can be configured to assert the $\overline{SYS\_SHDN}$ pin using the Hardware Thermal Shutdown Limit (see Register 5-29). If a channel is configured to assert the $\overline{SYS\_SHDN}$ pin using the Hardware Thermal Shutdown Limit, the temperature on the measured channel must exceed the Hardware Thermal Shutdown Limit value. If a channel is not configured to assert the $\overline{SYS\_SHDN}$ pin using the Hardware Thermal Shutdown Limit, the $\overline{SYS\_SHDN}$ pin will behave the same way as the $\overline{THERM}$ output.

3.1.6 SDA - I^2C DATA

This is the open drain, bidirectional data pin for I^2C communication

3.1.7 SCL - I^2C CLOCK

This is the I^2C input clock pin for I^2C communication.

3.1.8 DP1 - DIODE 1 POSITIVE CONNECTION

This is the External Diode 1 bias pin and positive differential measurement. Beta Compensation is available.

3.1.9 DN1 - REMOTE DIODE 1 NEGATIVE CONNECTION

This is the External Diode 1 bias return pin and negative differential measurement. Beta Compensation is available.

3.1.10 DP2 - DIODE 2 POSITIVE CONNECTION

This is the External Diode 2 bias pin and positive differential measurement. Beta Compensation is available.

3.1.11 DN2 - REMOTE DIODE 2 NEGATIVE CONNECTION

This is the External Diode 2 bias return pin and negative differential measurement. Beta Compensation is available.

3.1.12 DP1/DN2 - DIODE 1 POSITIVE/DIODE 2 NEGATIVE

External Diode 1 bias pin and positive differential measurement. External Diode 2 bias return pin and negative differential measurement. Beta compensation is not available when anti-parallel diode (APD) is enabled.

3.1.13 DN1/DP2 - DIODE 1 NEGATIVE/DIODE 2 POSITIVE

External Diode 1 bias return pin and negative differential measurement. External Diode 2 bias pin and positive differential measurement. Beta compensation is not available when APD is enabled.

3.1.14 DP2/DN3 - DIODE 2 POSITIVE/DIODE 3 NEGATIVE

External Diode 2 bias pin and positive differential measurement. If enabled, External Diode 3 bias return pin and negative differential measurement. Beta compensation is not available when APD is enabled.

3.1.15 DN2/DP3 - DIODE 2 NEGATIVE/DIODE 3 POSITIVE

External Diode 3 bias return pin and negative differential measurement and if enabled, External Diode 2 bias pin and positive differential measurement. Beta compensation is not available when APD is enabled.

3.1.16 DP3/DN4 - DIODE 3 POSITIVE/DIODE 4 NEGATIVE

External Diode 3 bias pin and positive differential measurement. External Diode 4 bias return pin and negative differential measurement. Beta compensation is not available when APD is enabled.

3.1.17 DN3/DP4 - DIODE 3 NEGATIVE / DIODE 4 POSITIVE

External Diode 3 bias return pin and negative differential measurement. External Diode 4 bias pin and positive differential measurement. Beta compensation is not available when APD is enabled.

4.0 PRODUCT DESCRIPTION

The MCP998X/MCP9933/MCP998XD/MCP9933D family monitors one internal diode and up to four externally connected temperature diodes.

Thermal management is performed in cooperation with a host device. This consists of the host reading the temperature data of both the external and internal temperature diodes of the MCP998X/MCP9933/MCP998XD/MCP9933D and using that data to manage thermal events or to control the speed of one or more fans.

The MCP998X/MCP9933/MCP998XD/MCP9933D family has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures exceed the user-programmed limits. This allows the MCP998X/MCP9933/MCP998XD/MCP9933D family to be used as an independent thermal watchdog to warn the host of temperature hot-spots without direct control by the host. The second level of monitoring provides a non-maskable interrupt on the $\overline{\text{THERM}}$/ADDR or $\overline{\text{SYS\_SHDN}}$ pins if the measured temperatures meet or exceed a second programmable limit.

The MCP9982/82D is a single-channel remote temperature sensor, while the MCP9983/83D features a dual-channel design. The remote channels for this selection of devices can support substrate diodes, discrete diode connected transistors, or embedded processor thermal diodes.

The MCP9984/84D supports APD only on one channel. For the channel that does not support APD functionality substrate diodes, discrete diode connected transistors or embedded processor thermal diodes are supported.

For the channel that does support APD, only discrete diode connected transistors may be implemented. However, if APD is disabled on the MCP9984/84D, the channel that does support APD will be functional with substrate diodes, discrete diode connected transistors and embedded processor thermal diodes.

The MCP9985/85D supports APD on all channels. When APD is enabled then the channels only support diode connected transistors. If APD is disabled, then the channels will support substrate transistors, discrete diode connected transistors, and embedded processor thermal diodes.

The MCP9933/33D supports APD on its two external channels. When APD is enabled, the channels only support diode-connected transistors. When APD is disabled, the channels only support substrate transistors, discrete diode-connected transistors, and embedded processor thermal diodes.

Note:	Disabling APD functionality to implement substrate diodes eliminates the benefit of APD (two diodes on one channel).

Figure 4-1 shows a system-level block diagram of the MCP998X.

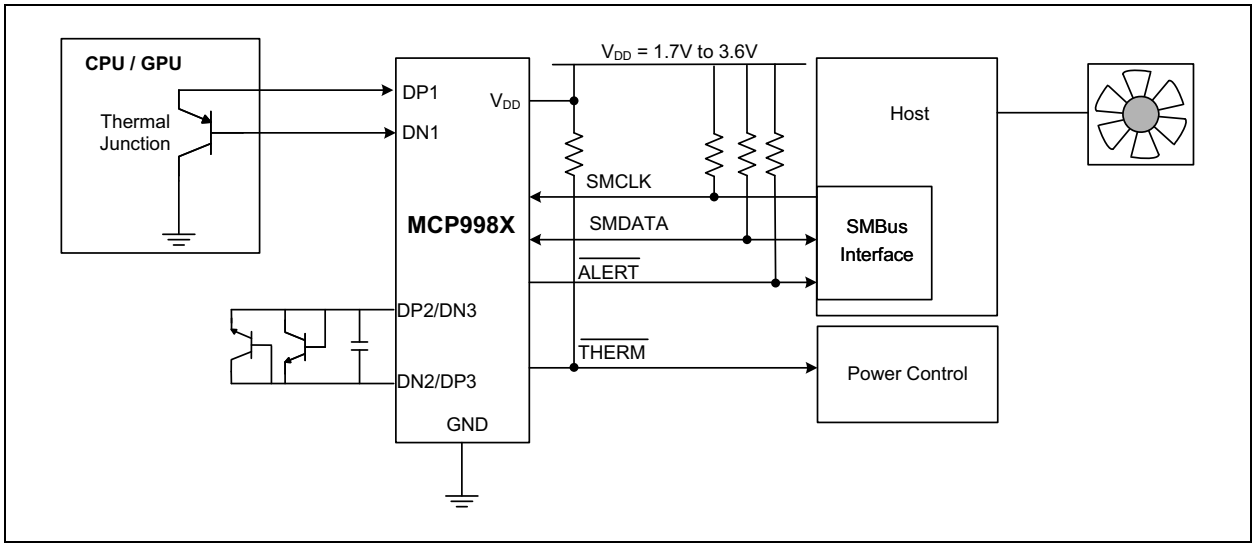


FIGURE 4-1: *MCP998X System Diagram.*

4.1 Power States

The MCP998X devices have two power states:

- Active (Run) state:
  In this state, the ADC is converting on all temperature channels at the programmed conversion rate. The temperature data is updated at the end of every conversion and the limits are checked. In the Active state, writing to the One-Shot Register will do nothing.
- Standby (One-shot) state:
  While the device is in Standby, the host can initiate a conversion cycle on demand by writing to the One-Shot register (see Register 5-5). After the conversion cycle is complete, the device will return to the Standby state.

Note:	The MCP998XD and MCP9933D devices do not support Standby (One-Shot) state.

4.2 Conversion Rates

The MCP998X/MCP9933/MCP998XD/MCP9933D devices may be configured for different conversion rates based on the system requirements (see Register 5-15). The default conversion rate is four conversions per second. Other available conversion rates are shown in Table 4-1.

So as not to interfere with the hardware shutdown feature, the MCP998XD devices cannot be set with a conversion rate slower than 1 conversion per second.

TABLE 4-1: CONVERSION RATE

CONV[3:0]					Conversions per Second
HEX	3	2	1	0	
0h	0	0	0	0	1/16 (**Note 1**)
1h	0	0	0	1	1/8 (**Note 1**)
2h	0	0	1	0	1/4 (**Note 1**)
3h	0	0	1	1	1/2 (**Note 1**)
4h	0	1	0	0	1
5h	0	1	0	1	2
6h	0	1	1	0	4 (default)
7h	0	1	1	1	8
8h	1	0	0	0	16
9h	1	0	0	1	32
Ah	1	0	1	0	64
Bh - Fh	All others				1

Note 1: Not available on MCP998XD devices.

4.3 Dynamic Averaging

Dynamic averaging causes the MCP998X/MCP9933/MCP998XD/MCP9933D to measure the external diode channels for an extended time based on the selected conversion rate. This functionality can be disabled for increased power savings at the lower conversion rates (see Register 5-14, DA_ENA bit). When dynamic averaging is enabled, the device will automatically adjust the sampling and measurement time for the external diode channels. This allows the device to average 2x to 16x longer than the normal 11-bit operation (nominally 25 ms per channel) while still maintaining the selected conversion rate. The benefits of dynamic averaging are improved noise rejection due to the longer integration time as well as less random variation of the temperature measurement.

When enabled, the dynamic averaging applies when a one-shot command is issued. The device will perform the desired averaging during the one-shot operation according to the selected conversion rate.

When enabled, the dynamic averaging will affect the average supply current based on the chosen conversion rate, as shown in Figure 4-2, and the averaging factor based on an 11-bit operation as seen in Table 4-2.

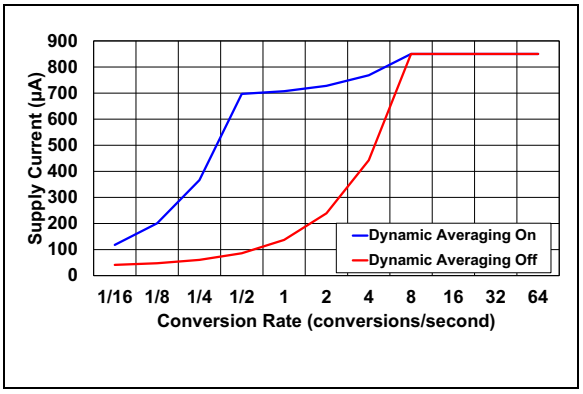


FIGURE 4-2: *Supply Current vs. Conversion Rate.*

TABLE 4-2: SUPPLY CURRENT VS. CONVERSION RATE

Conversion Rate	Averaging Factor (based on 11-bit operation)	
	Dynamic Averaging State	
	Enabled (default)	Disabled
1/16 sec.	16x	1x
1/8 sec.	16x	1x
1/4 sec.	16x	1x
1/2 sec.	16x	1x
1/sec.	16x	1x
2/sec.	16x	1x
4/sec. (default)	8x	1x
8/sec.	4x	1x
16/sec.	2x	1x
32/sec.	1x	1x
64/sec.	0.5x	0.5x

Note: The conversion time for external diodes will be dependent upon the chosen conversion rate. For the slower conversion rates, the external diode channels will convert over a longer period of time to provide more averaging at the cost of increased supply current.

4.4 Device Option Selection

TABLE 4-3: DEVICE SELECT BIT ASSIGNMENT

Device	Address	Device ID
MCP9982-1	4C	3101h
MCP9982-2	4D	3101h
MCP9982-A	Addr. decode	3101h
MCP9983-1	4C	3107h
MCP9983-2	4D	3107h
MCP9983-A	Addr. decode	3107h
MCP9984-1	4C	3104h
MCP9984-2	4D	3104h
MCP9984-A	Addr. decode	3104h
MCP9985-1	4C	3105h
MCP9985-2	4D	3105h
MCP9985-A	Addr. decode	3105h
MCP9933-1	4C	3103h
MCP9933-2	4D	3103h
MCP9933-A	Addr. decode	3103h
MCP9982D-1	4C	3109h
MCP9982D-2	4D	3109h
MCP9983D-1	4C	310Fh
MCP9983D-2	4D	310Fh
MCP9984D-1	4C	310Ch
MCP9984D-2	4D	310Ch
MCP9985D-1	4C	310Dh
MCP9985D-2	4D	310Dh
MCP9933D-1	4C	310Bh
MCP9933D-2	4D	310Bh

4.5 Hottest Diode Recognition Comparison

At the end of every measurement cycle, the MCP998X/MCP9933/MCP998XD/MCP9933D compares all of the user-selectable Internal and External Diode channels to determine which of these channels is reporting the hottest temperature. The hottest temperature is stored in the Hottest Temperature Registers and the appropriate status bit in the Hottest Status Register is set (see Register 5-28). If multiple temperature channels measure the same temperature and are equal to the hottest temperature, the hottest status will be based on the measurement order.

As an optional feature, the MCP998X/MCP9933/MCP998XD/MCP9933D can also flag an event if the hottest temperature channel changes by enabling the REMHOT (Remember Hottest) bit (see Register 5-33). For example, suppose that External Diode channels 1, 3, and 4 are programmed to be compared in the Hottest Diode Recognition Comparison. If the External Diode 1 channel reports the hottest temperature of the three, its temperature is copied into the Hottest Temperature Registers (in addition to the External Diode 1 Temperature registers, see Register 5-26 and Register 5-27) and it is flagged in the Hottest Status bit. If, on the next measurement, the External Diode 3 channel temperature has increased such that it is now the hottest temperature, the MCP998X/MCP9933/MCP998XD/MCP9933D can flag this event as an interrupt condition and assert the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin.

4.6 $\overline{\text{THERM}}$ Output

The $\overline{\text{THERM}}$ output is asserted independently of the $\overline{\text{ALERT}}$ output and cannot be masked. Whenever any of the measured temperatures exceed the user programmed Therm Limit values (see Register 5-12 and Register 5-13) for the programmed number of consecutive measurements, the $\overline{\text{THERM}}$ output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drop below the Therm Limit minus the Therm Hysteresis (also programmable, see Register 5-16).

When the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is asserted, the Therm status bits will likewise be set (see Register 5-21 and Register 5-25). Reading these bits will not clear them until the $\overline{\text{THERM}}$ pin is deasserted. Once the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is deasserted, the THERM status bits will be automatically cleared.

4.7 $\overline{\text{ALERT}}/\overline{\text{THERM}}$ Output

The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is an open-drain output and requires a pull-up resistor to V_{DD} and has two modes of operation: Interrupt mode and THERM (Comparator) mode. The mode of the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ output is selected via the ALERT/THERM bit (see Register 5-14, AT/THM bit).

4.7.1 $\overline{\text{ALERT}}/\overline{\text{THERM}}$ PIN INTERRUPT MODE

When configured to operate in interrupt mode, the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin asserts low when an out of limit measurement (less than or equal to the LOW limit or greater than the HIGH limit) is detected on any diode or when a diode fault is detected. The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin will remain asserted until the appropriate status bits are cleared.

The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin can be masked by setting the MASK_ALL bit. Once the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin has been masked, it will be deasserted and remain deasserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is masked will update the Status Register normally. There are also individual channel masks (see Register 5-31, addresses '33h' and '34h').

The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is used as an interrupt signal or as an I^2C Alert signal that allows an I^2C client to communicate an error condition to the host. One or more $\overline{\text{ALERT}}/\overline{\text{THERM}}$ outputs can be hard-wired together.

4.7.2 $\overline{\text{ALERT}}/\overline{\text{THERM}}$ PIN IN THERM MODE

When the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is configured to operate in THERM mode, it will be asserted if any of the measured temperatures exceeds the respective high limit. The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the Therm Hysteresis value.

When the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is asserted in THERM mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is deasserted. Once the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is dasserted, the status bits will be automatically cleared.

The MASK_ALL bit will not block the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin in this mode; however, the individual channel masks will prevent the respective channel from asserting the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin.

4.8 Temperature Measurement

The MCP998X/MCP9933/MCP998XD/MCP9933D can monitor the temperature of up to four externally connected diodes. Each external diode channel is configured with Resistance Error Correction and Beta Compensation based on user settings and system requirements.

For MCP998XD and MCP9933D devices, Resistance Error Correction, Beta Compensation, and Ideality Factor features cannot be turned off or changed, and the Conversion Rate cannot be set slower than one conversion per second. This ensures that the Hardware Shutdown feature cannot be overridden

The device contains programmable High, Low, and Therm limits for all measured temperature channels. If the measured temperature goes below the Low limit or above the High limit, the ALERT/THERM pin can be asserted (based on user settings). If the measured temperature meets or exceeds the Therm Limit, the THERM/ADDR or SYS_SHDN pin is asserted unconditionally, providing two tiers of temperature detection.

4.9 System Shutdown

The MCP998XD devices contain a hardware configured temperature limit circuit that controls the SYS_SHDN pin. The threshold temperature is determined by the pull-up resistors on both the SYS_SHDN and ALERT/THERM pins. Note, Standby and One-Shot modes cannot be enabled in device configurations including system shutdown functionality.

TABLE 4-4: PULL-UP RESISTOR VALUES

Pull-Up Resistor (1%)	Bit 2	Bit 1	Bit 0
4.7k	0	0	0
6.8k	0	0	1
10k	0	1	0
15k	0	1	1
22k	1	0	0
33k	1	0	1

The final temperature decode is the responsibility of the digital block. The overall decode is shown in Table 4-5.

TABLE 4-5: TEMPERATURE SELECT ENCODING

SYS_SHDN Pull-Up Decode			ALERT Pull-Up Decode			Combined Decode (HEX)	Threshold Temperature
2	1	0	2	1	0	—	
0	0	0	0	0	0	00h	+77°C
0	0	0	0	0	1	01h	+78°C
0	0	0	0	1	0	02h	+79°C
0	0	0	0	1	1	03h	+80°C
0	0	0	1	0	0	04h	+81°C
0	0	0	1	0	1	05h	+82°C
0	0	1	0	0	0	08h	+83°C
0	0	1	0	0	1	09h	+84°C
0	0	1	0	1	0	0Ah	+85°C
0	0	1	0	1	1	0Bh	+86°C
0	0	1	1	0	0	0Ch	+87°C
0	0	1	1	0	1	0Dh	+88°C
0	1	0	0	0	0	10h	+89°C
0	1	0	0	0	1	11h	+90°C
0	1	0	0	1	0	12h	+91°C
0	1	0	0	1	1	13h	+92°C
0	1	0	1	0	0	14h	+93°C
0	1	0	1	0	1	15h	+94°C
0	1	1	0	0	0	18h	+95°C
0	1	1	0	0	1	19h	+96°C
0	1	1	0	1	0	1Ah	+97°C
0	1	1	0	1	1	1Bh	+98°C
0	1	1	1	0	0	1Ch	+99°C
0	1	1	1	0	1	1Dh	+100°C
1	0	0	0	0	0	20h	+101°C
1	0	0	0	0	1	21h	+102°C
1	0	0	0	1	0	22h	+103°C
1	0	0	0	1	1	23h	+104°C
1	0	0	1	0	0	24h	+105°C
1	0	0	1	0	1	25h	+106°C
1	0	1	0	0	0	28h	+107°C
1	0	1	0	0	1	29h	+108°C
1	0	1	0	1	0	2Ah	+109°C
1	0	1	0	1	1	2Bh	+110°C
1	0	1	1	0	0	2Ch	+111°C
1	0	1	1	0	1	2Dh	+112°C

The Hardware Shutdown circuitry measures the External Diode 1 Channel and compares it against the Hardware Thermal Shutdown Limit. The THERM consecutive alert counter (set to four by default for the SYS_SHDN pin) applies to this comparison. If the temperature meets or exceeds the limit for the number of consecutive measurements, the SYS_SHDN pin is asserted. The SYS_SHDN pin remains asserted until the temperature drops below the limit minus 10°C. As well, all of the measurement channels (including the External Diode 1 channel) can be configured to assert the SYS_SHDN pin. If a channel is configured to assert the SYS_SHDN pin, the temperature on the measured channel must exceed the programmed therm limit value. This is treated in the same way as the ALERT/THERM output in THERM mode.

4.10 Limit Registers

The MCP998X/MCP9933/MCP998XD/MCP9933D contains both high and low limits for all temperature channels. If the measured temperature exceeds the high limit, then the corresponding status bit is set and the ALERT/THERM pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the ALERT/THERM pin is asserted.

The data format for the limits must match the selected data format for the temperature so that if the extended temperature range is used, the limits must be programmed in the extended data format (see **Section 4.20 "External Diode Connections"**).

The Limit registers with multiple addresses are fully accessible at either address.

When the device is in Standby state, updating the Limit registers will have no effect until the next conversion cycle occurs. This can be initiated via a write to the One-shot Register (see Register 5-5) or by clearing the RUN/STOP bit (see Register 5-14).

4.11 Limit Register interaction

The various Limit registers of the device interact based on both external conditions present on the diode pins as well as changes in register bits in the I^2C interface.

4.11.1 HIGH LIMIT REGISTER

The High Limit Status Register (see Register 5-23) contains the status bits that are set when a temperature channel high limit is exceeded. If any of these bits are set, then the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits. Reading from the register will also clear the HIGH status bit in the Status Register (see Register 5-21).

The ALERT/THERM pin will be asserted if the programmed number of consecutive alert counts have been met and any of these status bits are set.

The status bits will remain set until read unless the ALERT/THERM pin is configured as a THERM (comparator) output (see **Section 4.7.2 "ALERT/THERM Pin in THERM Mode"**).

4.11.2 LOW LIMIT REGISTER

The Low Limit Status Register contains the status bits that are set when a temperature channel drops below the low limit. If any of these bits are set, then the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits.

The ALERT/THERM pin will be asserted if the programmed number of consecutive alert counts have been met and any of these status bits are set.

If the auto-detection circuitry is disabled, these bits will determine the beta configuration setting that is used for their respective channels.

The status bits will remain set until read unless the ALERT/THERM pin is configured as a THERM (comparator) output (see **Section 4.7.2 "ALERT/THERM Pin in THERM Mode"**).

4.11.3 THERM LIMIT REGISTER

The Therm Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature exceeds the Therm Limit, the THERM pin for MCP998X devices or the SYS_SHDN pin for MCP998XD devices is asserted. The limit setting must match the chosen data format of the temperature reading registers.

Unlike the ALERT/THERM pin, the THERM/ADDR or SYS_SHDN pin cannot be masked. Additionally, the THERM/ADDR or SYS_SHDN pin will be released once the temperature drops below the corresponding threshold minus the Therm Hysteresis.

4.12 Beta Compensation

The MCP998X/MCP9933/MCP998XD/MCP9933D Family is configured to monitor the temperature of basic diodes (e.g., 2N3904) or CPU thermal diodes. It automatically detects the type of external diode (CPU diode or diode connected transistor) and determines the optimal setting to reduce temperature errors introduced by beta variation. Compensating for this error is also known as implementing the transistor or BJT model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

User programmable Beta Compensation is only supported on External Diode 1 and 2. If APD is enabled on the MCP9984/4D and MCP9985/5D, External Diode 2 will lock to Diode mode. So as not to interfere with the Hardware Shutdown feature, Beta Compensation on External Channel 1 on the MCP998XD devices cannot be changed and is locked to the default setting.

At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETA(N)[3:0] bits (see Register 5-31) will be automatically updated to indicate the current setting. This is the default for MCP998X/MCP9933/MCP998XD/MCP9933D devices.

Care should be taken when setting the BETA(N)[3:0] bits when the auto-detection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an embedded processor), the BETA(N)[3:0] bits should be set to '1111b'.

TABLE 4-6: CPU BETA VALUES

DI_BETA[3:0]				I_C - EMC4 IP (µA)	Minimum Beta
3	2	1	0		
0	0	0	0	0.47	0.050
0	0	0	1	0.6	0.066
0	0	1	0	0.8	0.087
0	0	1	1	1	0.114
0	1	0	0	1.3	0.150
0	1	0	1	1.6	0.197
0	1	1	0	2.1	0.260
0	1	1	1	2.5	0.342
1	0	0	0	3.1	0.449
1	0	0	1	3.7	0.591
1	0	1	0	4.4	0.778
1	0	1	1	5	1.024
1	1	0	0	5.7	1.348
1	1	0	1	6.4	1.773
1	1	1	0	7	2.333
1	1	1	1	9.5	Diode Mode

4.13 Resistance Error Correction (REC)

Parasitic resistance in series with the external diodes will limit the accuracy obtainable from temperature measurement devices. The voltage developed across this resistance by the switching diode currents causes the temperature measurement to read higher than the true temperature. Contributors to series resistance are PCB trace resistance, on die (i.e., on the processor) metal resistance, bulk resistance in the base and emitter of the temperature transistor. Typically, the error caused by series resistance is +0.7°C per Ω. The MCP998X/MCP9933/MCP998XD/MCP9933D automatically corrects up to 100Ω of series resistance. See the typical performance of the Resistance Error Correction feature in Figure 4-3.

This feature can be turned on and off in the Configuration Register (see Register 5-14).

So as not to interfere with the Hardware Shutdown feature, Resistance Error Correction on External Channel 1 on the MCP998XD devices cannot be changed and is locked to the default setting (ON).

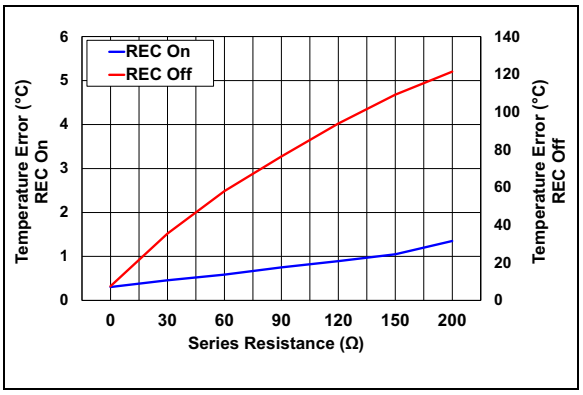


FIGURE 4-3: *Resistance Error Correction.*

4.14 Programmable External Diode Ideality Factor

The MCP998X/MCP9933/MCP998XD/MCP9933D is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the MCP998X/MCP9933/MCP998XD/MCP9933D family provides a 6-bit register for each external diode where the ideality factor of the diode used is programmed to eliminate errors across all temperatures.

When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

So as not to interfere with the Hardware Shutdown feature, Ideality Factor on External Channel 1 on the MCP998XD devices cannot be changed and is locked to the default setting (12h).

These registers (see Register 5-32) store the ideality factors that are applied to the external diodes. Table 4-7 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting Microchip.

TABLE 4-7: IDEALITY FACTOR LOOK-UP TABLE (DIODE MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9949	18h	1.0159	28h	1.0371
09h	0.9962	19h	1.0172	29h	1.0384
0Ah	0.9975	1Ah	1.0185	2Ah	1.0397
0Bh	0.9988	1Bh	1.0200	2Bh	1.0410
0Ch	1.0001	1Ch	1.0212	2Ch	1.0423
0Dh	1.0014	1Dh	1.0226	2Dh	1.0436
0Eh	1.0027	1Eh	1.0239	2Eh	1.0449
0Fh	1.0040	1Fh	1.0253	2Fh	1.0462
10h	1.0053	20h	1.0267	30h	1.0475
11h	1.0066	21h	1.0280	31h	1.0488
12h	1.0080	22h	1.0293	32h	1.0501
13h	1.0093	23h	1.0306	33h	1.0514
14h	1.0106	24h	1.0319	34h	1.0527
15h	1.0119	25h	1.0332	35h	1.0540
16h	1.0133	26h	1.0345	36h	1.0553
17h	1.0146	27h	1.0358	37h	1.0566

For CPU substrate transistors that require the BJT transistor model, the ideality factor behaves slightly differently than for discrete diode-connected transistors. Refer to Table 4-8 when using a CPU substrate transistor.

TABLE 4-8: SUBSTRATE DIODE IDEALITY FACTOR LOOK-UP TABLE (BJT MODEL)

Setting	Factor	Setting	Factor	Setting	Factor
08h	0.9869	18h	1.0079	28h	1.0291
09h	0.9882	19h	1.0092	29h	1.0304
0Ah	0.9895	1Ah	1.0105	2Ah	1.0317
0Bh	0.9908	1Bh	1.0120	2Bh	1.0330
0Ch	0.9921	1Ch	1.0132	2Ch	1.0343
0Dh	0.9934	1Dh	1.0146	2Dh	1.0356
0Eh	0.9947	1Eh	1.0159	2Eh	1.0369
0Fh	0.9960	1Fh	1.0173	2Fh	1.0382
10h	0.9973	20h	1.0187	30h	1.0395
11h	0.9986	21h	1.0200	31h	1.0408
12h	1.0000	22h	1.0213	32h	1.0421
13h	1.0013	23h	1.0226	33h	1.0434
14h	1.0026	24h	1.0239	34h	1.0447
15h	1.0039	25h	1.0252	35h	1.0460
16h	1.0053	26h	1.0265	36h	1.0473
17h	1.0066	27h	1.0278	37h	1.0486

Note: When measuring a 65 nm Intel® CPU, the Ideality Setting should be the default '12h'. When measuring a 45 nm Intel CPU, the Ideality Setting should be '15h'.

4.15 Diode Faults

The MCP998X/MCP9933/MCP998XD/MCP9933D detects an open on the DP and DN pins, and a short across the DP and DN pins. For each temperature measurement made, the device checks for a diode fault on the external diode channel(s). When a diode fault is detected, the ALERT/THERM pin asserts (unless masked) and the temperature data reads '00h' in the MSB and LSB registers (note: the low limit will not be checked). A diode fault is defined as one of the following: an open between DP and DN, a short from V_{DD} to DP, or a short from V_{DD} to DN.

If a short occurs across DP and DN or a short occurs from DP to GND, the low limit status bit is set and the ALERT/THERM pin asserts (unless masked). This condition is indistinguishable from a temperature measurement of 0.000°C (-64°C in extended range) resulting in temperature data of '00h' in the MSB and LSB registers.

If a short from DN to GND occurs (with a diode connected), temperature measurements will continue as normal with no alerts.

4.16 Consecutive Alerts

The MCP998X/MCP9933/MCP998XD/MCP9933D contains multiple consecutive alert counters. One set of counters applies to the ALERT/THERM pin and the second set of counters applies to the THERM/ADDR pin for MCP998X devices or SYS_SHDN pin for MCP998XD devices. Each temperature measurement channel has a separate consecutive alert counter for each of the ALERT/THERM and THERM/ADDR or SYS_SHDN pins. All counters are user programmable and determine the number of consecutive measurements that a temperature channel(s) must be out-of-limit or reporting a diode fault before the corresponding pin is asserted.

The Consecutive Alert Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the ALERT/THERM, THERM/ADDR or SYS_SHDN pins are asserted (see Register 5-17).

An out-of-limit condition (i.e., HIGH, LOW, or FAULT) occurring on the same temperature channel in consecutive measurements will increment the consecutive alert counter. The counters will also be reset if no out-of-limit condition or diode fault condition occurs in a consecutive reading.

When the ALERT/THERM pin is configured as an interrupt, when the consecutive alert counter reaches its programmed value, the following will occur: the STATUS bit(s) for that channel and the last error condition(s) (i.e., E1HIGH, or E2LOW and/or E2FAULT) will be set to '1', the ALERT/THERM pin will be asserted, the consecutive alert counter will be cleared, and measurements will continue.

When the ALERT/THERM pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature exceeds the High Limit. Additionally, once the consecutive alert counter reaches the programmed limit, the ALERT/THERM pin will be asserted, but the counter will not be reset. It will remain set until the temperature drops below the High Limit minus the Therm Hysteresis value.

Channels that are not enabled are not included in the consecutive alert checking. The signal logic chain is: Limit -> Counter -> Status -> Mask -> Pin (THERM and ALERT).

For example, if the CALRT[2:0] bits are set for four consecutive alerts on an MCP998X/MCP9933/MCP998XD/MCP9933D device, the high limits are set at +70°C, and none of the channels are masked, then the ALERT/THERM pin will be asserted after the following four measurements:

- Internal Diode reads +71°C and both the external diodes read +69°C. Consecutive alert counter for INT is incremented to 1.
- Both the Internal Diode and the External Diode 1 read +71°C and External Diode 2 read +68°C. Consecutive alert counter for INT is incremented to 2 and for EXT1 is set to 1.
- The External Diode 1 reads +71°C and both Internal Diode and External Diode 2 read +69°C. Consecutive alert counters for INT and EXT2 are cleared and EXT1 is incremented to 2.
- The Internal Diode reads +71°C and both external diodes read +71°C. Consecutive alert counter for INT is set to 1, EXT2 is set to 1, and EXT1 is incremented to 3.
- The Internal Diode reads +71°C and both external diodes read +71°C. Consecutive alert counter for INT is incremented to 2, EXT2 is set to 2, and EXT1 is incremented to 4. The appropriate status bits are set for EXT1 and the ALERT/THERM pin is asserted. EXT1 counter is reset to 0 and all other counters hold the last value until the next temperature measurement.

All temperature channels use this value to set the respective counters. The consecutive Therm counter is incremented whenever any measurement exceeds the corresponding Therm Limit.

If the temperature drops below the Therm Limit, the counter is reset. If a number of consecutive measurements above the Therm Limit occurs, the THERM/ADDR or SYS_SDHDN pin is asserted low.

Once the THERM/ADDR or SYS_SDHDN pin has been asserted, the consecutive therm counter will not reset until the corresponding temperature drops below the Therm Limit minus the Therm Hysteresis value.

All temperature channels use the Consecutive Alert/THERM Setting value to set the respective counters. The bits are decoded as shown in Table 4-9. The default setting for the ALERT/THERM pin is one consecutive out-of-limit conversions, while the default setting for the THERM/ADDR pin is four.

When the ALERT/THERM pin is in Comparator mode, the Low Limit and Diode fault will bypass the consecutive alert counter and set the appropriate status bits but will not assert the ALERT/THERM pin.

When a value is written to this register that is not defined in Table 4-9, the command is ignored and the last valid value is maintained.

TABLE 4-9: CONSECUTIVE ALERT/THERM SETTINGS

2	1	0	Number of Consecutive Out of Limit Measurements
0	0	0	1 (default for CALRT[3:1])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM[6:4]))

4.17 Digital Filter

To reduce the effect of noise and temperature spikes on the reported temperature, the External Diode 1 channel uses a programmable digital filter. This filter can be configured as Level 1, Level 2, or Disabled (default). The typical filter performance is shown in Figure 4-4 and Figure 4-5. The Filter Configuration Register (Register 5-19) controls the digital filter on the External Diode 1 channel. It will apply after the digital block has taken the appropriate 11 bits based on the dynamic averaging.

TABLE 4-10: FILTER SETTINGS

FILTER[1:0]		Averaging
1	0	
0	0	Disabled (default)
0	1	Level 1 (note1)
1	0	Level 1 (note1)
1	1	Level 2 (note2)

Note 1: Filtering Level 1 corresponds to 4x attenuation of a temperature spike.

2: Filtering Level 2 corresponds to 8x attenuation of a temperature spike.

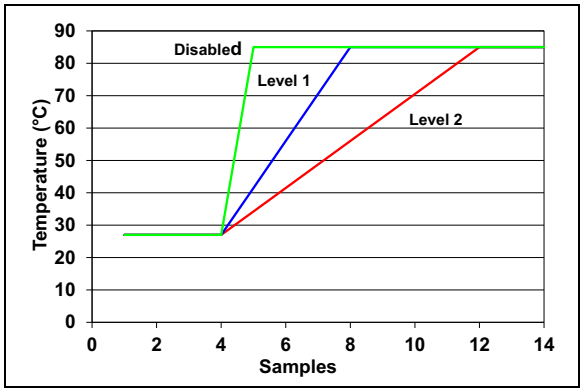


FIGURE 4-4: *Temperature Filter Step Response.*

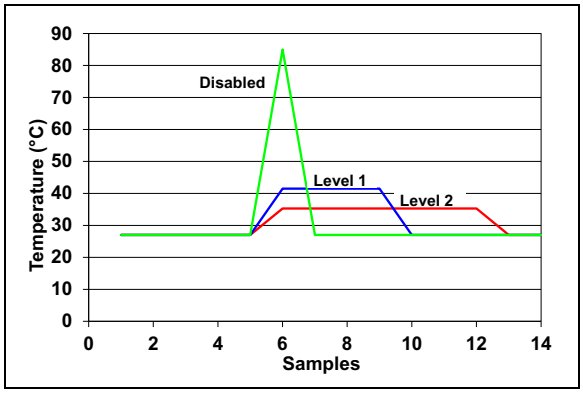


FIGURE 4-5: *Temperature Filter Impulse Response.*

The filter consists of a running average on the external diode channel. The Level 1 filter is a running average of the previous four samples while the Level 2 filter is a running average of the previous eight samples. For the first measurement immediately after power-up, the filter will be filled with the results of the first measurement. After this, the filter is operated normally. Any temperature comparisons will be done with the filtered results that are stored in the user register.

4.18 Temperature Measurement Results and Data

The temperature measurement results are stored in the Internal and External Temperature registers. Both external and internal temperature measurements are stored in 11-bit format with the eight (8) most significant bits stored in a high byte register and the three (3) least significant bits stored in the three (3) MSB positions of the low byte register. All other bits of the low byte register are set to zero.

The MCP998X/MCP9933/MCP998XD/MCP9933D has two selectable temperature ranges (see Register 5-14). The default range is from 0°C to +127°C and the temperature is represented as binary number able to report a temperature from 0°C to +127.875°C in 0.125°C steps.

The extended range is an extended temperature range from -64°C to +191°C. The data format is a binary number offset by 64°C. The extended range is used to measure temperature diodes with a large known offset (such as embedded processor diodes) where the diode temperature plus the offset would be equivalent to a temperature higher than +127°C.

Table 4-11 shows the default and extended range formats.

TABLE 4-11: TEMPERATURE DATA FORMAT

Temperature (°C)	Default Range (0°C to +127°C)	Extended Range (-64°C to +191°C)
Diode Fault	000 0000 0000	000 0000 0000
-64	000 0000 0000	000 0000 0000 **(Note 2)**
-1	000 0000 0000	001 1111 1000
0	000 0000 0000 **(Note 1)**	010 0000 0000
0.125	000 0000 0001	010 0000 0001
1	000 0000 1000	010 0000 1000

Note 1: In default range, all temperatures < 0°C will be reported as 0°C.

2: In the extended range, all temperatures < -64°C will be reported as -64°C.

3: For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

4: For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

TABLE 4-11: TEMPERATURE DATA FORMAT (CONTINUED)

Temperature (°C)	Default Range (0°C to +127°C)	Extended Range (-64°C to +191°C)
64	010 0000 0000	100 0000 0000
65	010 0000 1000	100 0000 1000
127	011 1111 1000	101 1111 1000
127.875	011 1111 1111	101 1111 1111
128	011 1111 1111 (Note 3)	110 0000 0000
190	011 1111 1111	111 1111 0000
191	011 1111 1111	111 1111 1000
≥ 191.875	011 1111 1111	111 1111 1111 (Note 4)

Note 1: In default range, all temperatures < 0°C will be reported as 0°C.

2: In the extended range, all temperatures < -64°C will be reported as -64°C.

3: For the default range, all temperatures > +127.875°C will be reported as +127.875°C.

4: For the extended range, all temperatures > +191.875°C will be reported as +191.875°C.

4.19 Anti-Parallel Diode Connections

The MCP9984/85/33 and MCP9984D/85D/33D support reading two external diodes on the same set of pins (ex. DP1/DN1 and DP2/DN2). These diodes are connected as shown in Figure 4-6. Due to the anti-parallel connection of these diodes, both diodes will be reverse biased by a VBE voltage (approximately 0.7V). Because of this reverse bias, only discrete thermal diodes (such as a 2N3904) are recommended to be placed on these pins.

4.20 External Diode Connections

The MCP9982 and MCP9982D can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an embedded processor diode. The diodes can be connected as indicated in Figure 4-6.

The MCP9983 and MCP9983D can be configured to measure a CPU substrate transistor, a discrete 2N3904 thermal diode, or an embedded processor diode on the External Diode 1 or External Diode 2 channels. For the MCP9984 and MCP9984D, External Diode 2 and External Diode 3 channels are configured to measure a pair of discrete anti-parallel diodes (shared on pins DP2 and DN2). The supported configurations for the external diode channels are shown in Figure 4-6.

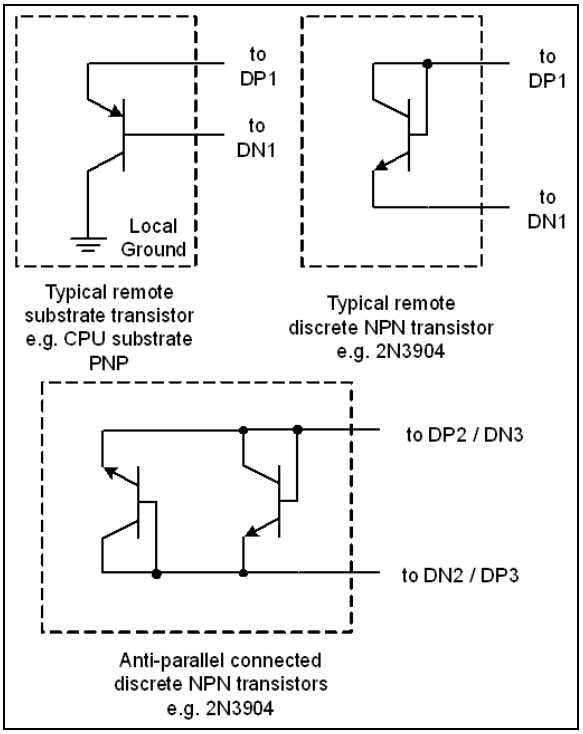


FIGURE 4-6: *Diode Configurations.*

To reduce error in noisier environments, use a capacitive filter in parallel with the external diodes. For an NPN transistor, a typical value of 2.2 nF is recommended. For a PNP transistor, the maximum value should be 470 pF. See Figure 4-7 for typical capacitive filter effects on temperature accuracy.

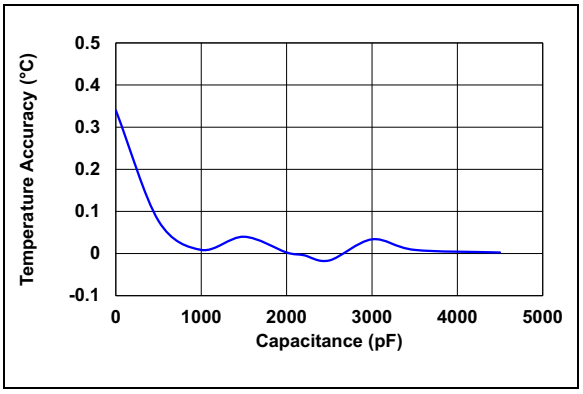


FIGURE 4-7: *Capacitive Filter Plot.*

5.0 SYSTEM MANAGEMENT BUS PROTOCOL

The MCP998X/MCP9933/MCP998XD/MCP9933D communicates with a host controller through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 1-1. Stretching of the SMCLK signal is supported; however, the MCP998X/MCP9933/MCP998XD/MCP9933D will not stretch the clock signal.

5.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

5.2 SMBus Address and RD / WR Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD/WR indicator bit. If this RD/WR bit is a logic '0', the SMBus Host is writing data to the client device. If this RD/WR bit is a logic '1', the SMBus Host is reading data from the client device.

The MCP998X/MCP9933/MCP998XD/MCP9933D responds to the client address '1001_100xb' for '-1' parts and '1001_101xb' for '-2' parts. Multiple addressing options are available for the '-A' parts, as shown in Table 5-1.

TABLE 5-1: I²C ADDRESS DECODE

$\overline{\text{THERM}}$ Pull-Up Res. (1%)	I²C 7-Bit Client Address
4.7k	1111_100xb
6.8k	1011_100xb
10k	1001_100xb
15k	1101_100xb
22k	0011_100xb
33k	0111_100xb

5.3 SMBus Data Bytes

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

5.4 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives. This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

The Host will NACK (not acknowledge) the last data byte to be received from the client by holding the SMBus data line high after the 8th data bit has been sent. For the Block Read protocol, the Host will ACK each data byte that it receives except the last data byte.

5.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the MCP998X/MCP9933/MCP998XD/MCP9933D detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

5.6 SMBus Time-out

The MCP998X/MCP9933/MCP998XD/MCP9933D includes an SMBus time-out feature. Following a 30 ms period of inactivity on the SMBus where the SMCLK pin is held low, the device will time-out and reset the SMBus interface.

The Time-Out function defaults to disabled. It can be enabled by setting the TIMEOUT bit in the Consecutive Alert register (see Register 5-17).

5.7 SMBus and I²C Compliance

The major difference between SMBus and I²C devices is highlighted here. For complete compliance information, refer to the SMBus 3.1 specification.

1. Minimum frequency for SMBus communications is 10 kHz.
2. The client protocol will reset if the clock is held low longer than 30 ms.
3. I²C devices do support the Alert Response Address functionality (which is optional for SMBus).

5.8 SMBus Protocols

The MCP998X/MCP9933/MCP998XD/MCP9933D is SMBus 3.1 compatible. The device supports Write Byte, Read Byte, and Block Read. All of the below protocols use the convention in Table 5-2.

The register address determines whether a single byte or multiple byte (block) operation is run. For a single byte operation, the MSB of the register address is set to '0'; for a multiple byte operation, it is set to '1'. The addresses quoted in the register map and throughout this data sheet assume single byte operation. For multiple byte operations, the user must set the MSB of each register address to '1'.

TABLE 5-2: SMBUS PROTOCOL

Data Sent to Device	Data Sent to the Host
(# of bits sent)	(# of bits sent)

TABLE 5-3: MEMORY BLOCKS

Memory Block	Reg. Location	# of Bytes
All Temp.	80h - 89h	10
All Status	90h - 97h	8

The Write Byte is used to write one byte of data to a specific register, as shown in Tables 5-4.

TABLE 5-4: WRITE BYTE PROTOCOL

START	ADDR	WR	ACK	ADDR	ACK	DATA	ACK	STOP

5.9 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in Tables 5-5.

TABLE 5-5: READ BYTE PROTOCOL

START	ADDR	WR	ACK	ADDR	ACK

START	ADDR	RD	ACK	ADDR	ACK	DATA	NACK	STOP

5.10 Block Read

The Block Read Process Call (Tables 5-6) is a two-part message. The call begins with a client address and a write condition. After the pointer location is set, the client should acknowledge (ACK). In the second part of the message, the host issues a start condition followed by a 7-bit client address with the read command. The client will ACK followed by byte count. The byte count is the number of user readable bytes, from the pointer location to the end of the memory block. When the host acknowledges following the byte count the client will clock out the data byte at the current pointer location. For every subsequent ACK by the host, the pointer will increment to the location of the next user-readable data byte. The Block read process is ended by a NACK followed by a STOP command from the host. If the host continues to ACK beyond the last register location for the memory block, the pointer will stay at the last register location within the memory block and the device will output 'FFh'.

TABLE 5-6: BLOCK READ PROTOCOL

START	ADDR	WR	ACK	ADDR	ACK

START	ADDR	RD	ACK	COUNT	ACK	DATA1	ACK	DATA2

ACK	DATA3	...	DATAN	NACK	STOP

5.11 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 5-7.

TABLE 5-7: SEND BYTE PROTOCOL

START	CLIENT ADDR.	WR	ACK	REG. ADDR.	ACK	STOP

5.12 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register as shown in Table 5-8.

TABLE 5-8: RECEIVE BYTE PROTOCOL

START	CLIENT ADDR.	RD	ACK	REG. DATA	NACK	STOP

5.13 Alert Response Address (ARA)

The MCP998X/MCP9933/MCP998XD/MCP9933D supports the Alert Response Address (ARA) protocol. A client-only device can signal the host through SMBALERT# that it wants to talk. The host processes the interrupt and simultaneously accesses all SMBALERT# devices through the Alert Response Address. Only the device(s) which pulled SMBALERT# low will acknowledge the Alert Response Address. The host performs a modified Receive Byte operation. The 7-bit device address provided by the client transmit device is placed in the seven most significant bits of the byte. The eighth bit (X) can be a zero or one.

TABLE 5-9: 7-BIT-ADDRESSABLE DEVICE RESPONDS TO ARA

START	ARA	RD	ACK	ADDR	X	NACK	STOP

5.14 THERM Pin Considerations

Because of the decode method used to determine the I^2C Address, it is important that the pull-up resistance on the $\overline{\text{THERM}}$/ADDR or $\overline{\text{SYS\_SHDN}}$ pin be within the tolerances shown in Table 5-1.

For t_{INT_T} after power-up, the $\overline{\text{THERM}}$/ADDR or $\overline{\text{SYS\_SHDN}}$ pin must not be pulled low or the I^2C address will not be decoded properly. If the system requirements do not permit these conditions, the $\overline{\text{THERM}}$/ADDR or $\overline{\text{SYS\_SHDN}}$ pin must be isolated from its hard-wired OR'd bus during this time.

One method of isolating this pin is shown in Figure 5-1.

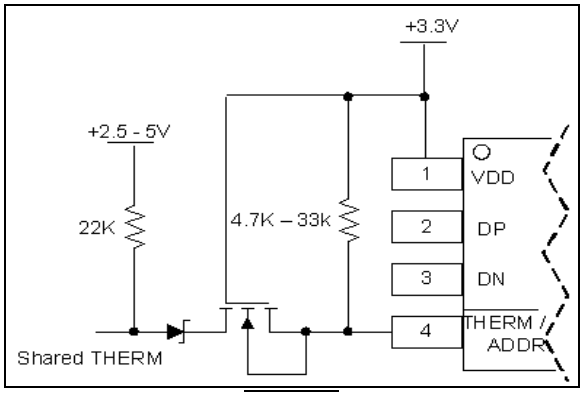


FIGURE 5-1: *$\overline{\text{THERM}}$ Pin Isolation.*

5.15 Register Description

Table 5-10 shows brief descriptions of MCP998X/MCP9933/MCP998XD/MCP9933D registers in hexadecimal order.

TABLE 5-10: REGISTER SET IN HEXADECIMAL ORDER

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
INT HIGH BYTE	00h	IHB7	IHB6	IHB5	IHB4	IHB3	IHB2	IHB1	IHB0	00h
INT LOW BYTE	01h	ILB2	ILB1	ILB0	—	—	—	—	—	00h
EXT1 HIGH BYTE	02h	E1HB7	E1HB6	E1HB5	E1HB4	E1HB3	E1HB2	E1HB1	E1HB0	00h
EXT1 LOW BYTE	03h	E1LB2	E1LB1	E1LB0	—	—	—	—	—	00h
EXT2 HIGH BYTE	04h	E2HB7	E2HB6	E2HB5	E2HB4	E2HB3	E2HB2	E2HB1	E2HB0	00h
EXT2 LOW BYTE	05h	E2LB2	E2LB1	E2LB0	—	—	—	—	—	00h
EXT3 HIGH BYTE	06h	E3HB7	E3HB6	E3HB5	E3HB4	E3HB3	E3HB2	E3HB1	E3HB0	00h
EXT3 LOW BYTE	07h	E3LB2	E3LB1	E3LB0	—	—	—	—	—	00h
EXT4 HIGH BYTE	08h	E4HB7	E4HB6	E4HB5	E4HB4	E4HB3	E4HB2	E4HB1	E4HB0	00h
EXT4 LOW BYTE	09h	E4LB2	E4LB1	E4LB0	—	—	—	—	—	00h
ONE SHOT	0Ah	ONSH7	ONSH6	ONSH5	ONSH4	ONSH3	ONSH2	ONSH1	ONSH0	00h
INT DIODE HIGH LIMIT	0Bh	IDHL7	IDHL6	IDHL5	IDHL4	IDHL3	IDHL2	IDHL1	IDHL0	55h (85°C)
INT DIODE LOW LIMIT	0Ch	IDLL7	IDLL6	IDLL5	IDLL4	IDLL3	IDLL2	IDLL1	IDLL0	00h (0°C)
EXT1 HIGH LIMIT HIGH BYTE	0Dh	E1HLH7	E1HLH6	E1HLH5	E1HLH4	E1HLH3	E1HLH2	E1HLH1	E1HLH0	55h (85°C)
EXT1 HIGH LIMIT LOW BYTE	0Eh	E1HLL2	E1HLL1	E1HLL0	—	—	—	—	—	00h
EXT1 LOW LIMIT HIGH BYTE	0Fh	E1LLH7	E1LLH6	E1LLH5	E1LLH4	E1LLH3	E1LLH2	E1LLH1	E1LLH0	00h (0°C)
EXT1 LOW LIMIT LOW BYTE	10h	E1LLL2	E1LLL1	E1LLL0	—	—	—	—	—	00h
EXT2 HIGH LIMIT HIGH BYTE	11h	E2HLH7	E2HLH6	E2HLH5	E2HLH4	E2HLH3	E2HLH2	E2HLH1	E2HLH0	55h (85°C)
EXT2 HIGH LIMIT LOW BYTE	12h	E2HLL2	E1HLL1	E1HLL0	—	—	—	—	—	00h
EXT2 LOW LIMIT HIGH BYTE	13h	E2LLH7	E2LLH6	E2LLH5	E2LLH4	E2LLH3	E2LLH2	E2LLH1	E2LLH0	00h (0°C)

TABLE 5-10: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
EXT2 LOW LIMIT LOW BYTE	14h	E2LLL2	E2LLL1	E2LLL0	—	—	—	—	—	00h
EXT3 HIGH LIMIT HIGH BYTE	15h	E3HLH7	E3HLH6	E3HLH5	E3HLH4	E3HLH3	E3HLH2	E3HLH1	E3HLH0	55h (85°C)
EXT3 HIGH LIMIT LOW BYTE	16h	E3HLL2	E3HLL1	E3HLL0	—	—	—	—	—	00h
EXT3 LOW LIMIT HIGH BYTE	17h	E3LLH7	E3LLH6	E3LLH5	E3LLH4	E3LLH3	E3LLH2	E3LLH1	E3LLH0	00h (0°C)
EXT3 LOW LIMIT LOW BYTE	18h	E3LLL2	E3LLL1	E3LLL0	—	—	—	—	—	00h
EXT4 HIGH LIMIT HIGH BYTE	19h	E4HLH7	E4HLH6	E4HLH5	E4HLH4	E4HLH3	E4HLH2	E4HLH1	E4HLH0	55h (85°C)
EXT4 HIGH LIMIT LOW BYTE	1Ah	E4HLL2	E4HLL1	E4HLL0	—	—	—	—	—	00h
EXT4 LOW LIMIT HIGH BYTE	1Bh	E4LLH7	E4LLH6	E4LLH5	E4LLH4	E4LLH3	E4LLH2	E4LLH1	E4LLH0	00h (0°C)
EXT4 LOW LIMIT LOW BYTE	1Ch	E4LLL2	E4LLL1	E4LLL0	—	—	—	—	—	00h
INT DIODE THERM LIMIT	1Dh	IDTHL7	IDTHL6	IDTHL5	IDTHL4	IDTHL3	IDTHL2	IDTHL1	IDTHL0	55h (85°C)
EXT1 THERM LIMIT	1Eh	E1THL7	E1THL6	E1THL5	E1THL4	E1THL3	E1THL2	E1THL1	E1THL0	55h (85°C)
EXT2 THERM LIMIT	1Fh	E2THL7	E2THL6	E2THL5	E2THL4	E2THL3	E2THL2	E2THL1	E2THL0	55h (85°C)
EXT3 THERM LIMIT	20h	E3THL7	E3THL6	E3THL5	E3THL4	E3THL3	E3THL2	E3THL1	E3THL0	55h (85°C)
EXT4 THERM LIMIT	21h	E4THL7	E4THL6	E4THL5	E4THL4	E4THL3	E4THL2	E4THL1	E4THL0	55h (85°C)
CONFIG	22h	MSKAL	R/S	AT/THM	RECD1/2	RECD3/4	RANGE	DA_ENA	APDD	00h
CONVERT	24h	—	—	—	—	CONV3	CONV2	CONV1	CONV0	06h (4/sec)
THRM HYS	25h	THMH7	THMH6	THMH5	THMH4	THMH3	THMH2	THMH1	THMH0	0Ah (10°C)
CONSEC ALRT	26h	TMOUT	CTHM2	CTHM1	CTHM0	CALRT2	CALRT1	CALRT0	—	70h

TABLE 5-10: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
DIODE ALRT MASK	27h	—	—	—	E4MSK	E3MSK	E2MSK	E1MSK	INTMSK	00h
FILTER SEL	28h	—	—	—	—	—	—	FLTER1	FLTER0	00h
HOTTEST CONFIG	29h	—	—	REM-HOT	E4ENB	E3ENB	E2ENB	E1ENB	IENB	00h
STATUS	2Ah	-	HOTCHG	BUSY	HIGH	LOW	FAULT	ETHRM	ITHRM	00h
EXT DIODE FAULT STS	2Bh	—	—	—	E4FLT	E3FLT	E2FLT	E1FLT	—	00h
HIGH LIMIT STATUS	2Ch	—	—	—	E4HIGH	E3HIGH	E2HIGH	E1HIGH	IHIGH	00h
LOW LIMIT STATUS	2Dh	—	—	—	E4LOW	E3LOW	E2LOW	E1LOW	ILOW	00h
THERM LIMIT STATUS	2Eh	HWSD-LIM	—	—	E4THM	E3THM	E2THM	E1THM	ITHM	00h
HOTTEST DIODE HIGH BYTE	2Fh	HDHB7	HDHB6	HDHB5	HDHB4	HDHB3	HDHB2	HDHB1	HDHB0	00h
HOTTEST DIODE LOW BYTE	30h	HDLB2	HDLB1	HDLB0	—	—	—	—	—	00h
HOTTEST STATUS	31h	—	—	—	E4HOT	E3HOT	E2HOT	E1HOT	IHOT	00h
SW THER-MAL LIMIT CONFIG	32h	—	—	—	E4SYS	E3SYS	E2SYS	E1SYS	INTSYS	00h
THERM SHDN TEMP	33h	SDNL7	SDNL6	SDNL5	SDNL4	SDNL3	SDNL2	SDNL1	SDNL0	00h
EXT1 BETA CONFIG	34h	—	—	—	ENBL1	BETA13	BETA12	BETA11	BETA10	00h
EXT2 BETA CONFIG	35h	—	—	—	ENBL2	BETA23	BETA22	BETA21	BETA20	08h
EXT1 IDE-ALITY FAC-TOR	36h	—	—	IDEL15	IDEL14	IDEL13	IDEL12	IDEL11	IDEL10	12h (1.008)
EXT2 IDE-ALITY FAC-TOR	37h	—	—	IDEL25	IDEL24	IDEL23	IDEL22	IDEL21	IDEL20	12h (1.008)
EXT3 IDE-ALITY FAC-TOR	38h	—	—	IDEL35	IDEL34	IDEL23	IDEL32	IDEL31	IDEL30	12h (1.008)
EXT4 IDE-ALITY FAC-TOR	39h	—	—	IDEL45	IDEL44	IDEL43	IDEL42	IDEL41	IDEL40	12h (1.008)
PRODUCT ID HIGH BYTE	3Eh	PIDHB7	PIDHB6	PIDHB5	PIDHB4	PIDHB3	PIDHB2	PIDHB1	PIDHB0	31h
PRODUCT ID LOW BYTE	3Fh	PIDLB7	PIDLB6	PIDLB5	PIDLB4	PIDLB3	PIDLB2	PIDLB1	PIDLB0	xxh

TABLE 5-10: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
MANUFAC-TURER ID HIGH BYTE	40h	MCH-P_IDHB7	MCH-P_IDHB6	MCH-P_IDHB5	MCH-P_IDLB4	MCH-P_IDLB3	MCH-P_IDHB2	MCH-P_IDHB1	MCH-P_IDHB0	00h
MANUFAC-TURER ID LOW BYTE	41h	MCH-P_IDLB7	MCH-P_IDLB6	MCH-P_IDLB5	MCH-P_IDLB4	MCH-P_IDLB3	MCH-P_IDLB2	MCH-P_IDLB1	MCH-P_IDLB0	54h
REVISION ID	42h	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	00h
SCRATCH-PD1	43h	SPD17	SPD16	SPD15	SPD14	SPD13	SPD12	SPD11	SPD10	00h
SCRATCH-PD2	44h	SPD27	SPD26	SPD25	SPD24	SPD23	SPD22	SPD21	SPD20	00h
TEMPERATURE MEMORY BLOCK (BELOW)										
INT HIGH BYTE	80h	IHB7	IHB6	IHB5	IHB4	IHB3	IHB2	IHB1	IHB0	00h
INT LOW BYTE	81h	ILB2	ILB1	ILB0	—	—	—	—	—	00h
EXT1 HIGH BYTE	82h	E1HB7	E1HB6	E1HB5	E1HB4	E1HB3	E1HB2	E1HB1	E1HB0	00h
EXT1 LOW BYTE	83h	E1LB2	E1LB1	E1LB0	—	—	—	—	—	00h
EXT2 HIGH BYTE	84h	E2HB7	E2HB6	E2HB5	E2HB4	E2HB3	E2HB2	E2HB1	E2HB0	00h
EXT2 LOW BYTE	85h	E2LB2	E2LB1	E2LB0	—	—	—	—	—	00h
EXT3 HIGH BYTE	86h	E3HB7	E3HB6	E3HB5	E3HB4	E3HB3	E3HB2	E3HB1	E3HB0	00h
EXT3 LOW BYTE	87h	E3LB2	E3LB1	E3LB0	—	—	—	—	—	00h
EXT4 HIGH BYTE	88h	E4HB7	E4HB6	E4HB5	E4HB4	E4HB3	E4HB2	E4HB1	E4HB0	00h
EXT4 LOW BYTE	89h	E4LB2	E4LB1	E4LB0	—	—	—	—	—	00h
STATUS MEMORY BLOCK (BELOW)										
STATUS	90h	—	HOTCHG	BUSY	HIGH	LOW	FAULT	ETHRM	ITHRM	00h
EXT DIODE FAULT STS	91h	—	—	—	E4FLT	E3FLT	E2FLT	E1FLT	—	00h
HIGH LIMIT STATUS	92h	—	—	—	E4HIGH	E3HIGH	E2HIGH	E1HIGH	IHIGH	00h
LOW LIMIT STATUS	93h	—	—	—	E4LOW	E3LOW	E2LOW	E1LOW	ILOW	00h
THERM LIMIT STATUS	94h	—	—	—	E4THM	E3THM	E2THM	E1THM	ITHM	00h
HOTTEST DIODE HIGH BYTE	95h	HDHB7	HDHB6	HDHB5	HDHB4	HDHB3	HDHB2	HDHB1	HDHB0	80h

TABLE 5-10: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)

Register Name	Reg. Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR Value
HOTTEST DIODE LOW BYTE	96h	HDLB2	HDLB1	HDLB0	—	—	—	—	—	00h
HOTTEST STATUS	97h	—	—	—	E4HOT	E3HOT	E2HOT	E1HOT	IHOT	00h

5.16 Data Read Interlock

When any temperature channel high byte register is read, the corresponding low byte is copied into an internal ‘shadow’ register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

REGISTER 5-1: INTERNAL HIGH BYTE REGISTER (ADDRESS 00H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
IHB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 7-0 **IHB[7:0]:**
Unsigned binary diode temperature reading

REGISTER 5-2: INTERNAL LOW BYTE REGISTER (ADDRESS 01H)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
ILB[7:5]			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writeable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = bit is set	‘0’ = Bit is cleared	x = Bit in unknown

bit 7-5 **ILB[7:5]:**
Fractional portion of the Internal Diode Temperature to be added to the value at register 00h
111 = 0.875 °C
110 = 0.750 °C
101 = 0.625 °C
100 = 0.500 °C
011 = 0.375 °C
010 = 0.250 °C
001 = 0.125 °C
000 = 0.000 °C

bit 4-0 Unimplemented: Read as ‘0’

REGISTER 5-3: EXT(N) HIGH BYTE REGISTER (ADDRESSES 02H,04H,06H,08H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
EXT(N)HB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT(N)HB[7:0]:**
Unsigned binary integer value of the External Diode 'N' temperature reading, where N = 1 to 4, depending on the device.

REGISTER 5-4: EXT(N) LOW BYTE REGISTER (ADDRESSES 03H,05H,07H,09H)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
EXT(N)LB[7:5]			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT(N)LB[7:5]**:
Fractional portion of the External Diode Temperature to be added to the value at the respective External Diode High Byte register (see Register 5-3).
111 = 0.875 °C
110 = 0.750 °C
101 = 0.625 °C
100 = 0.500 °C
011 = 0.375 °C
010 = 0.250 °C
001 = 0.125 °C
000 = 0.000 °C

bit 4 Unimplemented: Read as '0'

REGISTER 5-5: ONE SHOT REGISTER (ADDRESS 0AH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ONSH[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ONSH[7:0]**:
When the device is in the Standby state, writing to the One-shot Register will initiate a conversion cycle and update the temperature measurements. Writing to the One Shot Register while the device is in the Active state or when the BUSY bit is set in the Status Register Register 5-21 (2Ah) will have no effect. For MCP998XD devices, this register does not affect operation since all MCP998XD devices cannot enter Standby state.

REGISTER 5-6: INTERNAL DIODE HIGH LIMIT REGISTER (ADDRESS 0BH)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
IDHL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IDHL[7:0]**:
Unsigned binary integer value of the Internal Diode's High temperature limit, programmable by the user.

REGISTER 5-7: INTERNAL DIODE LOW LIMIT REGISTER (ADDRESS 0CH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IDLL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IDLL[7:0]**:
Integer value of the Internal Diode's Low temperature limit, programmable by the user.

REGISTER 5-8: EXT(N) HIGH LIMIT HIGH BYTE REGISTER (ADDRESSES 0DH, 11H, 15H, 19H)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
EXT(N)HLBH[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT(N)HLBH[7:0]**:
Integer value of the External Diode N High temperature limit's high byte, where N = 1 to 4 depending on device.

REGISTER 5-9: EXT(N) HIGH LIMIT LOW BYTE REGISTER (ADDRESSES 0EH, 12H, 16H, 1AH)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
EXT(N)HLLB[7:5]			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT(N)HLLB[7:5]**:
Fractional portion of the High Limit Temperature to be added to the value at the respective high byte registers.
111 = 0.875 °C
110 = 0.750 °C
101 = 0.625 °C
100 = 0.500 °C
011 = 0.375 °C
010 = 0.250 °C
001 = 0.125 °C
000 = 0.000 °C

bit 4-0 Unimplemented: Read as '0'.

REGISTER 5-10: EXT(N) LOW LIMIT HIGH BYTE REGISTER (ADDRESSES 0FH, 13H, 17H, 1BH)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
EXT(N)LLHB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT(N)LLHB[7:0]**:
Integer portion of External Diode N Low temperature Limit, where N = 1 to 4 depending on device.

REGISTER 5-11: EXT(N) LOW LIMIT LOW BYTE REGISTER (ADDRESSES 10H, 14H, 18H, 1CH)

R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0
EXT(N)LLLB[7:5]			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **EXT(N)LLLB[7:5]:**
Fractional portion of the Low Limit Temperature to be added to the value at the respective High Byte registers, where N = 1 to 4.
111 = 0.875 °C
110 = 0.750 °C
101 = 0.625 °C
100 = 0.500 °C
011 = 0.375 °C
010 = 0.250 °C
001 = 0.125 °C
000 = 0.000 °C

bit 4-0 **Unimplemented:** Read as '0'.

REGISTER 5-12: INTERNAL DIODE $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESS 1DH)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
IDTHL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **IDTHL[7:0]**: Integer value of the Internal Diode $\overline{\text{THERM}}$ Limit

REGISTER 5-13: EXT(N) $\overline{\text{THERM}}$ LIMIT REGISTER (ADDRESSES 1EH, 1FH, 20H, 21H)

R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1
EXT(N)THL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **EXT(N)THL[7:0]**: Integer value of the External Diode N $\overline{\text{THERM}}$ temperature limits, where N = 1 to 4.

REGISTER 5-14: CONFIGURATION REGISTER (ADDRESS 22H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MSKAL	R/S	AT/THM	RECD1/2	RECD3/4	RANGE	DA_ENA	APDD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **MSKAL**: MASK_ALL Bit

Masks the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin from asserting when the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is in Interrupt mode. This bit has no effect when the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is in THERM (Comparator) mode. Turning on the MASK_ALL bit will not deassert the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin.

1 = The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is masked and will not be asserted for any interrupt condition when the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is in Interrupt mode. The Status Registers will be updated normally

0 = The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin will be asserted.

bit 6 **R/S:** RUN/STANDBY Bit

Controls Active/Standby states. This bit is locked to '0' on all MCP998XD devices.

1 = The device is in Standby state and not converting (unless a one-shot has been commanded).

0 = The device is in Active state and converting on all channels.

bit 5 **AT/THM:** ALERT/THERM Bit

Controls the operation of the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin. (**Note 1**)

1 = The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin acts in THERM (Comparator) mode as described in **Section 4.7.2 "ALERT/THERM Pin in THERM Mode"**. In this mode the MASK_ALL bit is ignored

0 = The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin acts in interrupt mode as described in **Section 4.7.1 "ALERT/THERM Pin Interrupt Mode"**

bit 4 **RECD1/2:** Resistance Error Correction 1/2 Bits

Toggles the Resistance Error Correction (REC) for External Channel 1 on the MCP9982/3/4/2D/3D/4D and External Channels 1 and 2 on the MCP9985/33/5D/33D (**Note 2**).

1 = REC is disabled for External Channel 1 on the MCP9982/3/4 and External Channels 1 and 2 on the MCP9985/33/5D/33D.

0 = REC is enabled for External Channel 1 on the MCP9982/3/4/2D/3D/4D and External Channels 1 and 2 on the MCP9985/33/5D/33D.

bit 3 **RECD3/4:** Resistance Error Correction 3/4 Bits

Toggles the Resistance Error Correction (REC) for External Channel 2 on the MCP9983/3D, External Channels 2 and 3 on the MCP9984/4D and External Channels 3 and 4 on the MCP9985/5D.

1 = REC is disabled for External Channel 2 on the MCP9983/3D, External Channels 2 and 3 on the MCP9984/4D, and External Channels 3 and 4 on the MCP9985/5D.

0 = REC is enabled for External Channel 2 on the MCP9983/3D, External Channels 2 and 3 on the MCP9984/4D, and External Channels 3 and 4 on the MCP9985/5D.

bit 2 **RANGE:**

Configures the measurement range and data format of the temperature channels (**Note 3**).

1 = The temperature measurement range is -64°C to +191.875°C and the data format is offset binary (see **Table 4-11**)

0 = The temperature measurement range is 0°C to +127.875°C and the data format is binary

Note 1: When the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is in $\overline{\text{THERM}}$ (Comparator) mode, each channel has a consecutive counter OR'ed to assert the $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin. The $\overline{\text{ALERT}}/\overline{\text{THERM}}$ pin is deasserted after one measurement is below the High Limit minus the Therm Hysteresis.

2: REC on External Channel 1 on MCP998XD devices cannot be disabled and is locked to '0'.

3: The maximum ambient temperature while the device is operating is +125°C.

REGISTER 5-14: CONFIGURATION REGISTER (ADDRESS 22H) (CONTINUED)

bit 1 **DA_ENA:** Dynamic Averaging Enable bit
Enables the Dynamic Averaging feature on all temperature channels.
1 = The Dynamic Averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 4-1
0 = The Dynamic Averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion). For higher conversion rates, this averaging factor will be reduced as shown in Table 4-2

bit 0 **APDD:** Anti-Parallel Diode Operation bit
Disables the anti-parallel diode operation, only allowing each APD pin set to bias and measure one diode (only applicable to the MCP9984/5/33 and MCP9984D/5D/33D).
1 = Anti-parallel diode mode is disabled. Only one external diode will be measured on the channels capable of APD (ex. DP1/DN2 and DP2/DN1).
0 = Anti-parallel diode mode is enabled. Two external diodes will be measured on the channels capable of APD (ex. DP1/DN2 and DP2/DN1).

Note 1: When the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin is in $\overline{\text{THERM}}$ (Comparator) mode, each channel has a consecutive counter OR'ed to assert the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin. The $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin is deasserted after one measurement is below the High Limit minus the Therm Hysteresis.

2: REC on External Channel 1 on MCP998XD devices cannot be disabled and is locked to '0'.

3: The maximum ambient temperature while the device is operating is +125°C.

REGISTER 5-15: CONVERT REGISTER (ADDRESS 24H)

U-0	U-0	U-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0
—	—	—	—	CONV[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 Unimplemented: will be read as '0'.

bit 3-0 **CONV[3:0]:**
See **Section 4.2 "Conversion Rates"**:
0000 = 1/16
0001 = 1/8
0010 = 1/4
0011 = 1/2
0100 = 1
0101 = 2
0110 = 4 (default)
0111 = 8
1000 = 16
1001 = 32
1010 = 64
All other configurations = 1

REGISTER 5-16: $\overline{\text{THERM}}$ LIMIT HYSTERESIS REGISTER (ADDRESS 25H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
THMH[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **THMH[7:0]:**
Integer value of the $\overline{\text{THERM}}$ Limit hysteresis (see **Section 4.8 "Temperature Measurement"**).

REGISTER 5-17: CONSECUTIVE ALERT REGISTER (ADDRESS 26H)

R/W-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	U-0
TMOUT	CTHM[6:4]			CALRT[3:1]			—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TMOUT:** TIMEOUT Bit
Enables the time-out and idle functionality of the I^2C protocol.
1 = The I^2C time-out and idle functionality are enabled. The I^2C interface will time-out if the clock line is held low for longer than 30 ms.
0 = The I2C time-out and idle functionality are disabled. The I^2C interface will not time-out if the clock line is held low for longer than 30 ms.

bit 6-4 **CTHM[6:4]:**
Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the THERM/ADDR or SYS_SHDN pin is asserted.
000 = 1
001 = 2
011 = 3
111 = 4

bit 3-1 **CALRT[3:1]:**
Determines the number of consecutive measurements that must exceed the corresponding Therm Limit before the ALERT/THERM pin is asserted.
000 = 1
001 = 2
011 = 3
111 = 4

bit 0 **Unimplemented:** Read as '0'.

The Channel Mask Register controls individual channel masking. When a channel is masked, the ALERT/THERM pin will not be asserted when the masked channel reads a diode fault or out of limit error. The channel mask does not mask the THERM/ADDR pin.

REGISTER 5-18: DIODE ALERT MASK REGISTER (ADDRESS 27H)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	E4MSK	E3MSK	E2MSK	E1MSK	INTMSK
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 Unimplemented: will be read as '0'.

bit 4 **E4MSK:** E4MASK Bit
Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin from asserting when the External Diode 4 channel is out of limit or reports a diode fault.
1 = The External Diode 4 channel will not cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode 4 channel will cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.

bit 3 **E3MSK:** E3MASK Bit
Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin from asserting when the External Diode 3 channel is out of limit or reports a diode fault.
1 = The External Diode 3 channel will not cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode 3 channel will cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.

bit 2 **E2MSK:** E2MASK Bit
Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin from asserting when the External Diode 2 channel is out of limit or reports a diode fault.
1 = The External Diode 2 channel will not cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode 2 channel will cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.

bit 1 **E1MSK:** E1MASK Bit
Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin from asserting when the External Diode 1 channel is out of limit or reports a diode fault.
1 = The External Diode 1 channel will not cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.
0 = The External Diode 1 channel will cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit or reports a diode fault.

bit 0 **INTMSK:** INTMASK Bit
Masks the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin from asserting when the Internal Diode temperature is out of limit.
1 = The Internal Diode channel will not cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit.
0 = The Internal Diode channel will cause the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin to be asserted if it is out of limit.

REGISTER 5-19: FILTER SELECTION REGISTER (ADDRESS 28H)

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	FLTER[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'.

bit 1-0 **FLTER[1:0]:**
Control the level of digital filtering that is applied to the External Diode 1 temperature measurement, as shown in Table 4-10.

REGISTER 5-20: HOTTEST DIODE RECOGNITION REGISTER (ADDRESS 29H)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	REMHOT	E4ENB	E3ENB	E2ENB	E1ENB	IENB
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'.

bit 5 **REMHOT:**
Enables the Remember Hottest function, so if the hottest diode changes, the $\overline{\text{ALERT}}$/$\overline{\text{THERM}}$ pin is set.
1 = Remember hottest function enabled
0 = Remember hottest function disabled

bit 4 **E4ENB:**
Enables External Diode 4 for Hottest Diode Recognition comparisons.
1 = External Diode 4 is enabled
0 = External Diode 4 is not enabled

bit 3 **E3ENB:**
Enables External Diode 3 for Hottest Diode Recognition comparisons.
1 = External Diode 3 is enabled
0 = External Diode 3 is not enabled

bit 2 **E2ENB:**
Enables External Diode 2 for Hottest Diode Recognition comparisons.
1 = External Diode 2 is enabled
0 = External Diode 2 is not enabled

bit 1 **E1ENB:**
Enables External Diode 1 for Hottest Diode Recognition comparisons.
1 = External Diode 1 is enabled
0 = External Diode 1 is not enabled

bit 0 **IENB:**
Enables the Internal Diode for Hottest Diode Recognition comparisons.
1 = Internal Diode is enabled
0 = Internal Diode is not enabled

REGISTER 5-21: STATUS REGISTER (ADDRESS 2AH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	HOTCHG	BUSY	HIGH	LOW	FAULT	ETHRM	ITHRM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unused:** Read as '0'.

bit 6 **HOTCHG:**
This bit indicates if the hottest channel has changed from the previous temperature measurement.
1 = The hottest channel has changed from the previous temperature measurement
0 = The hottest channel has not changed from the previous temperature measurement

bit 5 **BUSY:**
This bit indicates if the ADC is currently converting measured data.
1 = The ADC is currently converting measured data
0 = The ADC is not currently converting measured data

bit 4 **HIGH:**
This bit indicates if a temperature channel exceeds its programmed high limit. When set, this bit will assert the ALERT/THERM pin.
1 = Reported temperature is above the high limit
0 = Reported temperature is not above the high limit

bit 3 **LOW:**
This bit indicates if a temperature channel drops below its programmed low limit. When set, this bit will assert the ALERT/THERM pin.
1 = Reported temperature is below the low limit
0 = Reported temperature is not below the low limit

bit 2 **FAULT:**
This bit indicates when a external diode fault is detected. When set, this bit will assert the ALERT/THERM pin.
1 = Open circuit or short of a diode
0 = No fault reported

bit 1 **ETHRM:**
This bit indicates the External Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pin. This bit will remain set until the THERM/ADDR or SYS_SHDN pin is released at which point it will be automatically cleared.
1 = Reported temperature above the Therm limit
0 = Reported temperature is not above the Therm limit

bit 0 **ITHRM:**
This bit is set when the Internal Diode channel exceeds the programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pin. This bit will remain set until the THERM/ADDR or SYS_SHDN pin is released at which point it will be automatically cleared.
1 = Reported temperature above the Therm limit
0 = Reported temperature is not above the Therm limit

REGISTER 5-22: EXTERNAL DIODE FAULT STATUS REGISTER (ADDRESS 2BH)(Note 1)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	U-0
—	—	—	E4FLT	E3FLT	E2FLT	E1FLT	—
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unused:** Read as '0'.

bit 4 **E4FLT:**
This bit is set if the External Diode 4 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

bit 3 **E3FLT:**
This bit is set if the External Diode 3 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

bit 2 **E2FLT:**
This bit is set if the External Diode 2 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

bit 1 **E1FLT:**
This bit is set if the External Diode 1 channel reported a diode fault.
1 = Diode Fault condition present
0 = No Diode Fault present

bit 0 **Unimplemented:** Read as '0'.

Note 1: The External Diode Fault Register indicates which of the external diodes caused the FAULT bit in the Status Register to be set. This register is cleared when it is read (see **Section 4.15 "Diode Faults"**).

REGISTER 5-23: HIGH LIMIT STATUS REGISTER (ADDRESS 2CH)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0
—	—	—	E4HIGH	E3HIGH	E2HIGH	E1HIGH	IHIGH
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'.

bit 4 **E4HIGH:**
This bit is set when the External Diode 4 exceeds its programmed High Limit. Reading this register will also clear the HIGH bit.
1 = High Limit exceeded
0 = High Limit not exceeded

bit 3 **E3HIGH:**
This bit is set when the External Diode 3 exceeds its programmed High Limit. Reading this register will also clear the HIGH bit.
1 = High Limit exceeded
0 = High Limit not exceeded

bit 2 **E2HIGH:**
This bit is set when the External Diode 2 exceeds its programmed High Limit. Reading this register will also clear the HIGH bit.
1 = High Limit exceeded
0 = High Limit not exceeded

bit 1 **E1HIGH:**
This bit is set when the External Diode 1 exceeds its programmed High Limit. Reading this register will also clear the HIGH bit.
1 = High Limit exceeded
0 = High Limit not exceeded

bit 0 **IHIGH:**
This bit is set when the Internal Diode exceeds its programmed High Limit. Reading this register will also clear the HIGH bit.
1 = High Limit exceeded
0 = High Limit not exceeded

REGISTER 5-24: LOW LIMIT STATUS REGISTER (ADDRESS 2DH)

U-0	U-0	U-0	RC-0	RC-0	RC-0	RC-0	RC-0
—	—	—	E4LOW	E3LOW	E2LOW	E1LOW	ILOW
bit 7							bit 0

Legend:			
RC = Read-then-clear bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'.

bit 4 **E4LOW:**
This bit is set when the External Diode 4 exceeds its programmed Low Limit. Reading this register will also clear the LOW bit.
1 = Low Limit exceeded
0 = Low Limit not exceeded

bit 3 **E3LOW:**
This bit is set when the External Diode 3 exceeds its programmed Low Limit. Reading this register will also clear the LOW bit.
1 = Low Limit exceeded
0 = Low Limit not exceeded

bit 2 **E2LOW:**
This bit is set when the External Diode 2 exceeds its programmed Low Limit. Reading this register will also clear the LOW bit.
1 = Low Limit exceeded
0 = Low Limit not exceeded

bit 1 **E1LOW:**
This bit is set when the External Diode 1 exceeds its programmed Low Limit. Reading this register will also clear the LOW bit.
1 = Low Limit exceeded
0 = Low Limit not exceeded

bit 0 **ILOW:**
This bit is set when the Internal Diode exceeds its programmed Low Limit. Reading this register will also clear the LOW bit.
1 = Low Limit exceeded
0 = Low Limit not exceeded

REGISTER 5-25: THERM LIMIT STATUS REGISTER (ADDRESS 2EH)(Note 1)

R-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
HWSDLIM	—	—	E4THM	E3THM	E2THM	E1THM	ITHM
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **HWSDLIM:**
This bit is set when the External Diode 1 channel is above the Hardware Thermal Shutdown limit.

bit 6-5 **Unimplemented:** Read as '0'.

bit 4 **E4THM:**
This bit is set when the External Diode 4 channel exceeds its programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pins.
1 = THERM pin asserted
0 = THERM pin not asserted

bit 3 **E3THM:**
This bit is set when the External Diode 3 channel exceeds its programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pins.
1 = THERM pin asserted
0 = THERM pin not asserted

bit 2 **E2THM:**
This bit is set when the External Diode 2 channel exceeds its programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pins.
1 = THERM pin asserted
0 = THERM pin not asserted

bit 1 **E1THM:**
This bit is set when the External Diode 1 channel exceeds its programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pins.
1 = THERM pin asserted
0 = THERM pin not asserted

bit 0 **ITHM:**
This bit is set when the Internal Diode channel exceeds its programmed Therm Limit. When set, this bit will assert the THERM/ADDR or SYS_SHDN pins.
1 = THERM pin asserted
0 = THERM pin not asserted

Note 1: The Therm Limit Status Register contains the status bits that are set when a temperature channel Therm Limit is exceeded. If any of these bits are set, the THERM status bit in the Status Register is set. Reading from the Therm Limit Status Register will not clear the status bits. Once the temperature drops below the Therm Limit minus the Therm Hysteresis, the corresponding status bits will be automatically cleared. The THERM bit in the Status Register will be cleared when all individual channel THERM bits are cleared.

REGISTER 5-26: HOTTEST DIODE TEMPERATURE HIGH BYTE REGISTER (ADDRESS 2FH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
HDHB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **HDHB[7:0]:**
Integer value of the hottest diode's temperature reading from the most recent samples.

REGISTER 5-27: HOTTEST DIODE TEMPERATURE LOW BYTE REGISTER (ADDRESS 30H)

R-0	R-0	R-0	U-0	U-0	U-0	U-0	U-0
HDLB[7:5]			—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **HDLB[7:5]:**
Fractional portion of the hottest diode's temperature reading for the most recent sample period.
111 = 0.875 °C
110 = 0.750 °C
101 = 0.625 °C
100 = 0.500 °C
011 = 0.375 °C
010 = 0.250 °C
001 = 0.125 °C
000 = 0.000 °C

bit 4-0 **Unimplemented:** Read as '0'.

REGISTER 5-28: HOTTEST DIODE STATUS REGISTER (ADDRESS 31H)

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	E4HOT	E3HOT	E2HOT	E1HOT	IHOT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'.

bit 4 **E4HOT:**
Indicates External Diode 4 is the hottest.
1 = External Diode 4 is hottest
0 = External Diode 4 is not hottest

bit 3 **E3HOT:**
Indicates External Diode 3 is the hottest.
1 = External Diode 3 is hottest
0 = External Diode 3 is not hottest

bit 2 **E2HOT:**
Indicates External Diode 2 is the hottest.
1 = External Diode 2 is hottest
0 = External Diode 2 is not hottest

bit 1 **E1HOT:**
Indicates External Diode 1 is the hottest.
1 = External Diode 1 is hottest
0 = External Diode 1 is not hottest

bit 0 **IHOT:**
Indicates Internal Diode is the hottest.
1 = Internal Diode is hottest
0 = Internal Diode is not hottest

REGISTER 5-29: SOFTWARE THERMAL SHUTDOWN CONFIGURATION REGISTER (REGISTER 32H)

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	E4SYS	E3SYS	E2SYS	E1SYS	INTSYS
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'.

bit 4 **E4SYS:**
Configures the External Diode 4 channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on the Hardware Thermal Shutdown Limit.
0 = The External Diode 4 channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E4THRM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
1 = The External Diode 4 channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E4THRM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Hardware Thermal Shutdown Limit minus the Therm Hysteresis.

bit 3 **E3SYS:**
Configures the External Diode 3 channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on the Hardware Thermal Shutdown Limit.
0 = The External Diode 3 channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E3THRM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
1 = The External Diode 3 channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E3THRM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Hardware Thermal Shutdown Limit minus the Therm Hysteresis.

bit 2 **E2SYS:**
Configures the External Diode 2 channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on the Hardware Thermal Shutdown Limit.
0 = The External Diode 2 channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E2THRM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
1 = The External Diode 2 channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E2THRM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Hardware Thermal Shutdown Limit minus the Therm Hysteresis.

bit 1 **E1SYS:**
Configures the External Diode 1 channel to assert the $\overline{\text{SYS\_SHDN}}$ pin based on the Hardware Thermal Shutdown Limit.
0 = The External Diode 1 channel is not linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E1THRM status bit is set but the $\overline{\text{SYS\_SHDN}}$ pin is not asserted.
1 = The External Diode 1 channel is linked to the $\overline{\text{SYS\_SHDN}}$ pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the E1THRM status bit is set and the $\overline{\text{SYS\_SHDN}}$ pin is asserted. It will remain asserted until the temperature drops below its Hardware Thermal Shutdown Limit minus the Therm Hysteresis.

REGISTER 5-29: SOFTWARE THERMAL SHUTDOWN CONFIGURATION REGISTER (REGISTER 32H) (CONTINUED)

bit 0 **INTSYS:**
Configures the Internal Diode channel to assert the SYS_SHDN pin based on the Hardware Thermal Shutdown Limit.
0 = The Internal Diode channel is not linked to the SYS_SHDN pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the INTTHRM status bit is set but the SYS_SHDN pin is not asserted.
1 = The Internal Diode channel is linked to the SYS_SHDN pin. If the temperature exceeds the Hardware Thermal Shutdown Limit, the INTTHRM status bit is set and the SYS_SHDN pin is asserted. It will remain asserted until the temperature drops below its Hardware Thermal Shutdown Limit minus the Therm Hysteresis.

REGISTER 5-30: HARDWARE THERMAL SHUTDOWN LIMIT REGISTER (ADDRESS 33H)(Note 1)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
SDNL[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SDNL[7:0]:**
This read only register returns the Hardware Thermal Shutdown Limit selected by the value of the pull-up resistors on the ALERT/THERM and SYS_SHDN pins (see **Table 4-5**). The data represents the hardware set temperature in °C using the active temperature setting set by the RANGE bit in the Configuration Register. See **Table 4-11** for the data format.
When the External Diode 1 Temperature exceeds this limit, the SYS_SHDN pin is asserted and will remain asserted until the External Diode 1 temperature drops below this limit minus 10°C.

Note 1: Only available on MCP998XD devices.

REGISTER 5-31: EXT(N) BETA COMPENSATION CONFIGURATION REGISTER (ADDRESSES 34H, 35H)

U-0	U-0	U-0	R-0	R-1	R-0	R-0	R-0
—	—	—	ENBL(N)	BETA(N)[3:0]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **ENBL(N):**
Enables the Beta Compensation factor auto-detection function. N = 1 or 2, depending on the device.
1 = Auto-Beta detection for External Diode N is enabled
0 = Auto-Beta detection for External Diode N is disabled

bit 3-0 **BETA(N)[3:0]:**
These bits always reflect the current beta configuration settings. If auto-detection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect. See Table 4-6 for details.

REGISTER 5-32: EXT(N) PROGRAMMABLE IDEALITY FACTOR REGISTER (ADDRESSES 36H, 37H, 38H, 39H)

U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0
—	—	IDEAL(N)[5:0]					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IDEAL(N):[5:0]:**
External Diode N Ideality Factor, where N = 1 to 4 depending on device. See **Table 4-7** or **Table 4-8** for details.

REGISTER 5-33: PRODUCT ID HIGH BYTE REGISTER (ADDRESS 3EH)

R-0	R-0	R-1	R-1	R-0	R-0	R-0	R-1
PIDHB[15:8]							
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PIDHB[15:8]**
Hardwired as '31h'. See **Table 4-3**.

REGISTER 5-34: PRODUCT ID LOW BYTE REGISTER (ADDRESS 3FH)

R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
PIDLB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **PIDLB[7:0]**
Integer value of Product ID Low Byte. Product ID is a 16-bit expression: HBLB (31LBh). See **Table 4-3**.

REGISTER 5-35: MANUFACTURER ID HIGH BYTE REGISTER (ADDRESS 40H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
MCHP_IDHB[15:8]							
bit 15							bit 8

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MCHP_IDHB[15:8]:**
Hardwired as '00h'.

REGISTER 5-36: MANUFACTURER ID LOW BYTE REGISTER (ADDRESS 41H)

R-0	R-1	R-0	R-1	R-0	R-1	R-0	R-0
MCHP_IDLB[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **MCHP_IDLB[7:0]:**
Hardwired as '54h'.

REGISTER 5-37: REVISION REGISTER (ADDRESS 42H)

R-X	R-X	R-X	R-X	R-X	R-X	R-X	R-X
REV[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **REV[7:0]:**
DIE revision number.

REGISTER 5-38: SCRTCHPD(N): SCRATCHPAD REGISTER (ADDRESSES 43H AND 44H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPD(N)[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **SPD(N)[7:0]:**
User temporary storage registers, where N = 1 to 2.

6.0 PACKAGING INFORMATION

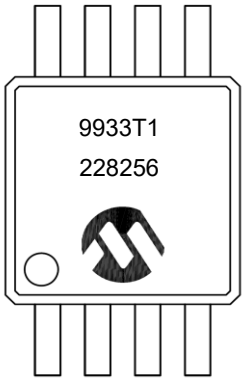
6.1 Package Marking Information

8-Lead MSOP
(**MCP9982/2D, MCP9933/33D**)

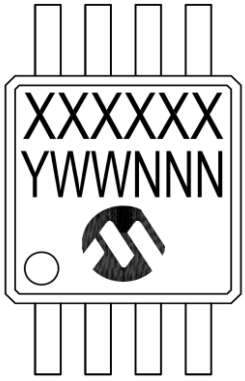
Part Number	Code
MCP9982T-1E/A3	9982T1
MCP9982T-2E/A3	9982T2
MCP9982T-AE/A3	9982TA
MCP9982DT-1E/A3	9982D1
MCP9982DT-2E/A3	9982D2
MCP9933T-1E/A3	9933T1
MCP9933T-2E/A3	9933T2
MCP9933T-AE/A3	9933TA
MCP9933DT-1E/A3	9933D1
MCP9933DT-2E/A3	9933D2

Note 1: Applies to MSOP8 parts only.
2: Automotive-qualified parts (part number ending in VAO) have the same code as their non-automotive counterpart.

Example



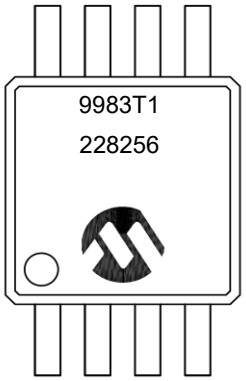
10-Lead MSOP
(**MCP9983/4/5/3D/4D/5D**)



Part Number	Code
MCP9983T-1E/E3	9983T1
MCP9983T-2E/E3	9983T2
MCP9983T-AE/E3	9983TA
MCP9983DT-1E/E3	9983D1
MCP9983DT-2E/E3	9983D2
MCP9984T-1E/E3	9984T1
MCP9984T-2E/E3	9984T2
MCP9984T-AE/E3	9984TA
MCP9984DT-1E/E3	9984D1
MCP9984DT-2E/E3	9984D2
MCP9985T-1E/E3	9985T1
MCP9985T- 2E/E3	9985T2
MCP9985T-AE/E3	9985TA
MCP9985DT-1E/E3	9985D1
MCP9985DT-2E/E3	9985D2

Note 1: Applies to MSOP10 parts only.
2: Automotive-qualified parts (part number ending in VAO) have the same code as their non-automotive counterpart.

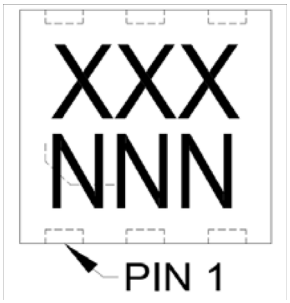
Example



Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.

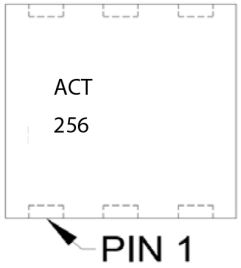
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead WDFN
(**MCP9982/2D, MCP9933/33D**)



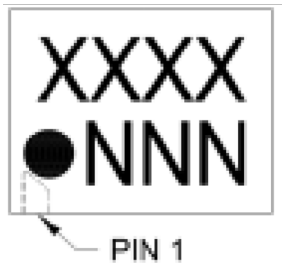
Part Number	Code
MCP9982T-1E/RW	ACT
MCP9982T-2E/RW	ACU
MCP9982T-AE/RW	ACV
MCP9982DT-1E/RW	ACX
MCP9982DT-2E/RW	ACY
MCP9933T-1E/RW	ADA
MCP9933T-2E/RW	ADB
MCP9933T-AE/RW	ADC
MCP9933DT-1E/RW	ADF
MCP9933DT-2E/RW	ADF

Example



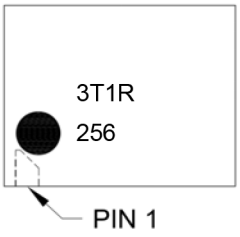
Note 1: Applies to WDFN parts only.
2: Automotive-qualified parts (part number ending in VAO) have the same code as their non-automotive counterpart.

10-Lead VDFN
(**MCP9983/4/5/3D/4D/5D**)



Part Number	Code
MCP9983T-1E/9R	3T1R
MCP9983T-2E/9R	3T2R
MCP9983T-AE/9R	3TAR
MCP9983DT-1E/9R	3D1R
MCP9983DT-2E/9R	3D2R
MCP9984T-1E/9R	4T1R
MCP9984T-2E/9R	4T2R
MCP9984T-AE/9R	4TAR
MCP9984DT-1E/9R	4D1R
MCP9984DT-2E/9R	4D2R
MCP9985T-1E/9R	5T1R
MCP9985T- 2E/9R	5T2R
MCP9985T-AE/9R	5TAR
MCP9985DT-1E/9R	5D1R
MCP9985DT-2E/9R	5D2R

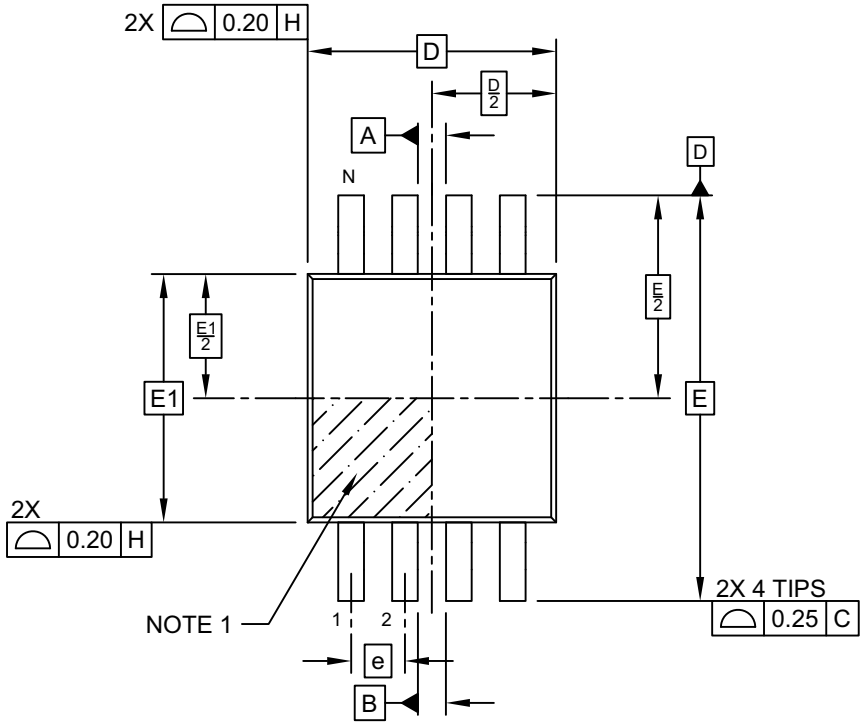
Example



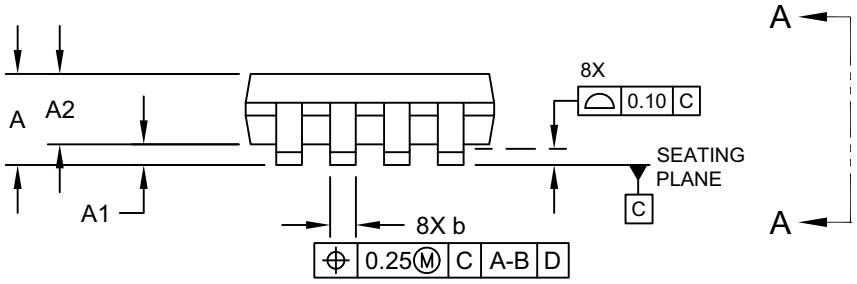
Note 1: Applies to VDFN10 parts only.
2: Automotive-qualified parts (part number ending in VAO) have the same code as their non-automotive counterpart.

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

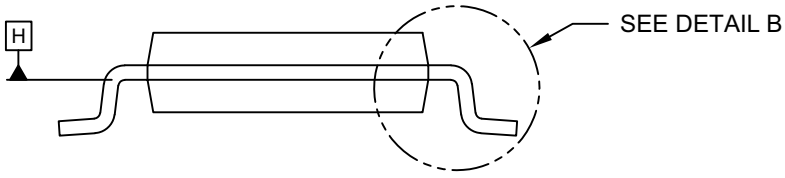
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

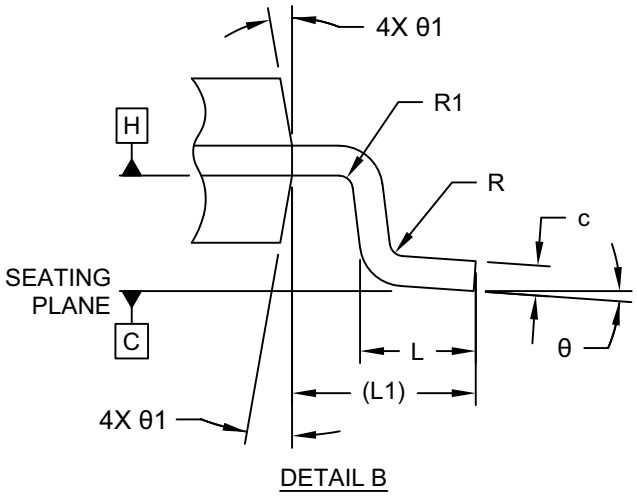


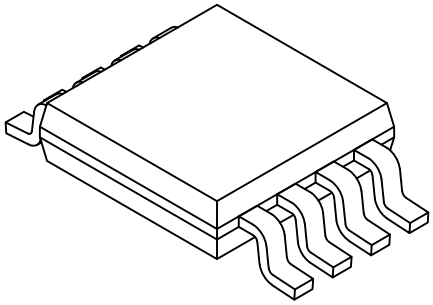
VIEW A–A

Microchip Technology Drawing C04-111-MS Rev F Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.10
Standoff	A1	0.00	–	0.15
Molded Package Thickness	A2	0.75	0.85	0.95
Overall Length	D		3.00 BSC	
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Terminal Width	b	0.22	–	0.40
Terminal Thickness	c	0.08	–	0.23
Terminal Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°

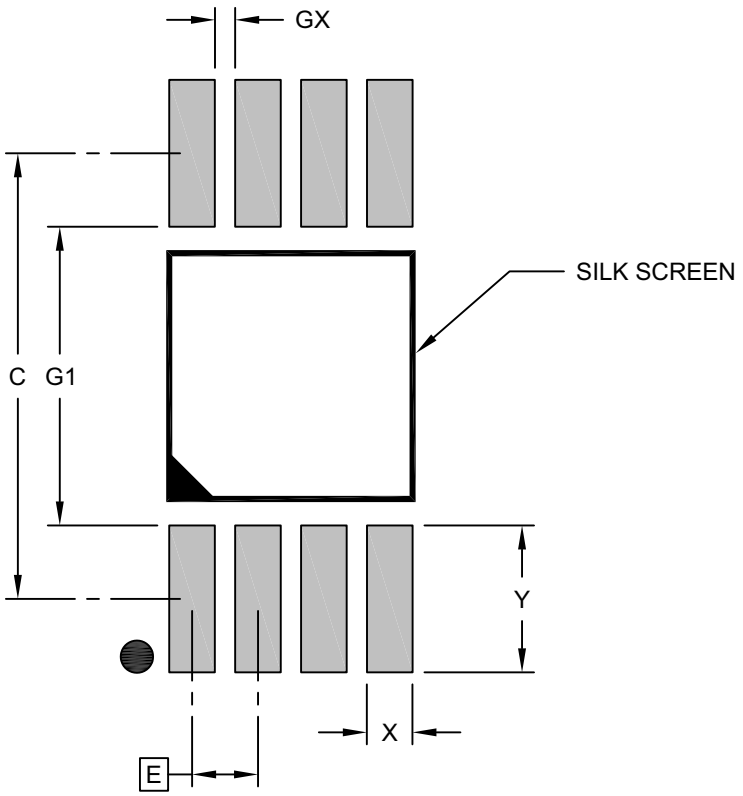
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111-MS Rev F Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Contact Pad Width (X8)	X			0.45
Contact Pad Length (X8)	Y			1.45
Contact Pad to Contact Pad (X4)	G1	2.95		
Contact Pad to Contact Pad (X6)	GX	0.20		

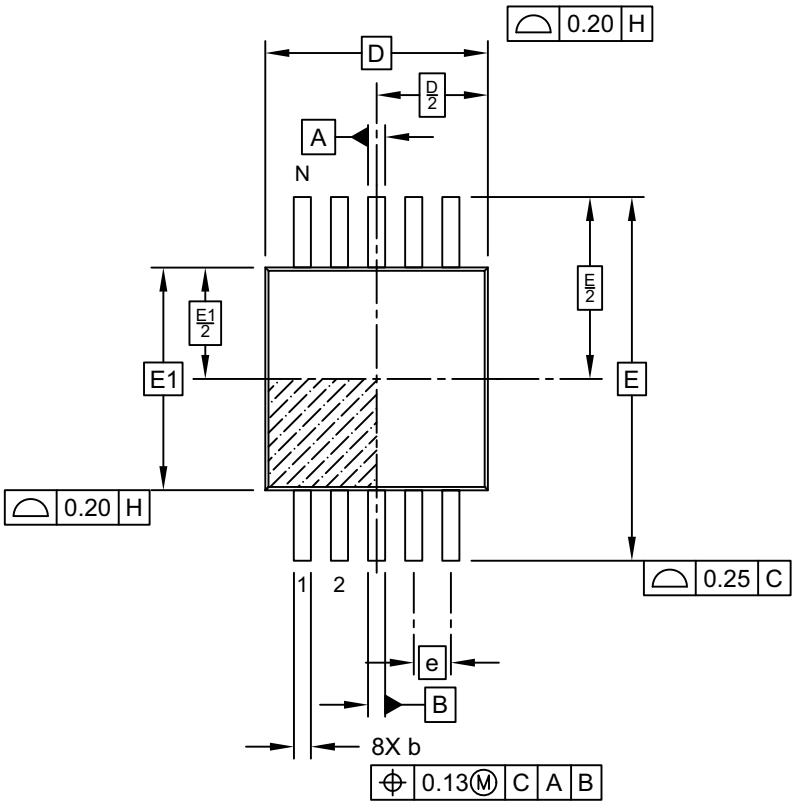
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

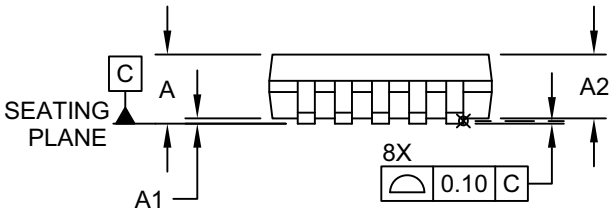
Microchip Technology Drawing C04-2111-MS Rev F

10-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

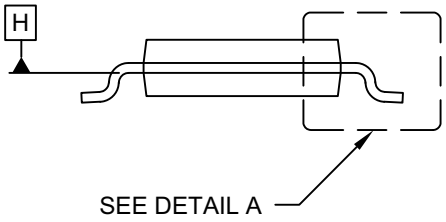
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

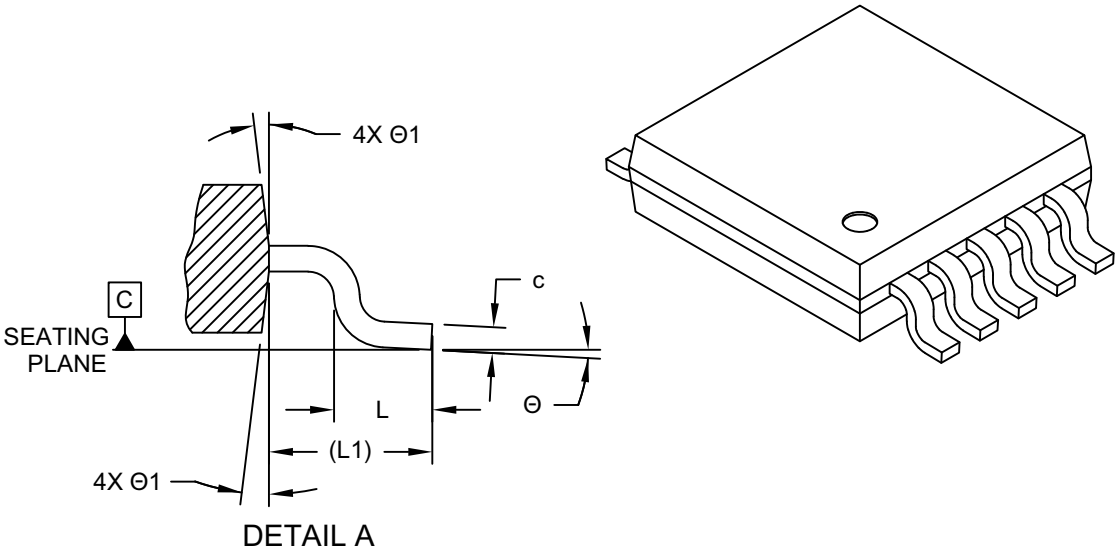


END VIEW

Microchip Technology Drawing C04-021-MS Rev F Sheet 1 of 2

10-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	Θ	0°	-	8°
Mold Draft Angle	Θ1	5°	-	15°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.15	-	0.33

Notes:

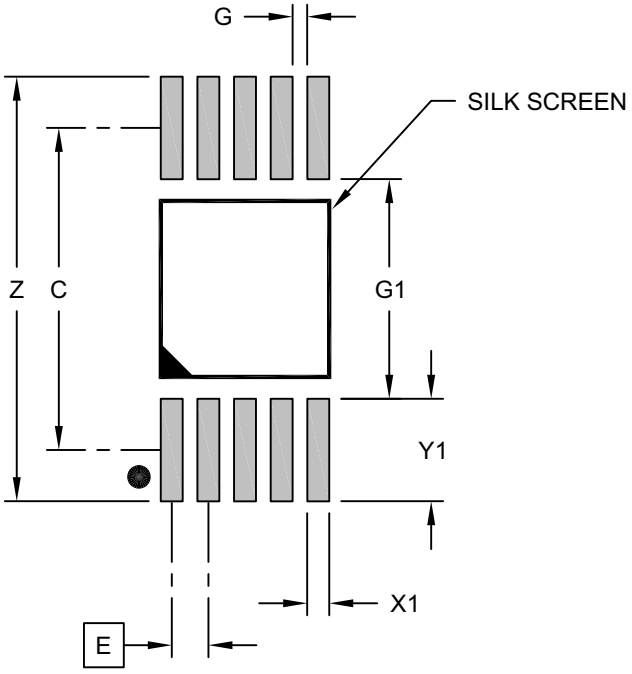
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-021-MS Rev F Sheet 2 of 2

10-Lead Plastic Micro Small Outline Package (MS) - 3x3 mm Body [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.80
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			1.40
Distance Between Pads (X5)	G1	3.00		
Distance Between Pads (X8)	G	0.20		

Notes:

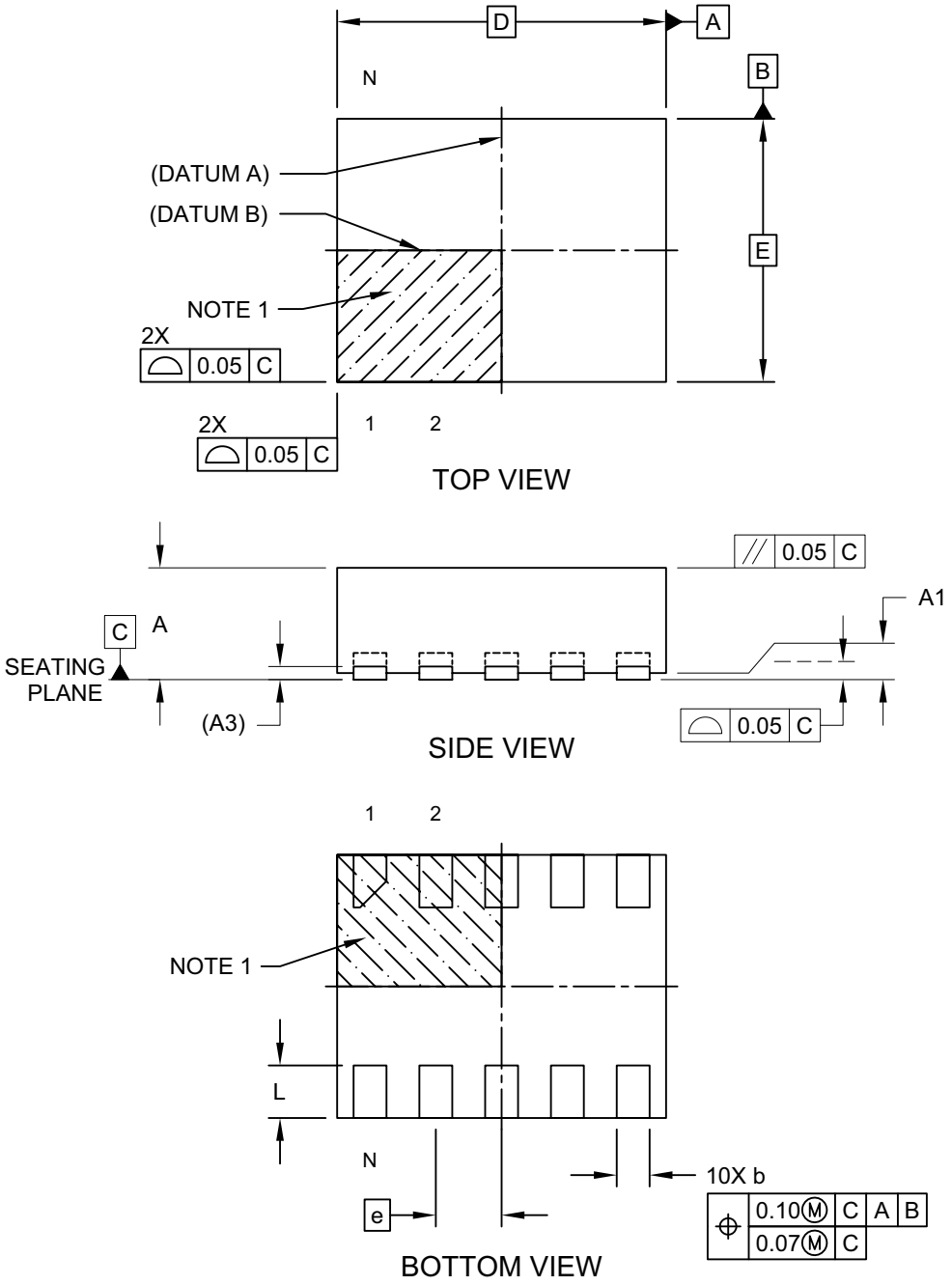
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021-MS Rev F

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

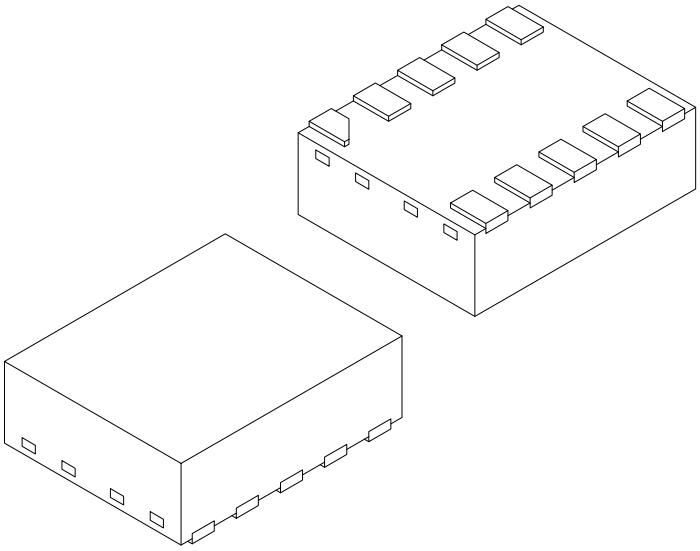
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-332B Sheet 1 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	(A3)		0.10 REF	
Overall Length	D		2.50 BSC	
Overall Width	E		2.00 BSC	
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

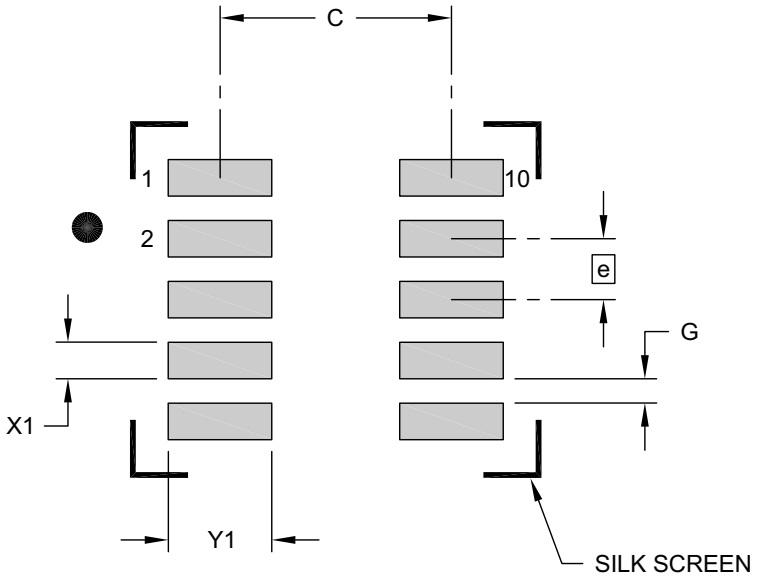
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-332B Sheet 2 of 2

10-Lead Very Thin Plastic Dual Flat, No Lead Package (9R) - 2.5x2.0 mm Body [VDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C		1.90	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.85
Contact Pad to Center Pad (X10)	G1	0.20		

Notes:

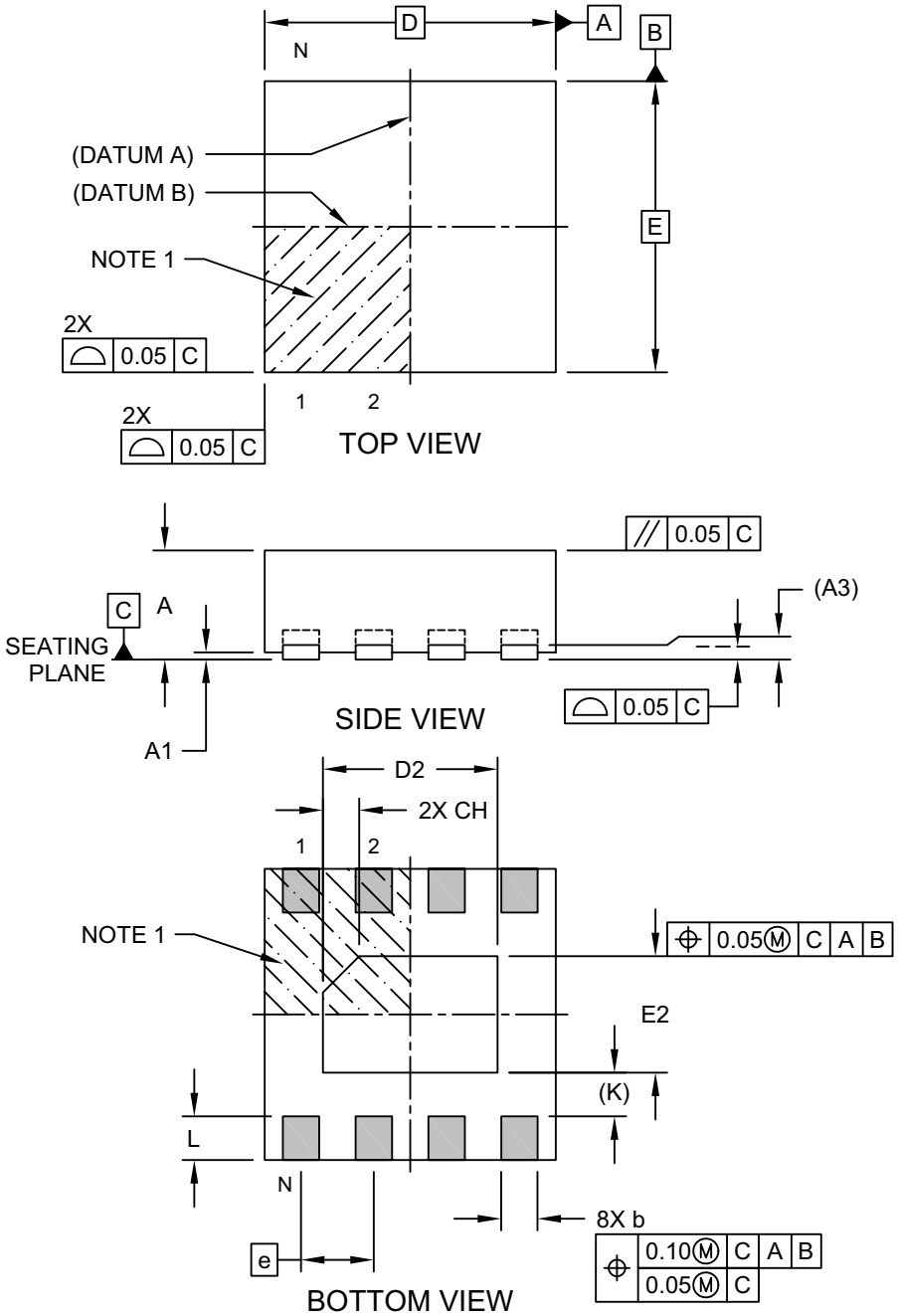
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2332A

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

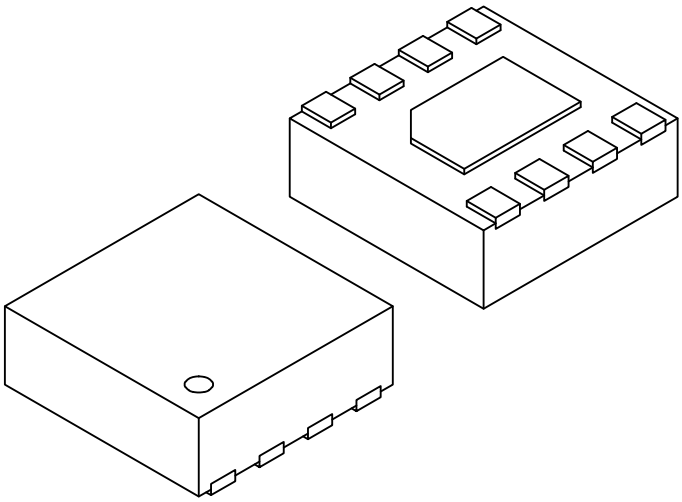
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-261C Sheet 1 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.10 REF	
Overall Width	E		2.00 BSC	
Exposed Pad Width	E2	0.70	0.80	0.90
Overall Length	D		2.00 BSC	
Exposed Pad Length	D2	1.10	1.20	1.30
Exposed Pad Chamfer	CH	-	0.25	-
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.25	0.30	0.35
Terminal-to-Exposed-Pad	K		0.30 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

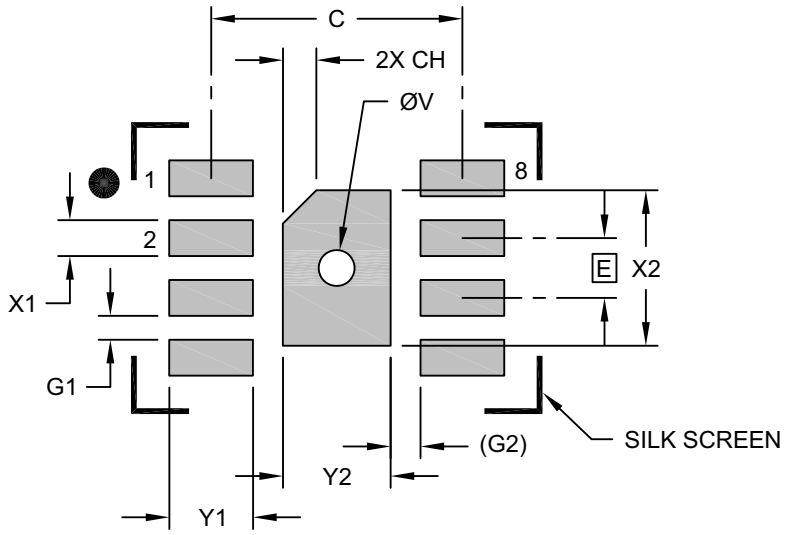
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-261C Sheet 2 of 2

8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (RW) - 2x2 mm Body [WDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	Y2			0.90
Optional Center Pad Length	X2			1.30
Contact Pad Spacing	C		2.10	
Center Pad Chamfer	CH		0.28	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.70
Contact Pad to Contact Pad (X6)	G1	0.20		
Contact Pad to Center Pad (X8)	G2		0.25 REF	
Thermal Via Diameter	V		0.30	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2261C

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	[X](1)	-X	X	/XX
Device	Number of Channels	Hardware Shutdown	Tape and Reel Option	Address Option	Temperature Range	Package

Device:	**MCP998X**:	Remote Diode Temperature Sensor
Number of Channels:	2, 3, 4,5 =	Number of Channels
	33 =	3-Channel 8-LD Option
Hardware Shutdown Option:	D =	Hardware Shutdown (**MCP998XD**)
	Blank =	No Hardware Shutdown Option (**MCP998X**)
Tape and Reel:	T =	Tape and Reel(1)
	Blank =	Tube
Address Option:	1, 2 =	Fixed Address Options
	A =	Addressable Option (**MCP998X** only)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	A3 =	8-Lead Plastic Micro Small Outline
	E3 =	10-Lead Plastic Micro Small Outline
	RW =	=8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (WDFN)
	9R =	10-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (VDFN)

Examples:

a) MCP9982T-1E/A3: 8-Lead MSOP, Two-Channel, Tape and Reel, 1001_100 (R/W)

b) MCP9985T-AE/9R: 10-Lead VDFN, Five-Channel, Tape and Reel, Addressable

c))MCP9985DT-2E/E3: 10-Lead MSOP, Five-Channel with Hardware Shutdown, Tape and Reel, 1001_101 (R/W)

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	[X](1)	-X	X	/XX	VAO
Device	Number of Channels	Hardware Shutdown	Tape and Reel Option	Address Option	Temperature Range	Package	Automotive Qualified

Device:	**MCP998X**:	Remote Diode Temperature Sensor
Number of Channels:	2, 3, 4,5 =	Number of Channels
	33 =	3-Channel 8-LD Option
Hardware Shutdown Option:	D =	Hardware Shutdown (**MCP998XD**)
	Blank =	No Hardware Shutdown Option (**MCP998X**)
Tape and Reel:	T =	Tape and Reel(1)
	Blank =	Tube
Address Option:	1, 2 =	Fixed Address Options
	A =	Addressable Option (**MCP998X** only)
Temperature Range:	E =	-40°C to +125°C (Extended)
Package:	A3 =	8-Lead Plastic Micro Small Outline
	E3 =	10-Lead Plastic Micro Small Outline
	RW =	8-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (WDFN)
	9R =	10-Lead Very, Very Thin Plastic Dual Flat, No Lead Package (VDFN)
Automotive Qualified	VAO =	Tested and qualified in accordance with AEC-Q100

Examples:

a) MCP9982T-AE/A3VAO: 8-Lead MSOP, Two-Channel, Tape and Reel, Addressable, Automotive Qualified

Note 1: The Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variant have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

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ISBN: 978-1-6683-3604-5

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