



80V, 0.8A, Synchronous Buck Converter **Evaluation Board**

DESCRIPTION

The EV4541-N-00A is an evaluation board designed to demonstrate the capabilities of MPS's MP4541, a high-efficiency, synchronous step-down converter with integrated high-side and low-side MOSFETs. The MP4541 provides 0.8A of output current in a buck topology from up to an 80V input power supply.

The MP4541 supports high-efficiency pulseskip mode (PSM) under light-load conditions. Valley current limit circuits protect against overload and short circuit conditions.

The MP4541 is available in an SOIC-8EP package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V _{IN}	8 to 80	V
Output voltage	Vouт	5	V
Output current	Іоит	0 to 0.8	Α

FEATURES

- 8V to 80V Input Voltage
- 1V to 30V Output Voltage
- 90% Maximum Operation Duty Cycle
- $625m\Omega/380m\Omega$ Internal MSOFETs
- Constant-On-Time Control Mode
- Configurable 100kHz to 1MHz Frequency
- Internal Soft Start and Loop Compensation
- Over-Current Protection (OCP) and Short-Circuit Protection (SCP) with Hiccup Mode
- High-Efficiency PSM at Light-Load
- Available in an SOIC-8EP Package

APPLICATIONS

- **High-Voltage Battery Packs**
- **Industrial Power Supplies**
- **Printer Power Boards**

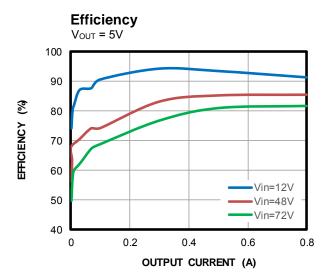
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EVALUATION BOARD



(LxWxH) 6.35cmx6.35cmx0.6cm

Board Number	MPS IC Number	
EV4541-N-00A	MP4541GN	





QUICK START GUIDE

The output voltage of this board is set to 5V. The board layout accommodates most commonly used components. Follow the steps below to quick start the EV4541-N-00A:

- 1. Preset the power supply (V_{IN}) between 8V and 80V.
- 2. Turn the power supply off.
- 3. Connect the power supply terminals to:
 - a. Positive (+): VIN
 - b. Negative (-): GND
- 4. Connect the load to:
 - a. Positive (+): VOUT
 - b. Negative (-): GND
- 5. Turn the power supply on after making the connections.
- 6. The MP4541 is enabled on the evaluation board once V_{IN} is applied.
- 7. The output voltage (V_{OUT}) can be adjusted by changing R1 and R2. Calculate V_{OUT} with Equation (1):

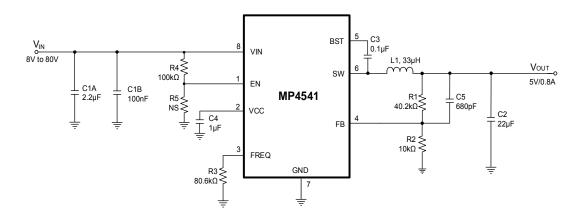
$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \tag{1}$$

Where $V_{FB} = 1V$.

8. To use the enable function, apply a digital input to the EN pin. Drive EN above 1.35V to turn on the EV4541-N-00A; drive it below 0.4V to turn the device off.



EVALUATION BOARD SCHEMATIC





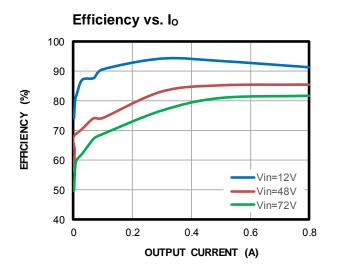
BILL OF MATERIALS

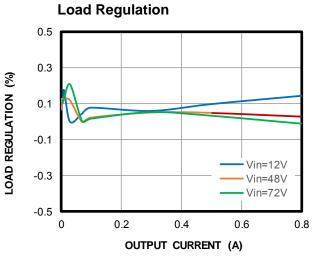
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
1	C1A	2.2µF	Ceramic capacitor, 100V, X7R	1210	muRata	GRM32ER72A225KA35L
1	C1B	100nF	Ceramic capacitor, 100V, X7R	0603	muRata	GRM188R72A104KA35D
1	C2	22µF	Ceramic capacitor, 16V, X7S	1206	muRata	GRM31CC71C226ME11L
1	C3	100nF	Ceramic capacitor, 16V, X7R	0402	muRata	GRM155R71C104KA88D
1	C4	1µF	Ceramic capacitor, 10V, X7S	0402	muRata	GRM155C71A105KE11D
1	C5	680pF	Ceramic capacitor, 16V, X7R	0402	WE	885012205024
1	R1	40.2kΩ	Film resistor, 1%	0603	YAGEO	RC0603FR-0740K2L
1	R2	10kΩ	Film resistor, 1%	0603	YAGEO	RC0603FR-0710KL
1	R3	80.6kΩ	Film resistor, 1%	0603	YAGEO	RC0603FR-0780K6L
1	R4	100kΩ	Film resistor, 1%	0603	YAGEO	RC0603FR-07100KL
0	R5	NS				
1	L1	33µH	I _{SAT} = 1.4A, 140mΩ inductor	SMD	WE	7447779133
1	U1	MP4541	80V, 0.8A, synchronous buck	SOIC-8EP	MPS	MP4541GN

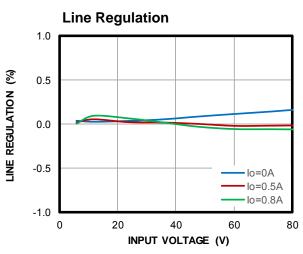


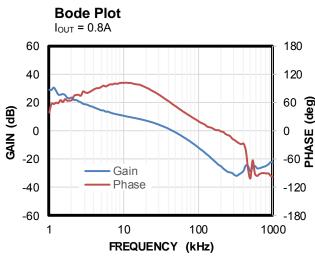
EVB TEST RESULTS

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 48V$, $V_{OUT} = 5V$, $L = 33\mu H$, $T_A = 25^{\circ}C$, unless otherwise noted.

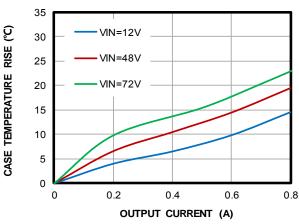








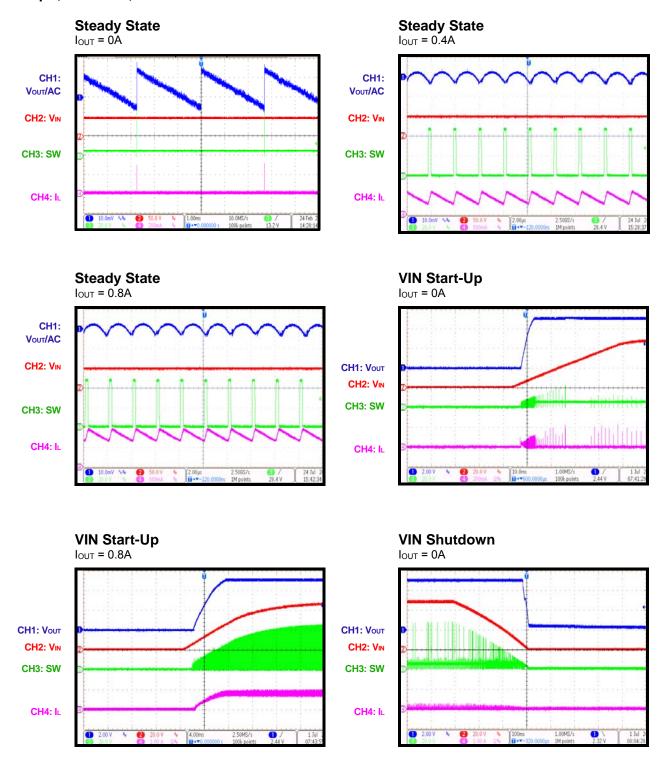
Case Temperature Rise vs. Output Current





EVB TEST RESULTS (continued)

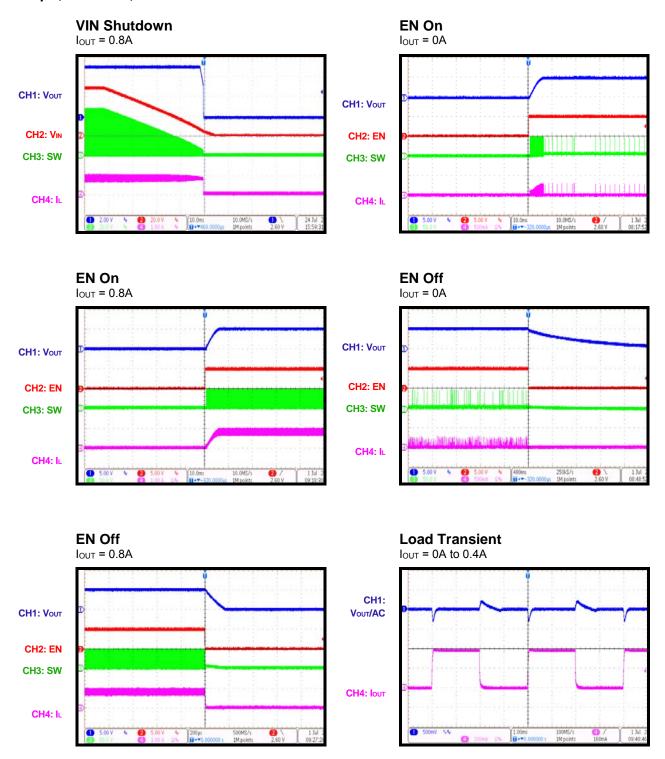
Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 48V$, $V_{OUT} = 5V$, L = 33μ H, $T_A = 25$ °C, unless otherwise noted.





EVB TEST RESULTS (continued)

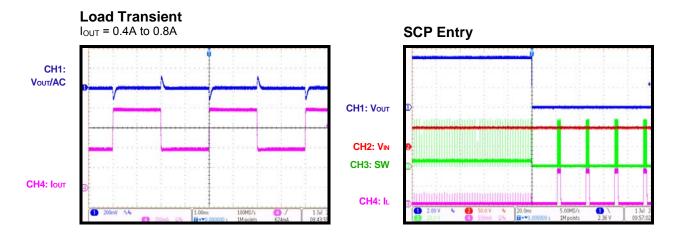
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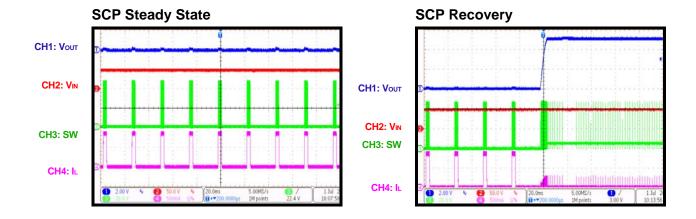




EVB TEST RESULTS (continued)

Performance curves and waveforms are tested on the evaluation board. $V_{IN} = 48V$, $V_{OUT} = 5V$, L = 33μ H, $T_A = 25$ °C, unless otherwise noted.







PCB LAYOUT

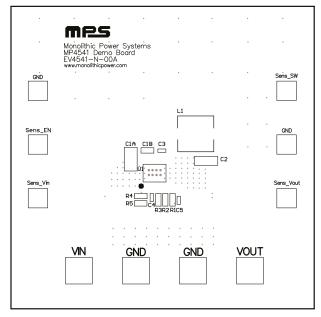


Figure 1: Top Silkscreen Layer

Figure 2: Top Layer

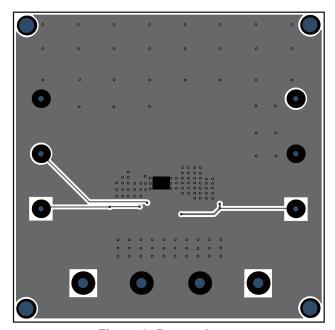


Figure 3: Bottom Layer

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