EV5515-U-00A

18V Power backup and Management Unit for SSD Application Evaluation Board

The Future of Analog IC Technology

DESCRIPTION

EV5515-U-00A Evaluation Board is designed to demonstrate the capabilities of MP5515. MP5515 is an input power conditioning PMIC targeting enterprise solid-state drive applications.

MP5515 consists of input current limiting, input reverse current blocking, and a MPS patented high efficiency bi-directional boost/buck converter with only one inductor for energy storage and system backup power at power fail. It also provides I2C interface, accurate input current sensing, ADC, and backup capacitor health test.

MP5515 is available in QFN30-5x5mm package.

ELECTRICAL SPECIFICATION

Parameter	Symbol	Value	Units
Input Voltage	V_{IN}	12	V
Storage Voltage	V_{STRG}	28	V
Input Pfail Threshold	V_{PFI}	8	V
Bus Backup Voltage	V_{RLS}	7.5	V
Bus Backup Max Load	$I_{RELEASE}$	5	A

FEATURES

- Wide 2.7V to 18V Operating Input Range
- Programmable up to 32V Storage Voltage
- Up to 6A Programmable Input Current Limit
- 5A Buck Load Capability
- Adjustable Slew Rate for VB Voltage Rising
- Input Current Limiter with Integrated 14mΩ MOSFET
- Input Over Voltage Protection
- Reverse Current Protection
- Input Failure Indicator
- Backup Capacitor Health Test
- Comprehensive Voltage, Current, Temperature Sensor ADC Conversion
- Thermal Protection
- Available in a QFN30 (5mm×5mm) Package

APPLICATIONS

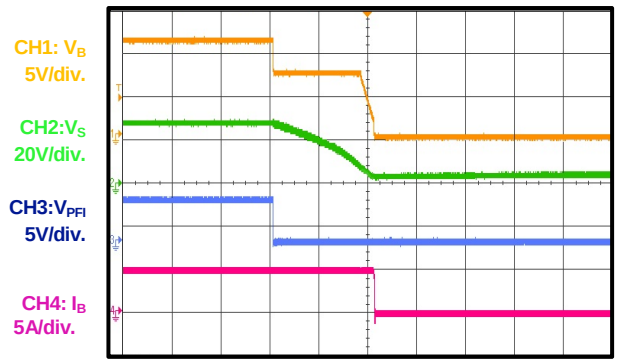
- Solid-State Drives
- Hard-Disk Drives
- Power Back-up Systems

EV5515-U-00A EVALUATION BOARD

(L x W) 6.3cm x 6.3cm

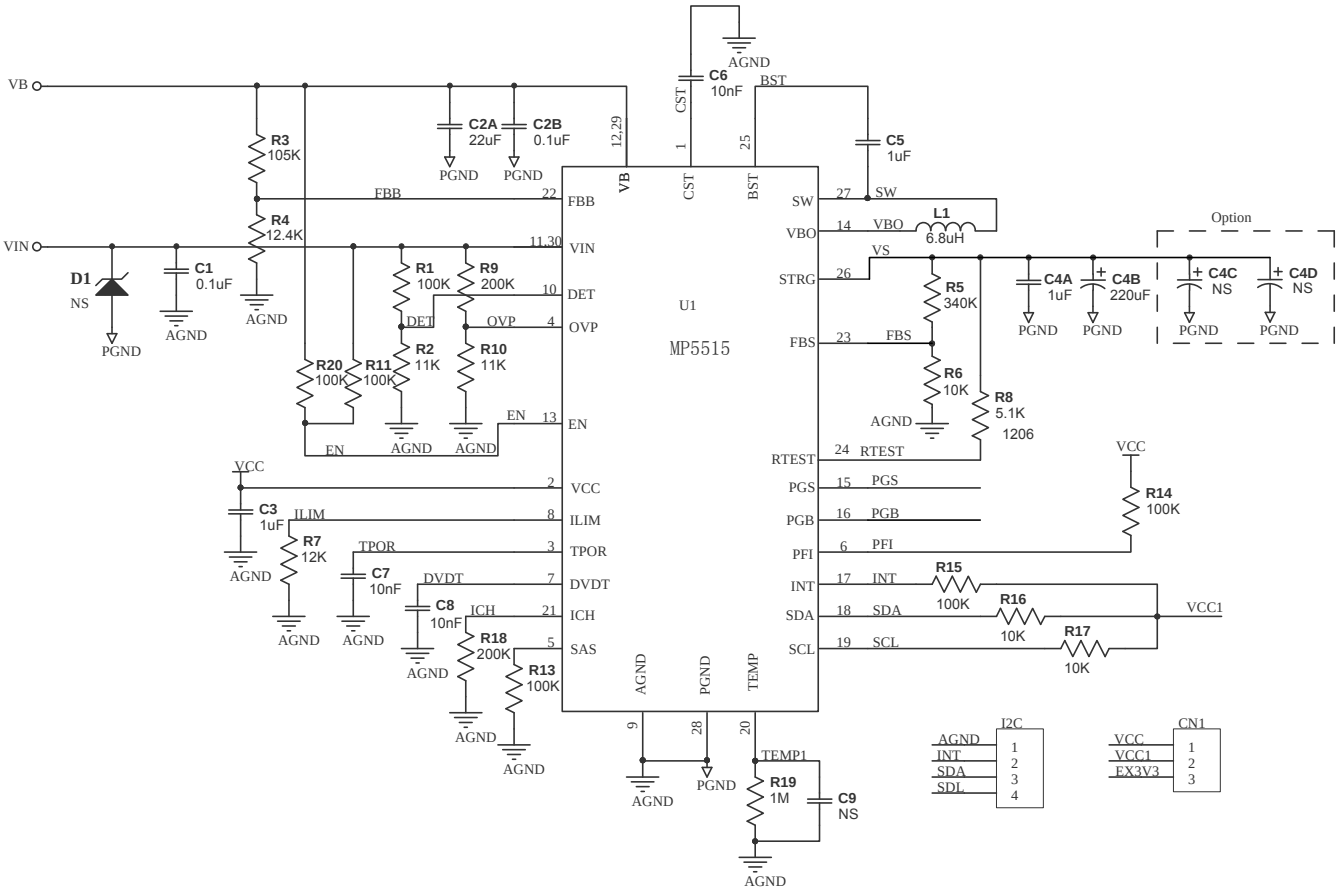
Board Number	MPS IC Number
EV5515-U-00A	MP5515GU

V_{STRG} Release
VB Load=5A



1ms/div.

EVALUATION BOARD SCHEMATIC



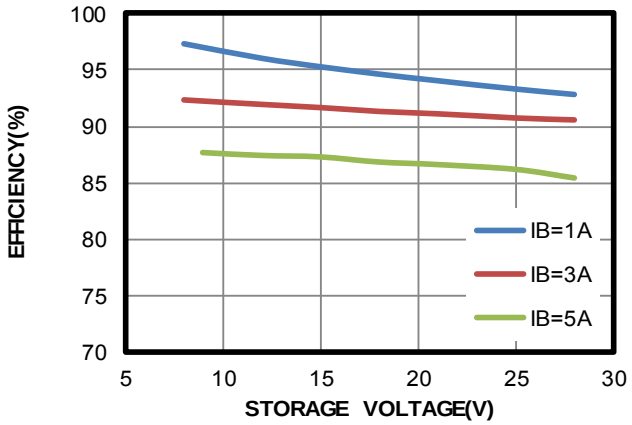
EV5515-U-00A BILL OF MATERIALS

Qty	Ref	Value	Description	Package	Manufacturer	Manufacture P/N
2	C1, C2B	100nF	Ceramic Cap.,50V,X7R	0603	Murata	GRM155R71H104ME14D
1	C2A	22μF	Ceramic Cap.,25V,X5R	1210	Murata	GRM32ER61E226KE15L
2	C3, C5	1μF	Ceramic Cap.,25V,X7R	0402	TDK	C1005X7R1E105KT00E
1	C4A	1μF	Ceramic Cap.,50V,X7R	1210	Murata	GRM32RR71H105KA01L
1	C4B	220μF	220μF/35V	DIP	WE	8.60081E+11
0	C4C, C4D, C9	NS				
3	C6, C7, C8	10nF	Ceramic Cap.,50V,X7R	0402	WE	8.85012E+11
1	L1	6.8μH	Inductor 6.8μH, DCR=54mΩ, Isat=8A		WE	74437346068
6	R1, R11, R20, R13, R14, R15,	100K	Film Res,1%,0402,100K	0402	UniOhm	RF0402-100K-HS
2	R2, R10	11K	Film Res,1%,0402,11K	0402	YAGEO	RC0402FR-0711KL
1	R3	105K	Film Res,1%,0402,105K	0402	YAGEO	RC0402FR-07105KL
1	R4	12.4K	Film Res,1%,0402,12.4K	0402	YAGEO	RC0402FR-0712K4L
1	R5	340K	Film Res,1%,0402,340K	0402	YAGEO	RC0402FR-07340KL
3	R6, R16, R17	10K	Film Res,1%,0402,10K	0402	YAGEO	RC0402FR-0710KL
1	R7	12K	Film Res,1%,0402,12K	0402	YAGEO	RC0402FR-0712KL
1	R8	5K1	Film Res,5%,1206,5K1	1206	N/A	4090F0F
2	R9, R18	200K	Film Res,1%,0402,200K	0402	YAGEO	RC0402FR-07200KL
1	R19	1M	Film Res,1%,0402,1M	0402	YAGEO	RC0402JR-071ML
1	MP5515	MP5515	ENERGY BACKUP AND MANAGEMENT UNIT	QFN30	MPS	MP5515GU

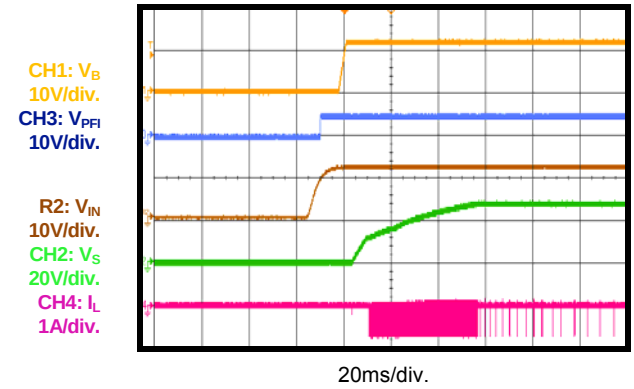
EVB TEST RESULTS

Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{STRG} = 28V, V_{PFI} = 8V, V_{RLS} = 7.5V, L = 6.8μH, T_A = 25ºC, $I_{RELEASE}$=5A, unless otherwise noted.

Backup-Release Efficiency

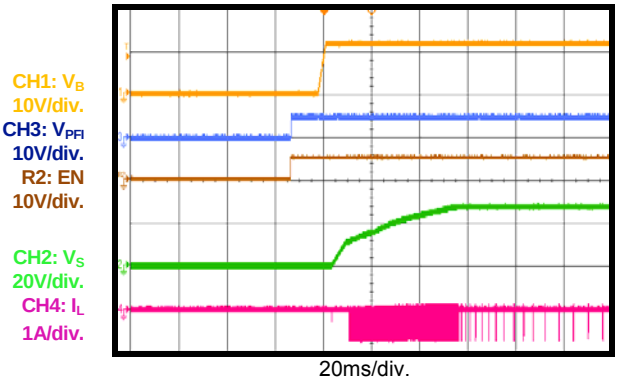


VIN Power On



20ms/div.

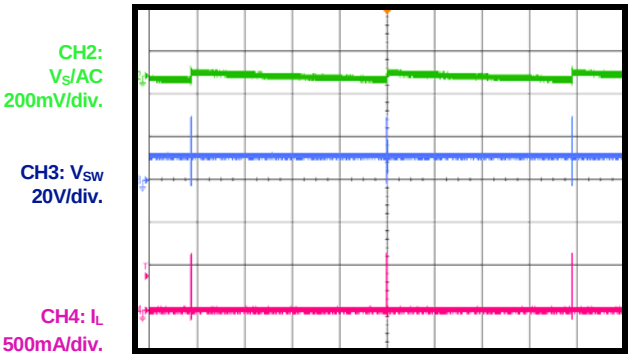
EN Turn On



20ms/div.

Boost Steady State

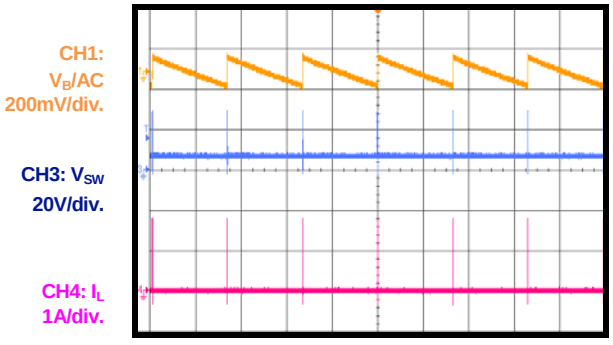
R_{ICH}=200kΩ



10ms/div.

BUCK Steady State

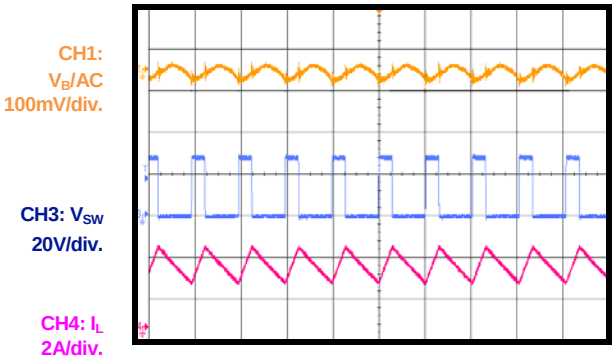
V_B, Load=0A



500μs/div.

BUCK Steady State

V_B, Load=3A

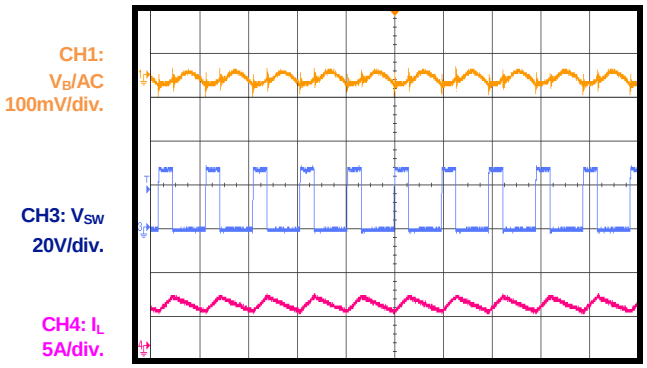


2μs/div.

EVB TEST RESULTS *(continued)*

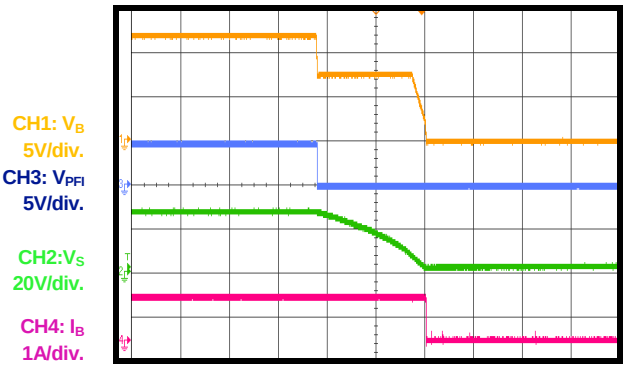
Performance waveforms are tested on the evaluation board.
V_{IN} = 12V, V_{STRG} = 28V, V_{PFI} = 8V, V_{RLS} = 7.5V, L = 6.8µH, T_A = 25ºC, $I_{RELEASE}$=5A, unless otherwise noted.

BUCK Steady State
V_B, Load=5A



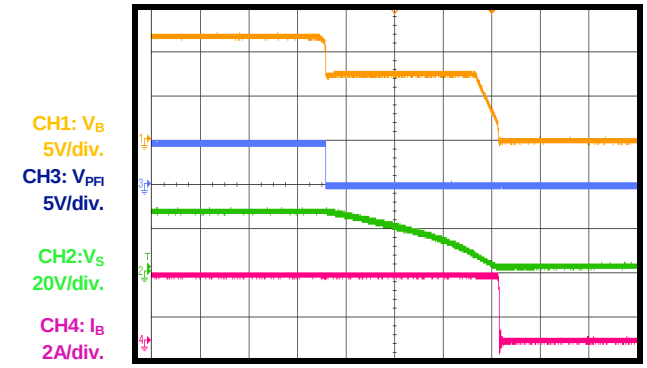
2µs/div.

V_{STRG} Release
VB Load=1A



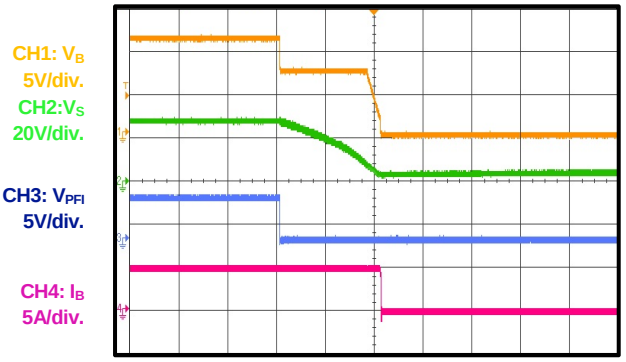
5ms/div.

V_{STRG} Release
VB Load=3A



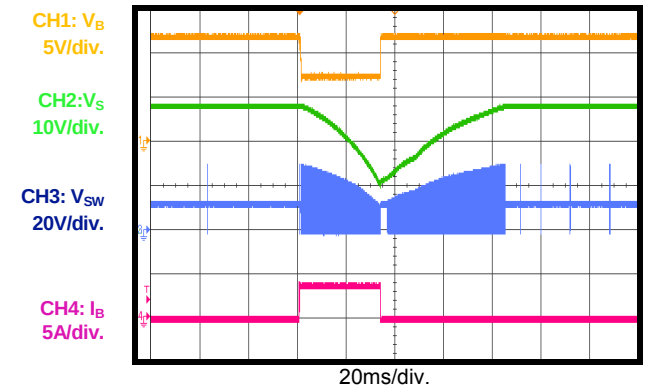
1ms/div.

V_{STRG} Release
VB Load=5A



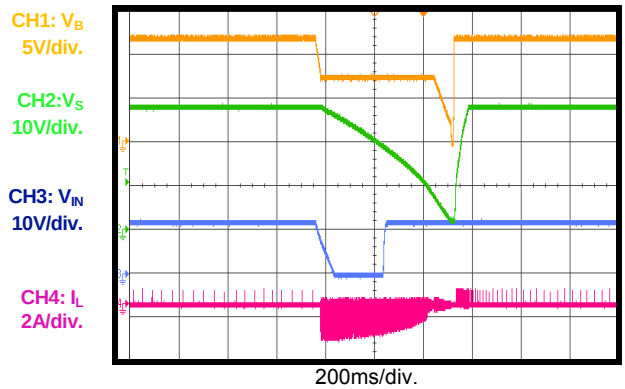
1ms/div.

Input-Current Limit Recover
VB Load=4A, R_{LIM}=22kΩ



20ms/div.

VIN OFF, then ON
VB Load=20mA



200ms/div.

PRINTED CIRCUIT BOARD LAYOUT

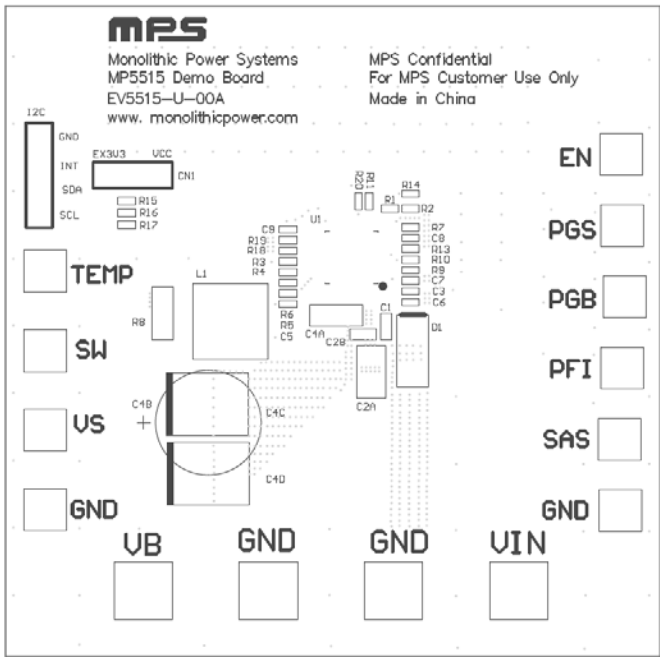


Figure 1—Top Silk Layer

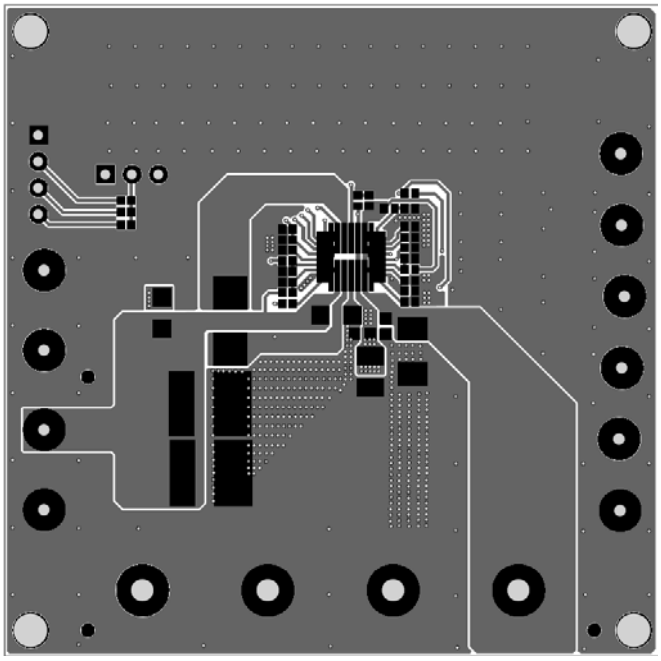


Figure 2—Top Layer

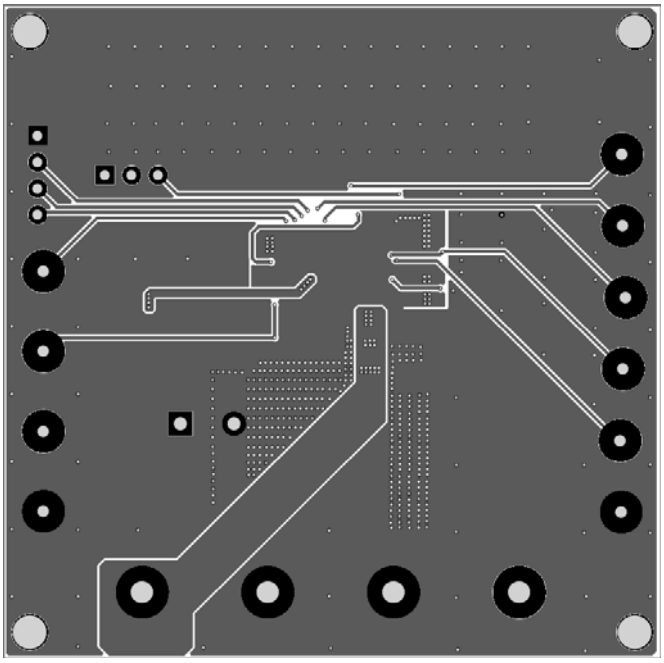


Figure 3—Bottom Layer

QUICK START GUIDE

The board layout accommodates most commonly used components.

1. Connect the positive and negative terminals of the load to VB and GND pins, respectively.

2. Preset power supply to 12V, and then turn off power supply.

3. Connect power supply terminals to: VIN and GND on board.

4. Turn on power supply after making connections, MP5515 will charge the storage capacitor to 28V.

5. Turn off the power supply to observe the power release performance.

6. To use the enable function, apply a digital input to the EN pin. When EN is high, MP5515 is enabled, and when EN is from high to low, MP5515 is forced to buck mode until VSTRG is discharged.

7. Connect pin-2 and pin-3 of CON1 together to set MP5515 I2C signal with VCC voltage, connect pin-1 and pin-2 of CON1 together to set MP5515 I2C signal with external voltage (external voltage source must be connected to pin-3 of CIN1).

8. Use R1 and R2 to set power fail indicate voltage:

$$V_{PFI} = (1 + \frac{R1}{R2}) \times 0.792V$$

And after power fail, bus voltage VB regulation can be set through R3 and R4:

$$VB_{RLS} = (1 + \frac{R_X \times R3}{(R_X + R3) \times R4}) \times V_{FBB-REF}$$

Where, R_X=9MΩ, $V_{FBB-REF}$ is 0.8V typically.

Similarly, R5 and R6 can be chosen for storage voltage setting:

$$V_{STORAGE} = (1 + \frac{R5}{R6}) \times V_{FBS-REF}$$

Where, $V_{FBS-REF}$ is 0.8V typically.