



EVBL4415A-QB-00A

High-Efficiency, 1.5A, 36V, 2.2MHz Synchronous Step-Down Converter Evaluation Board

DESCRIPTION

The EVBL4415A-QB-00A is an evaluation board designed for the MP4415A and MPQ4415A. It features an MPS inductor.

The MP4415A is a synchronous, rectified, step-down switch-mode converter with built-in power MOSFETs. The device offers a very compact solution to achieve 1.5A of continuous output current with excellent load and line regulation across a wide input supply range. The MP4415A uses synchronous mode operation to achieve high efficiency across the output current load range.

The MP4415A is available in a QFN-13 (2.5mmx3mm) package.

ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	V_{IN}	4 to 36	V
Output voltage	V_{OUT}	3.3	V
Output current	I_{OUT}	1.5	A

FEATURES

- Wide 4V to 36V Operating Input Range
- 90mΩ High-Side/50mΩ Low-Side Internal Power MOSFETs
- High-Efficiency Synchronous Mode Operation
- Default 2.2MHz Switching Frequency
- 450kHz to 2.2MHz Frequency Sync
- Forced Continuous Conduction Mode (FCCM)
- High Duty Cycle for Automotive Cold Crank
- Internal Soft Start (SS)
- Power Good (PG) Indicator
- Over-Current Protection (OCP) with Valley Current Detection and Hiccup Mode
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a QFN-13 (2.5mmx3mm) Package

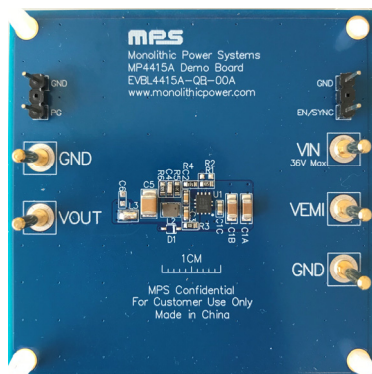
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MPS Inductor MPL-AT2514 Series**

APPLICATIONS

- Automotive
- Industrial Control System
- Distributed Power Systems

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EVBL4415A-QB-00A EVALUATION BOARD

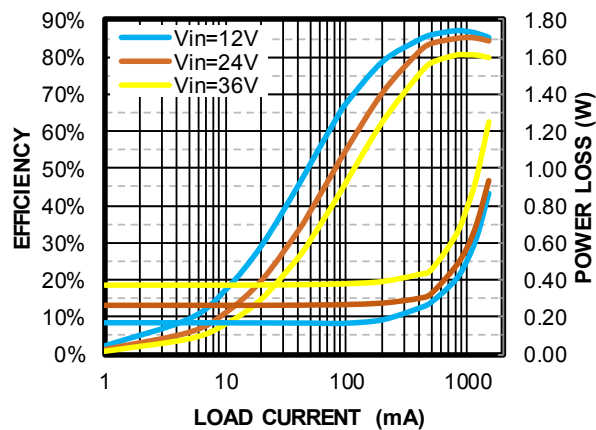


LxWxH (6.35cmx6.35cmx0.5cm)

Board Number	MPS IC Number
EVBL4415A-QB-00A	MP4415AGQB, MPQ4415AGQB

Efficiency vs. Load Current

$V_{OUT} = 3.3V$



QUICK START GUIDE

1. Connect the load terminals to:

- Positive (+): VOUT
- Negative (-): GND

Note that electronic loads represent a negative impedance to the regulator, so a high current can trigger hiccup mode.

2. Preset the power supply output to be between 4 and 36V, then turn it off.

If longer cables (>0.5m total) are used between the source and the EVB, install a damping capacitor at the input terminals, especially when V_{IN} is greater than or equal to 24V.

3. Connect the power supply output terminals to:

- Positive (+): VIN
- Negative (-): GND.

4. Turn the power supply on. The MP4415A should automatically start up.

5. To use the enable function, apply a digital input to the EN/SYNC pin. Drive EN/SYNC above 1.45V to turn the regulator on; drive EN below 1V to turn it off.

6. To use the sync function, apply a 450kHz to 2.2MHz external clock to the EN/SYNC pin to synchronize the internal clock rising edge.

7. The output voltage is set by the external resistor divider. The feedback resistor (R_{FB1}) also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R_{FB1} to be around 40k Ω when $V_{OUT} \geq 1V$. R_{FB2} can then be calculated with Equation (1):

$$R_{FB2} = \frac{R_{FB1}}{\frac{V_{OUT}}{0.807V} - 1} \quad (1)$$

8. The T-type network is highly recommended when V_{OUT} is low (see Figure 1)

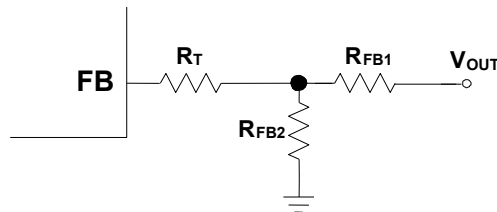


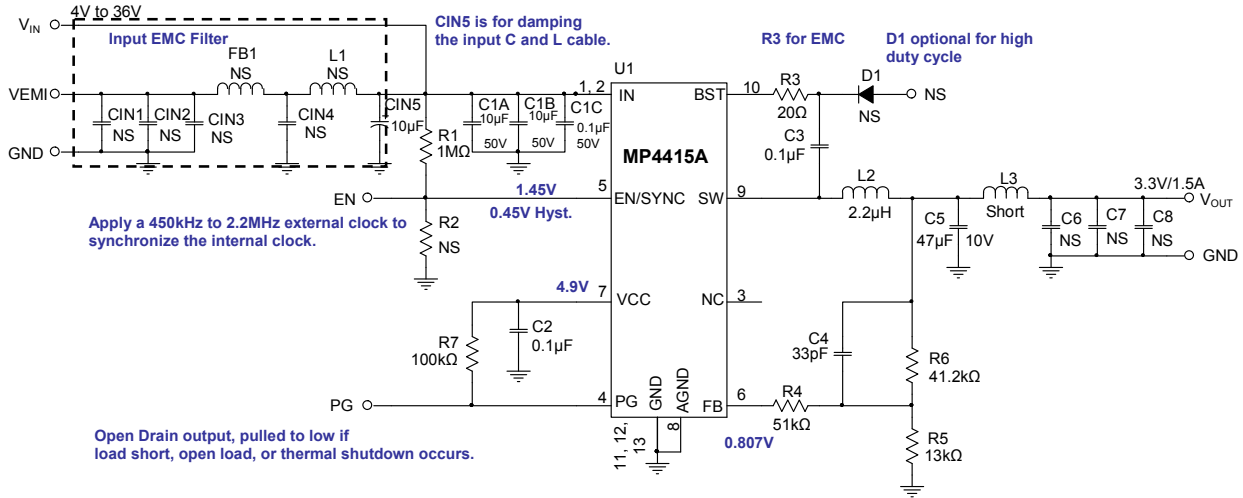
Figure 1: T-Type Network

9. R_T and R_{FB1} are used to set the loop bandwidth. The lower R_T and R_{FB1} is, the higher the bandwidth. However, a high bandwidth may cause an insufficient phase margin, which results in an unstable loop. Select an appropriate value for R_T to make a tradeoff between the bandwidth and phase margin. Table 1 lists the recommended feedback resistor and R_T values for common output voltages.

Table 1: Recommended Feedback Resistors and Output Voltages

V _{OUT} (V)	R _{FB1} (k Ω)	R _{FB2} (k Ω)	R _T (k Ω)
3.3	41.2 (1%)	13 (1%)	51 (1%)
5	41.2 (1%)	7.68 (1%)	51 (1%)

EVALUATION BOARD SCHEMATIC

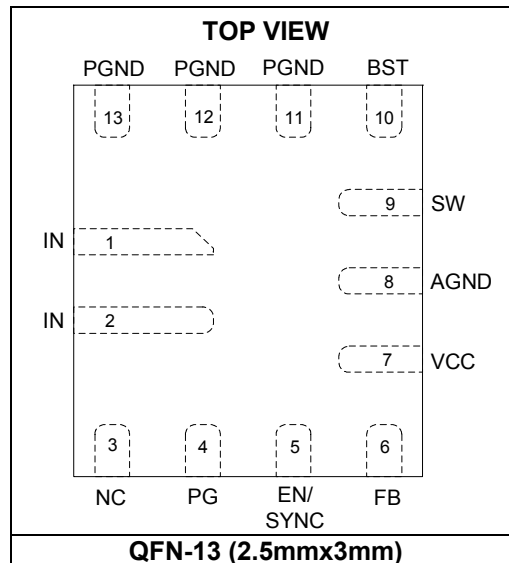


Reference for FB divider selection

V_{OUT} (V)	$R6$ (k Ω)	$R5$ (k Ω)
5	41.2(1%)	7.68(1%)
2.5	41.2(1%)	19.6(1%)
1.8	41.2(1%)	33.5(1%)

Figure 2: Evaluation Board Schematic

PACKAGE REFERENCE



EVBL4415A-QB-00A BILL OF MATERIALS

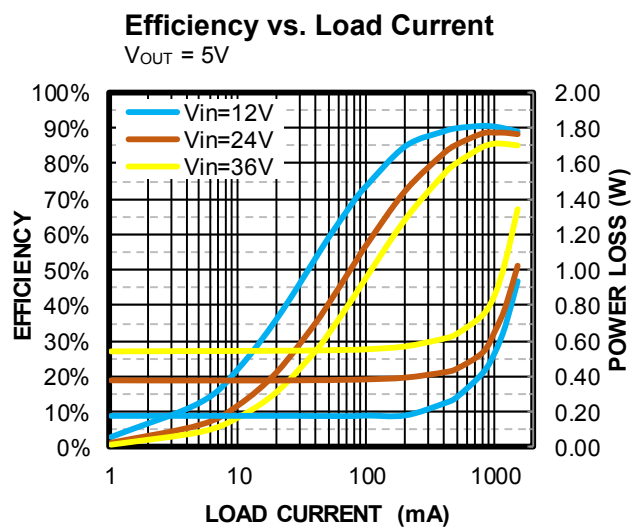
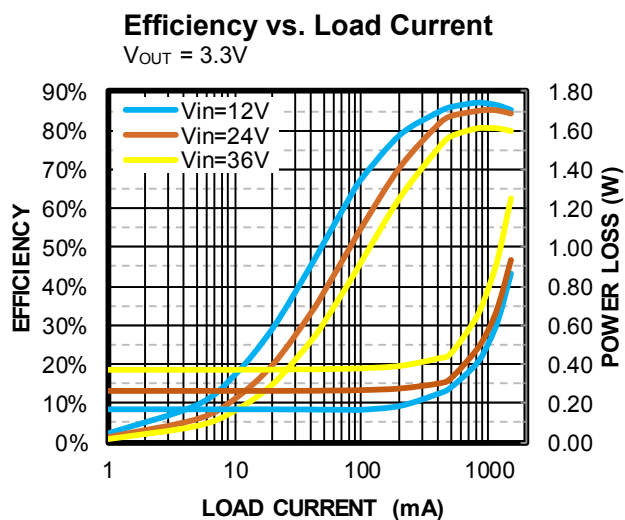
Qty	Designator	Value	Description	Package	Manufacture	Manufacturer PN
5	CIN1, CIN2, CIN3, CIN4, CIN5	NS				
2	C1A, C1B	10 μ F	Ceramic capacitor, 50V, X5R	1206	Murata	GRM31CR61H106KA12L
1	C1C	0.1 μ F	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
2	C2, C3	0.1 μ F	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C4	33pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H330JA01D
1	C5	47 μ F	Ceramic capacitor, 10V, X5R	1210	Murata	GRM32ER61A476KE20L
3	C6, C7, C8	NS				
1	D1	NS				
1	FB1	NS				
1	L1	NS				
1	L2	2.2 μ H	Inductor, 70m Ω DCR, 2.5A	SMD	MPS	MPL-AT2514-2R2
1	L3	NS				
1	R1	1M Ω	Film resistor, 5%	0603	Yageo	RC0603JR-071ML
1	R3	20 Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0720RL
1	R4	51k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0751KL
1	R5	13k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0713KL
1	R6	41.2k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-0741K2L
1	R7	100k Ω	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R2	NS				
1	U1	MP4415A	Step-down converter	QFN-13 (2mmx 3mm)	MPS	MP4415AGQB
5	VIN, VEMI, GND, GND, VOUT	2.0	2.0 golden pin	DIP	MPS ⁽¹⁾	
4	PG, GND, EN/SYNC, GND	2.54mm	2.54mm test pin	DIP	Any	

Note:

1) Contact an MPS FAE for more information regarding these pins.

EVB TEST RESULTS

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $f_{SW} = 2.2MHz$, $T_A = 25^\circ C$, unless otherwise noted.

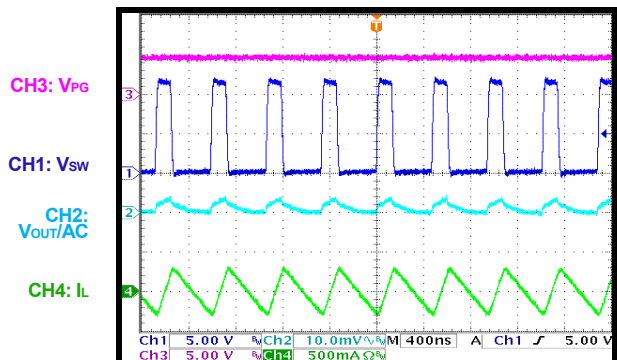


EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $f_{SW} = 2.2MHz$, $T_A = 25^\circ C$, unless otherwise noted.

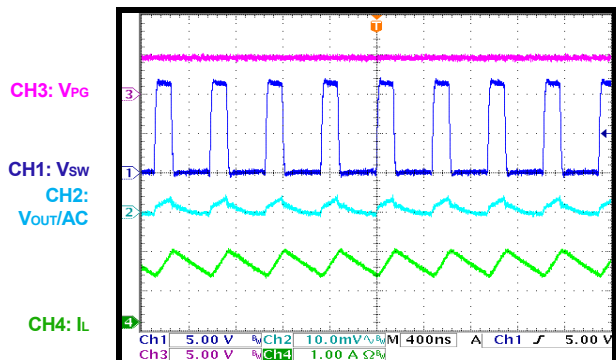
Steady State

$I_{OUT} = 0A$



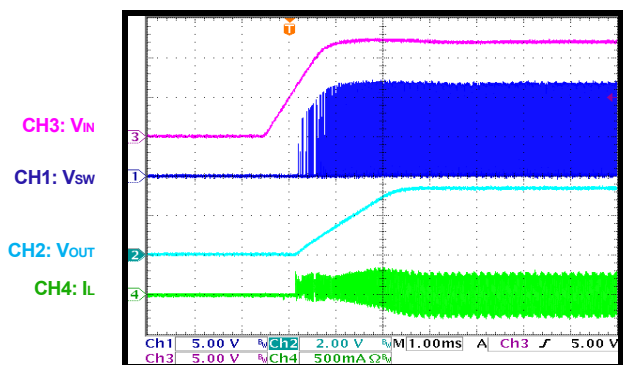
Steady State

$I_{OUT} = 1.5A$



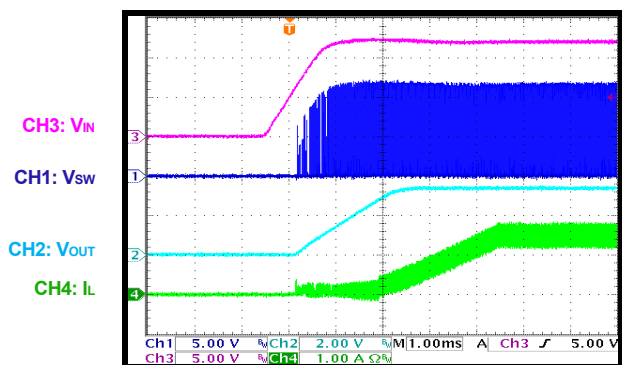
Start-Up

$I_{OUT} = 0A$



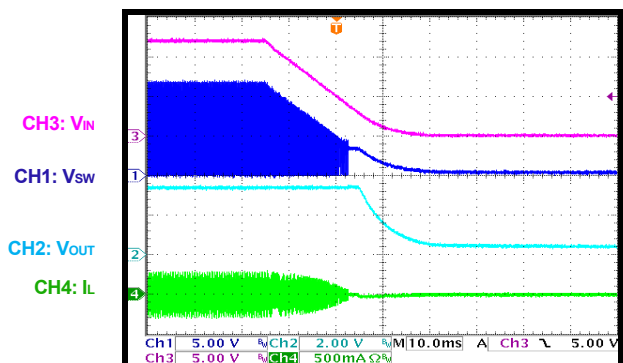
Start-Up

$I_{OUT} = 1.5A$



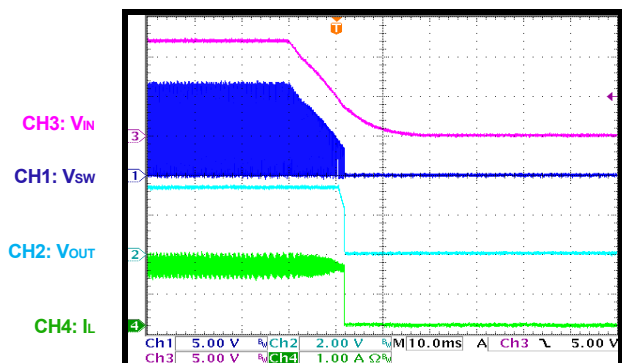
Shutdown

$I_{OUT} = 0A$



Shutdown

$I_{OUT} = 1.5A$

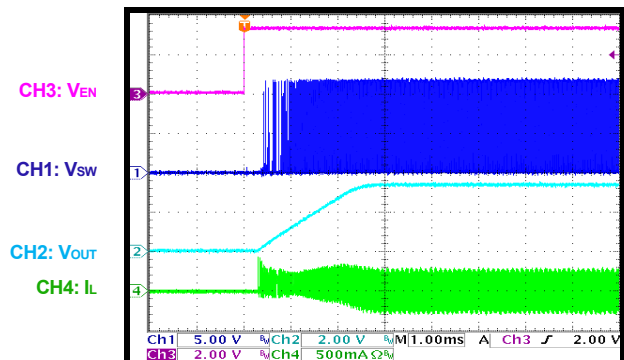


EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $f_{SW} = 2.2MHz$, $T_A = 25^\circ C$, unless otherwise noted.

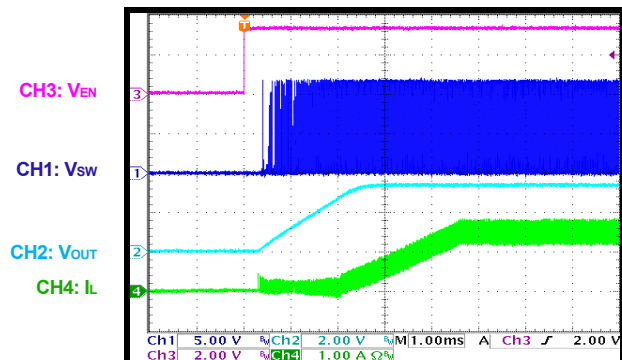
EN On

$I_{OUT} = 0A$



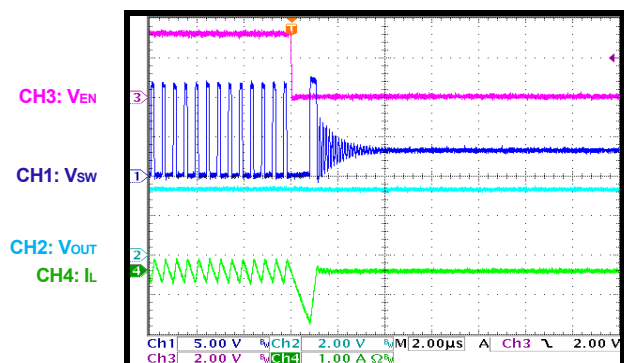
EN On

$I_{OUT} = 1.5A$



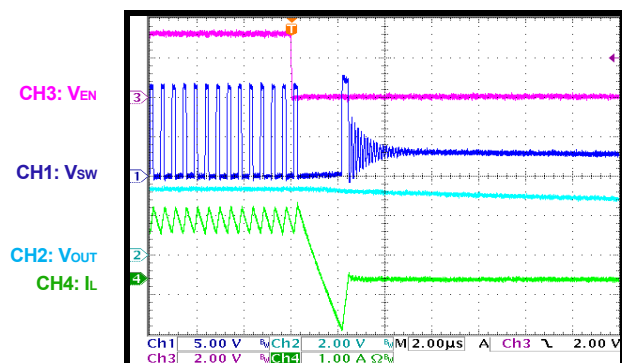
EN Off

$I_{OUT} = 0A$



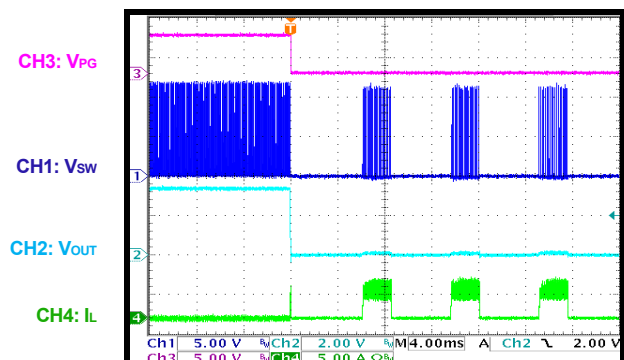
EN Off

$I_{OUT} = 1.5A$



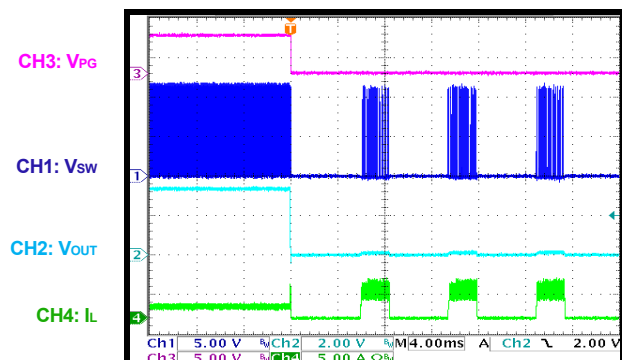
SCP Entry

$I_{OUT} = 0A$



SCP Entry

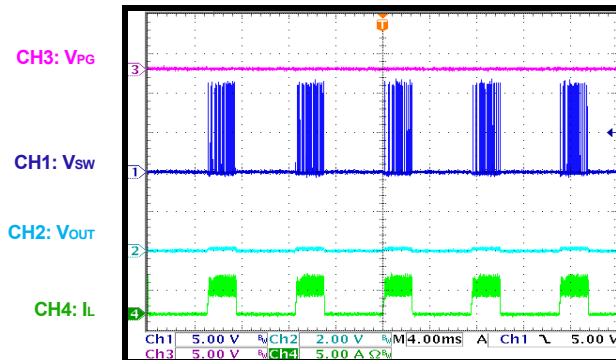
$I_{OUT} = 1.5A$



EVB TEST RESULTS *(continued)*

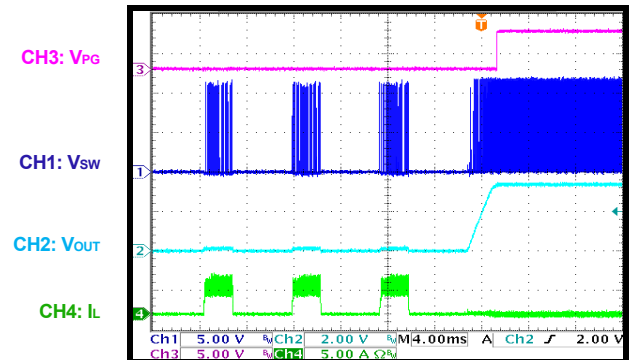
$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $f_{SW} = 2.2MHz$, $T_A = 25^\circ C$, unless otherwise noted.

SCP Steady State



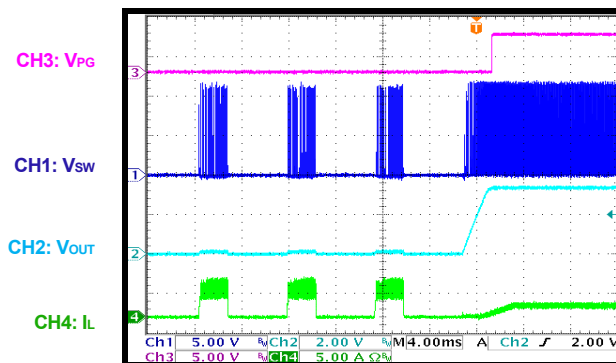
SCP Recovery

$I_{OUT} = 0A$



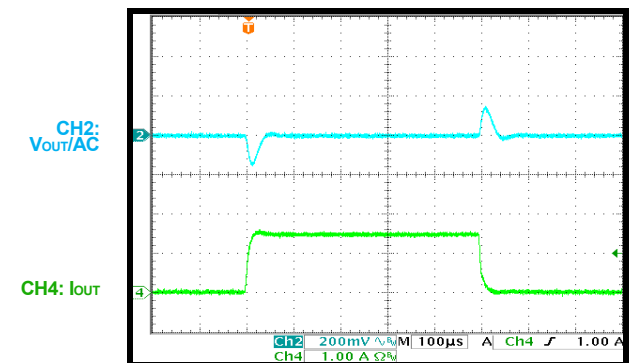
SCP Recovery

$I_{OUT} = 1.5A$



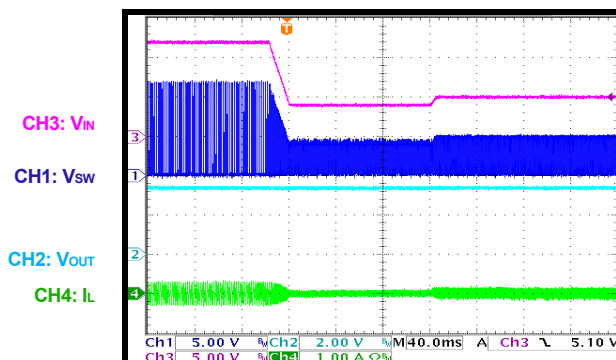
Load Transient

$I_{OUT} = 0A$ to $1.5A$



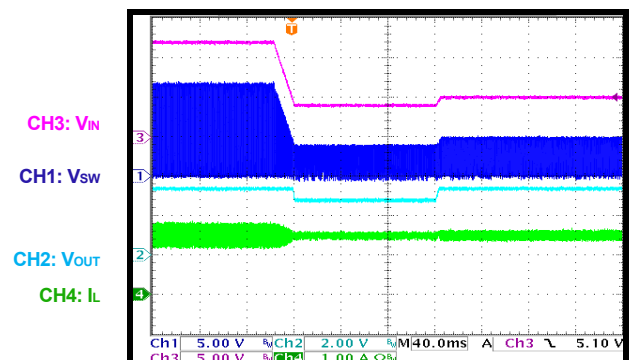
Cold Crank

$V_{IN} = 12V$ to $4V$ to $5V$, $I_{OUT} = 0A$



Cold Crank

$V_{IN} = 12V$ to $4V$ to $5V$, $I_{OUT} = 1.5A$

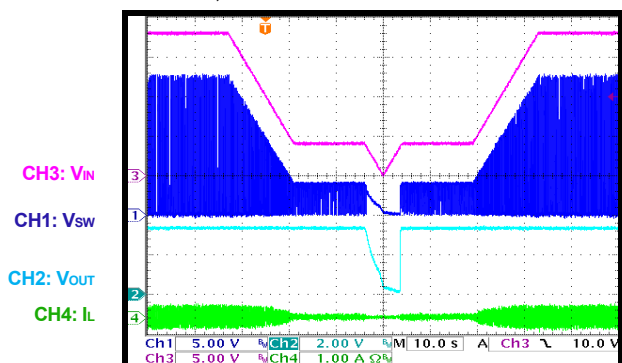


EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 3.3V$, $L = 2.2\mu H$, $f_{SW} = 2.2MHz$, $T_A = 25^\circ C$, unless otherwise noted.

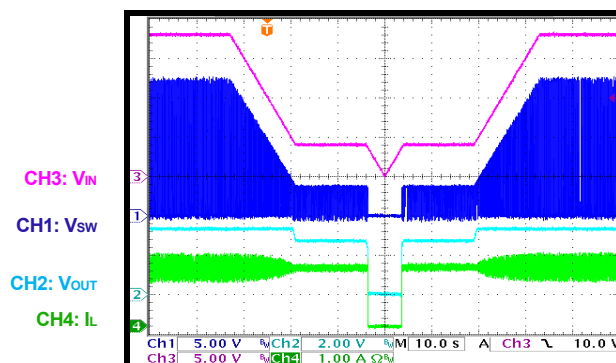
VIN Ramp Down and Up

$V_{IN} = 18V$ to $4.5V$ to $0V$ to $4.5V$ to $18V$,
 $I_{OUT} = 0A$, V_{OUT} connected to a diode with BST



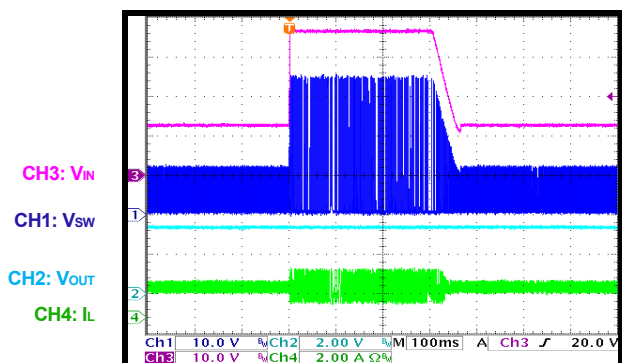
VIN Ramp Down and Up

$V_{IN} = 18V$ to $4V$ to $0V$ to $4V$ to $18V$, $I_{OUT} = 1.5A$



Load Dump

$V_{IN} = 12V$ to $36V$ to $12V$, $I_{OUT} = 1.5A$



PCB LAYOUT

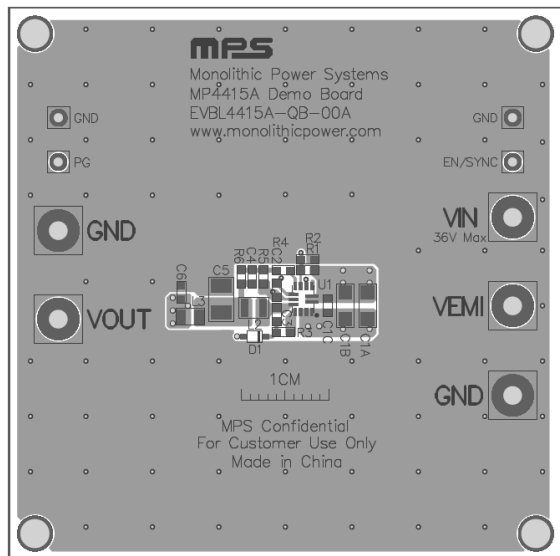


Figure 3: Top Silk Layer and Top Layer

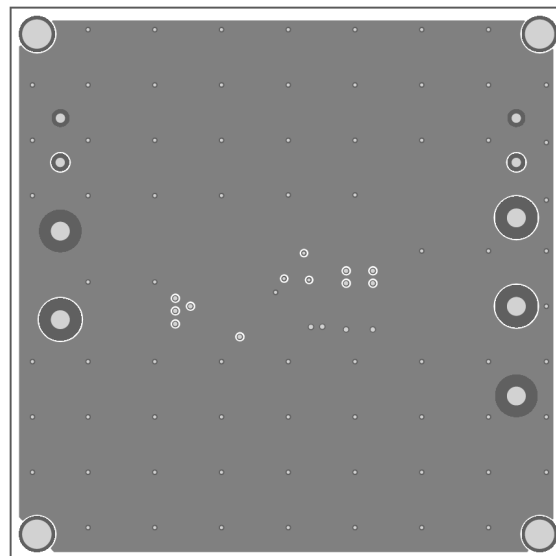


Figure 4: Inner Layer 1

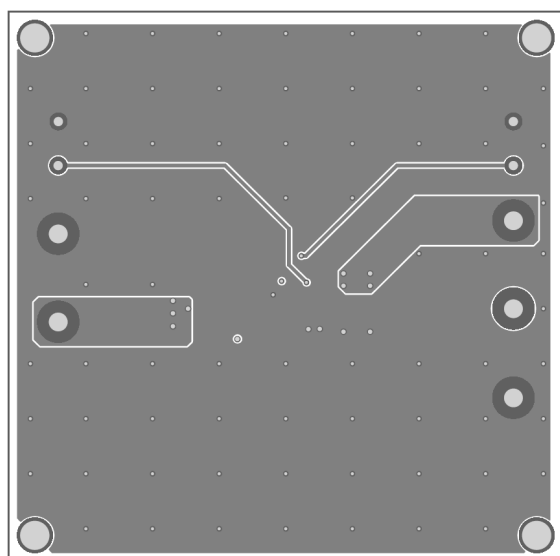


Figure 5: Inner Layer 2

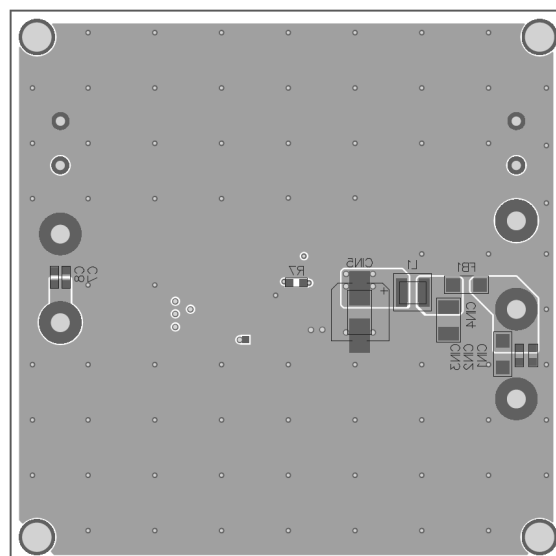


Figure 6: Bottom Silk Layer and Bottom Layer

**REVISION HISTORY**

Revision #	Revision Date	Description	Pages Updated
1.0	10/8/2019	Initial Release	-
1.1	9/10/2021	Updated BOM	Page 5
		Grammatical and clerical updates	All

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