



# EVBL4423H-Q-00A

## 36V, 3A, Synchronous, Step-Down Converter Evaluation Board

### DESCRIPTION

The EVBL4423H-Q-00A is an evaluation board designed to demonstrate the MP4423H and the MPQ4423H. The MP4423H is a high-frequency, synchronous, rectified, step-down switch-mode converter with built-in power MOSFETs and an integrated MPS power inductor. It offers a compact solution that can achieve up to 3A of continuous output current ( $I_{OUT}$ ) across a wide 4V to 36V input voltage ( $V_{IN}$ ) range, with excellent load and line regulation.

Synchronous mode provides high efficiency across the entire  $I_{OUT}$  range. Current-mode control provides fast transient response and eases loop stabilization.

Full protection features include over-current protection (OCP) with hiccup mode and thermal shutdown.

The EVBL4423H-Q-00A is a fully assembled and tested evaluation board. The MP4423H is available in a QFN-8 (3mmx3mm) package.

### ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Value	Units
Input voltage	$V_{IN}$	4 to 36	V
Output voltage	$V_{OUT}$	3.3	V
Output current	$I_{OUT}$	3	A

### FEATURES

- Wide 4V to 36V Operating Input Voltage ( $V_{IN}$ ) Range
- 85mΩ/55mΩ, Low  $R_{DS(ON)}$  Internal Power MOSFETs
- High-Efficiency Synchronous Mode
- 410kHz Default Switching Frequency ( $f_{SW}$ )
- 200kHz to 2.2MHz Synchronized External Clock
- High Duty Cycle for Automotive Cold-Crank Conditions
- Power-Save Mode (PSM)
- Internal Soft Start (SS)
- Power Good (PG)
- Over-Current Protection (OCP) with Hiccup Mode
- Thermal Shutdown
- Fully Assembled and Tested
- Available in a QFN-8 (3mmx3mm) Package
- Available in AEC-Q100 Grade 1



Optimized Performance with MPS Inductor MPL-AL6060 Series

### APPLICATIONS

- Automotive Applications
- Industrial Control Systems
- Distributed Power Systems

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## EVBL4423H-Q-00A EVALUATION BOARD

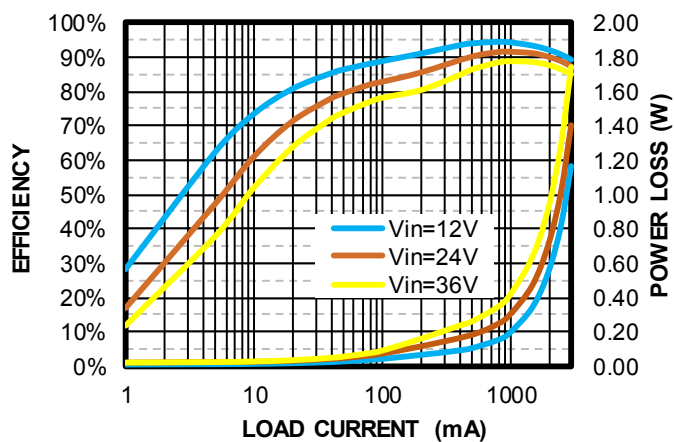


LxWxH (6.35cmx6.35cmx0.5cm)

Board Number	MPS IC Number	MPS Inductor
EVBL4423H-Q-00A	MP4423HGQ, MPQ4423HGQ	MPL-AL6060-100

### Efficiency vs. Load Current vs. Power Loss

$V_{OUT} = 3.3V$



## QUICK START GUIDE

1. Connect the load terminals to:
  - a. Positive (+): VOUT
  - b. Negative (-): GND
2. Preset the power supply between 4V and 36V, then turn the power supply off.
3. Connect the power supply terminals to:
  - a. Positive (+): VIN
  - b. Negative (-): GND
4. Turn the power supply on. The evaluation board should start up automatically.
5. To use the enable (EN) function, apply a digital input to the EN/SYNC pin. Pull EN/SYNC above 1.65V to turn the converter on; pull EN/SYNC below 1.05V or float EN/SYNC to turn it off. Connect an internal 500kΩ resistor between the EN/SYNC and GND pins to allow EN/SYNC to be floated.
6. Connect the EN/SYNC input pin to any voltage connected to the VIN pin via a pull-up resistor (R1). Ensure that R1 is large enough to limit the EN input current below 150μA. For example, if EN/SYNC is connected to a 12V VIN, then R1 should be ≥36.7kΩ.
7. To connect EN/SYNC directly to a voltage source without using a pull-up resistor, the voltage amplitude should be limited to ≤6V to prevent damage to the internal Zener diode at EN/SYNC.
8. After the output voltage (VOUT) is set, connect the EN/SYNC input pin to a 200kHz to 2.2MHz external clock to synchronize the internal clock's rising edge to the external clock's rising edge. The external clock's pulse-width signal should be below 1.7μs.
9. Use R7 and R8 to set VOUT. R8 can be calculated by Equation (1):

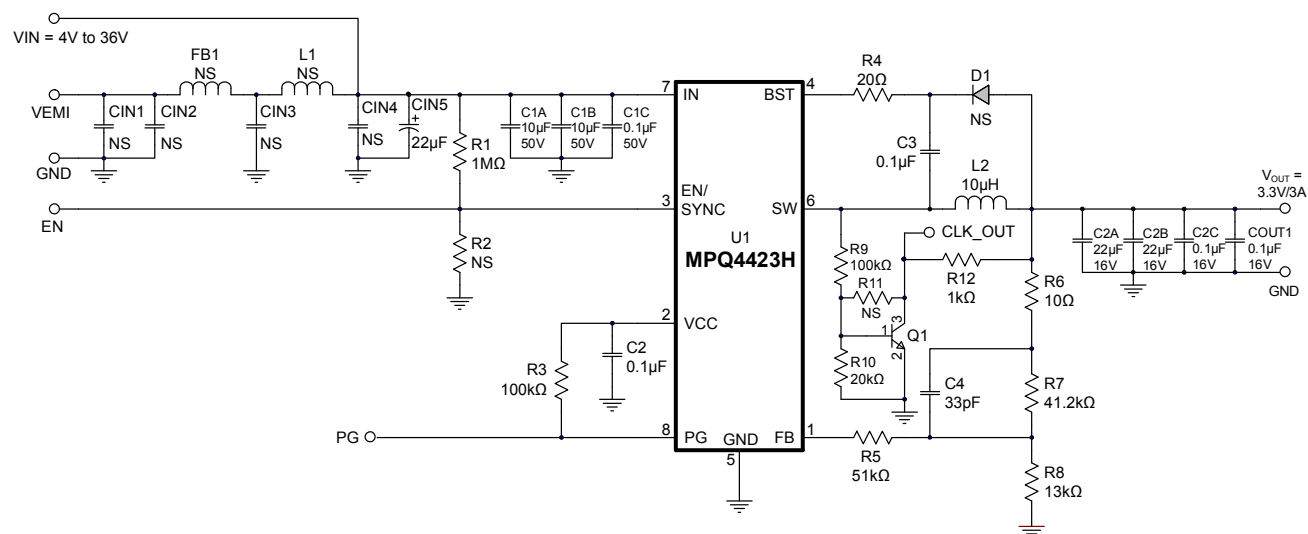
$$R8 = \frac{R7}{\frac{V_{OUT}}{0.792} - 1} \quad (1)$$

Where R7 is 41.2kΩ, and VFB is 0.792V.

If VOUT is changed, refer to the Application Information section in the MP4423H/MPQ4423H datasheet to calculate the compensation, inductance, and output capacitance.

10. CLK\_OUT is a signal inverted to SW that can be used as another buck's SYNC signal to operate 180° out-of-phase. The CLK\_OUT high voltage is equal to VOUT. Ensure that it is safe to operate the synchronized part while VOUT is high.

## EVALUATION BOARD SCHEMATIC



### Figure 1: Evaluation Board Schematic

**EVBL4423H-Q-00A BILL OF MATERIALS**

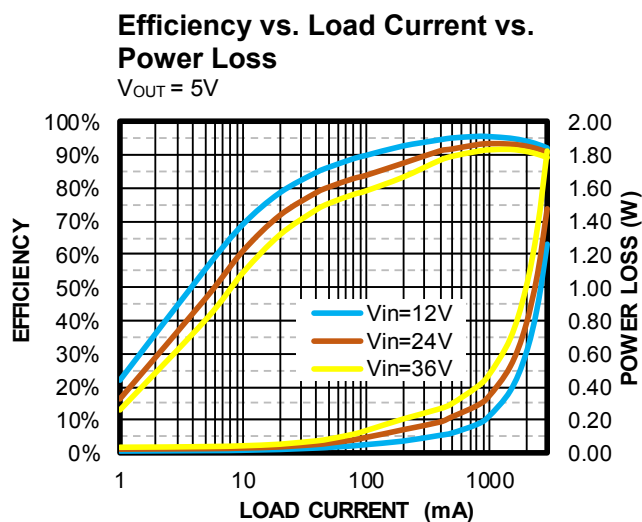
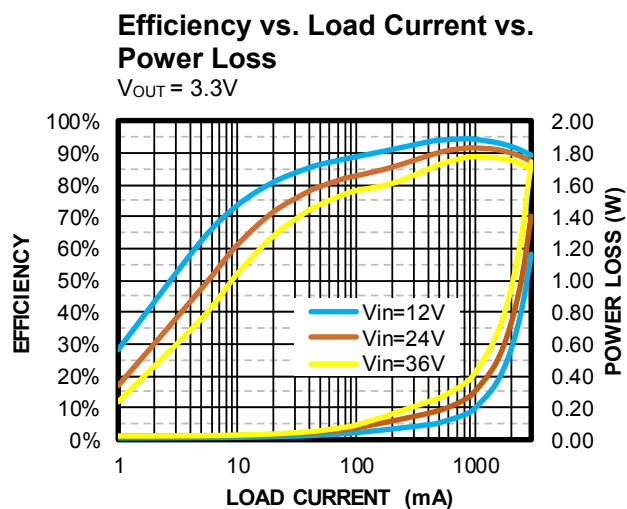
Qty	Ref	Value	Description	Package	Manufacturer	Manufacturer PN
2	C1A, C1B	10 $\mu$ F	Ceramic capacitor, 50V, X7R	1210	Murata	GRM32ER71H106KA12L
1	C1C	0.1 $\mu$ F	Ceramic capacitor, 50V, X7R	0603	Murata	GRM188R71H104KA93D
2	C2A, C2B	22 $\mu$ F	Ceramic capacitor, 16V, X7R	1210	Murata	GRM32ER71C226KE79
4	C2, C2C, C3, COUT1	0.1 $\mu$ F	Ceramic capacitor, 16V, X7R	0603	Murata	GRM188R71C104KA01D
1	C4	33pF	Ceramic capacitor, 50V, C0G	0603	Murata	GRM1885C1H330JA01D
4	CIN1, CIN2, CIN3, CIN4	NS				
1	CIN5	22 $\mu$ F	Electrolytic capacitor	SMD	Jianghai	VTD-63V22
1	D1	NS				
1	FB1	NS				
1	L1	NS				
1	R1	1M $\Omega$	Film resistor, 5%	0603	Yageo	RC0603JR-071ML
2	R3, R9	100k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-07100KL
1	R4	20 $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0720RL
1	R5	51k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0751KL
1	R6	10 $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0710RL
1	R7	41.2k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0741K2L
1	R8	13k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0713KL
1	R10	20k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-0720KL
1	R12	1k $\Omega$	Film resistor, 1%	0603	Yageo	RC0603FR-071KL
2	R2, R11	NS				
5	VIN, VEMI, GND, VOUT, GND	2mm	2mm golden test pin	DIP	Custom <sup>(1)</sup>	
5	EN/SYNC, GND, PG, GND, CLK_OUT	1mm	1mm golden pin	DIP	Custom <sup>(1)</sup>	
1	Q1	40V	Transistor, 0.2A	SOT-23	ON Semiconductor	MMBT3904LT1
1	L2	MPL-AL6060-100	Inductor, 10 $\mu$ H, 7A, DCR = 27m $\Omega$	SMD	MPS	MPL-AL6060-100
1	U1	MPQ4423H	Step-down converter, 36V, 3A	QFN-8 (3mmx3mm)	MPS	MPQ4423HGQ

**Note:**

1) These pins are custom-made by MPS. Contact an MPS FAE for more information.

## EVB TEST RESULTS

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

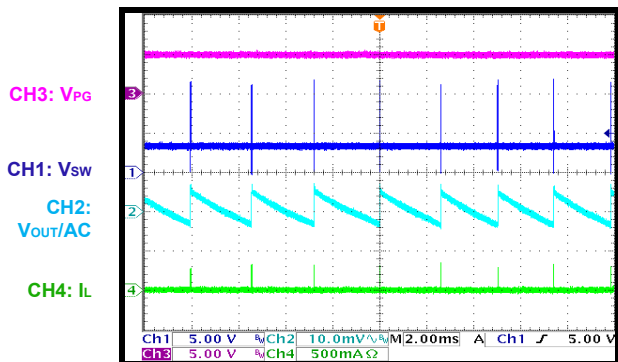


## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

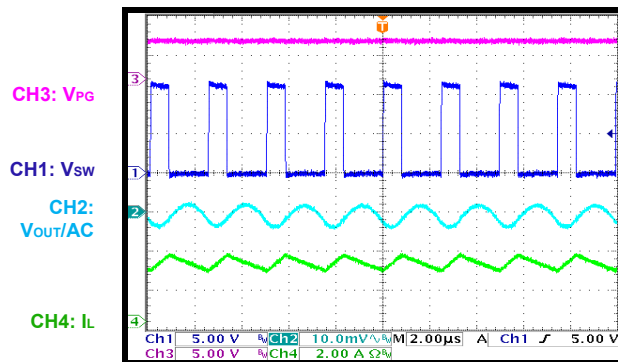
### Steady State

$I_{OUT} = 0A$



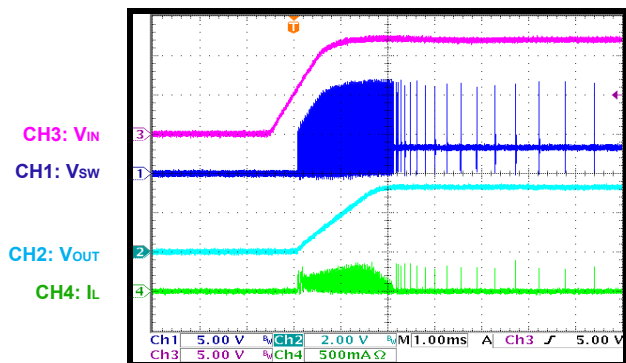
### Steady State

$I_{OUT} = 3A$



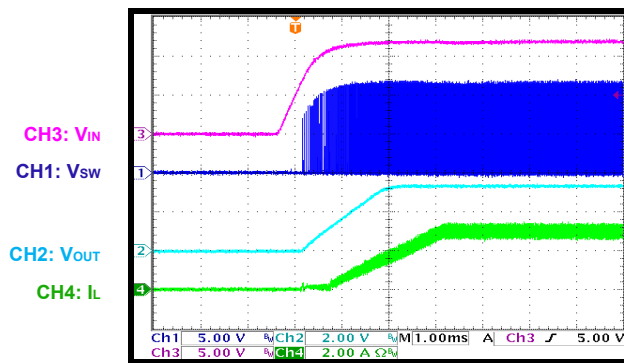
### Start-Up

$I_{OUT} = 0A$



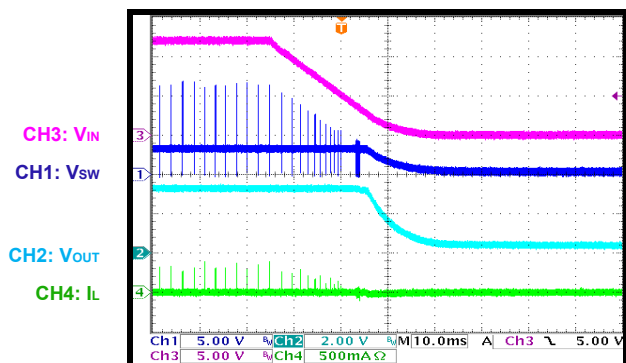
### Start-Up

$I_{OUT} = 3A$



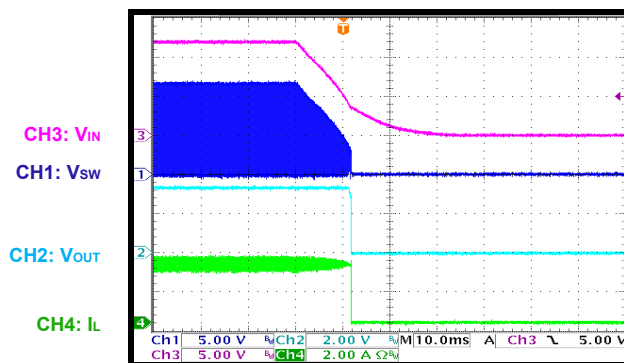
### Shutdown

$I_{OUT} = 0A$



### Shutdown

$I_{OUT} = 3A$

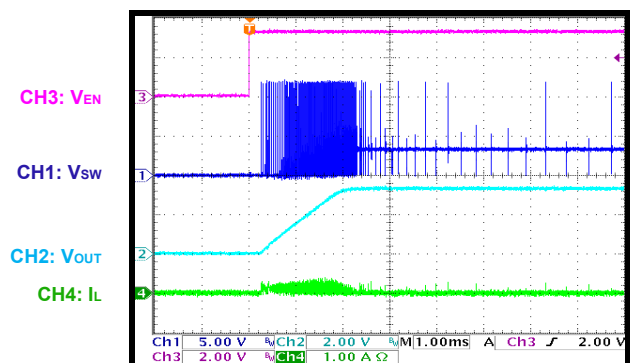


## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

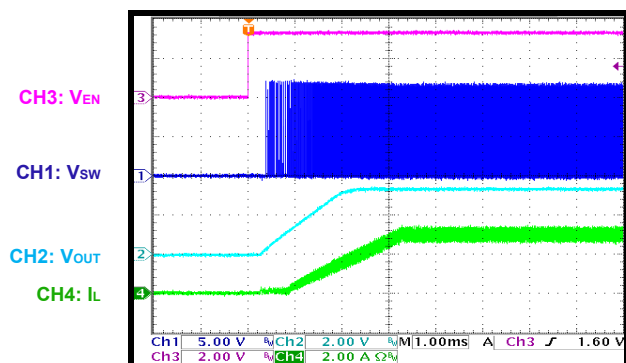
### Start-Up through EN

$I_{OUT} = 0A$



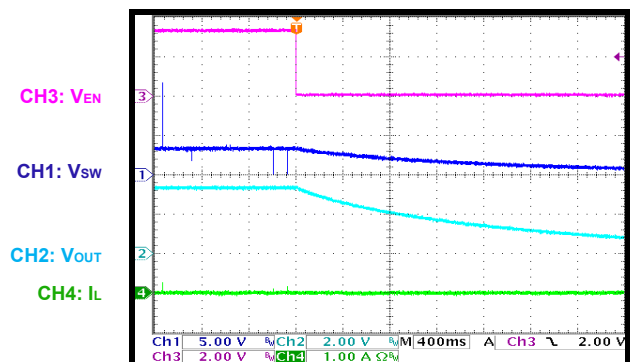
### Start-Up through EN

$I_{OUT} = 3A$



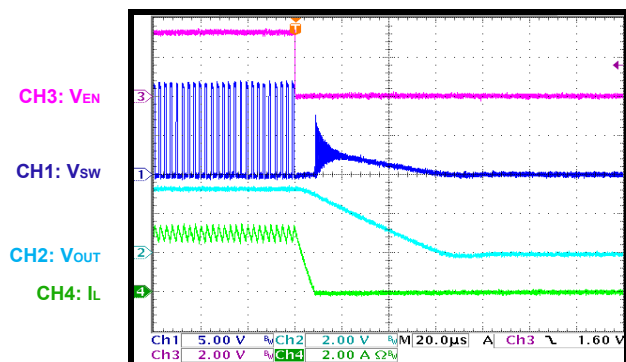
### Shutdown through EN

$I_{OUT} = 0A$



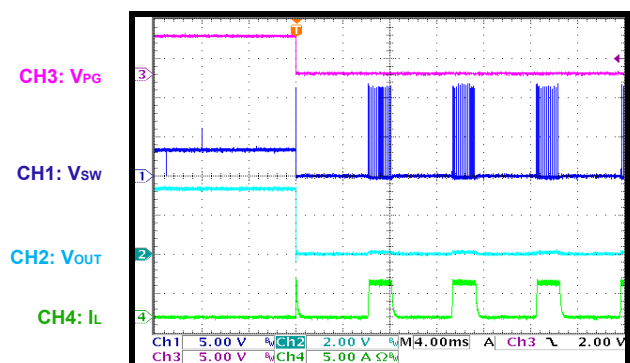
### Shutdown through EN

$I_{OUT} = 3A$



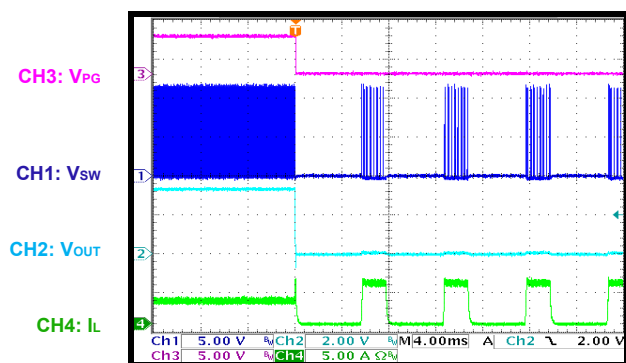
### SCP Entry

$I_{OUT} = 0A$



### SCP Entry

$I_{OUT} = 3A$

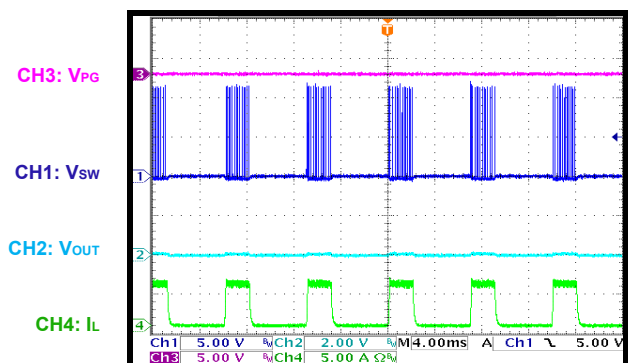




## EVB TEST RESULTS *(continued)*

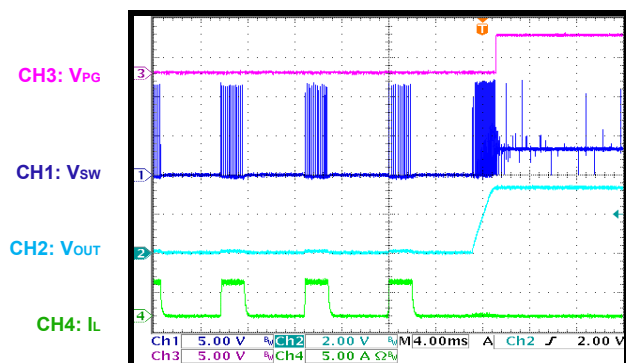
$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

### SCP Steady State



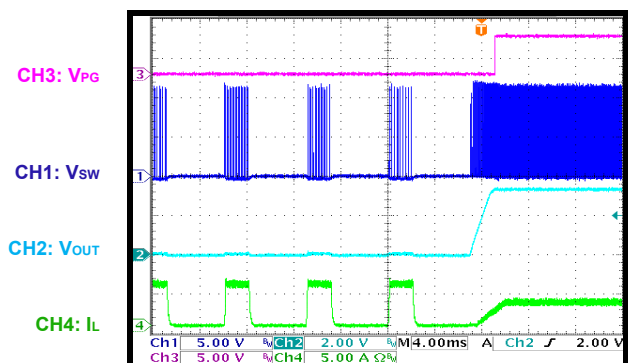
### SCP Recovery

$I_{OUT} = 0A$



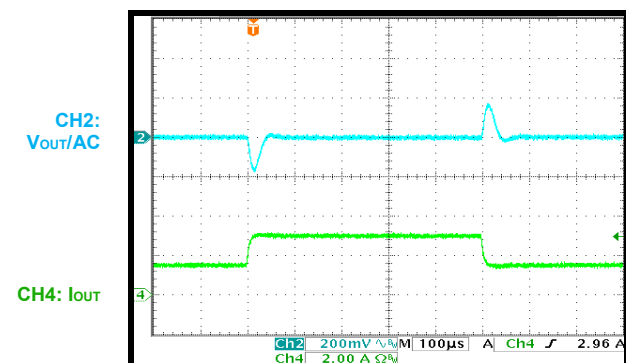
### SCP Recovery

$I_{OUT} = 3A$



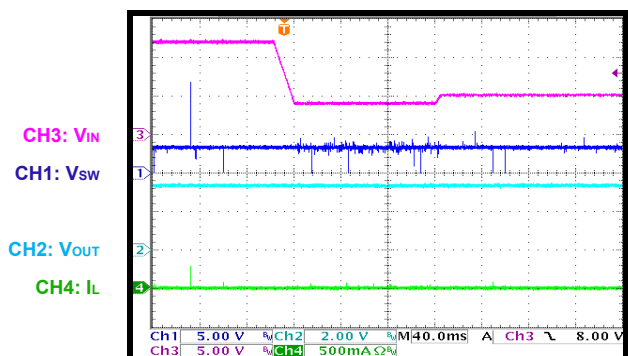
### Load Transient

$I_{OUT} = 1.5A$  to  $3A$



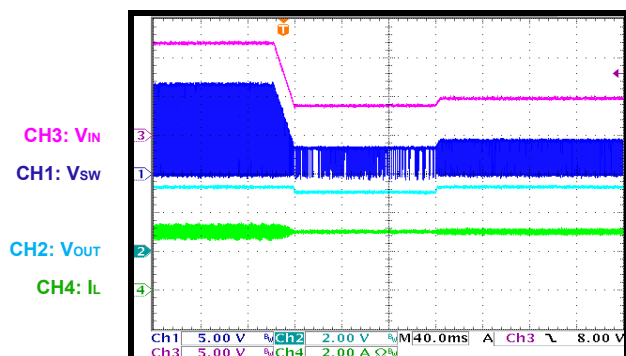
### Cold Crank

$V_{IN} = 12V$  to  $4V$  to  $5V$ ,  $I_{OUT} = 0A$



### Cold Crank

$V_{IN} = 12V$  to  $4V$  to  $5V$ ,  $I_{OUT} = 3A$

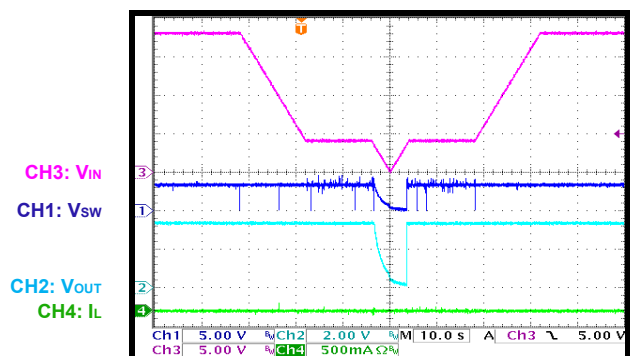


## EVB TEST RESULTS *(continued)*

$V_{IN} = 12V$ ,  $V_{OUT} = 3.3V$ ,  $C_{OUT} = 2 \times 22\mu F$ ,  $L = 10\mu H$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

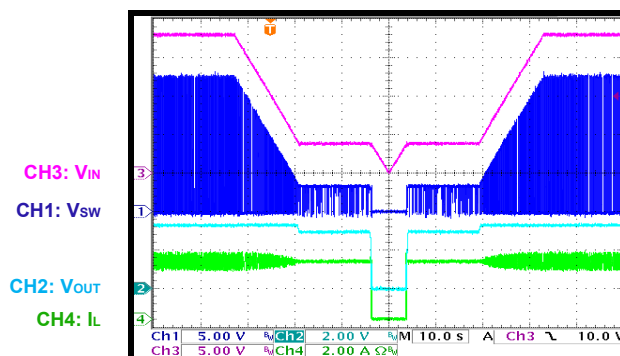
### $V_{IN}$ Ramps Down and Up

$V_{IN} = 18V$  to  $4V$  to  $0V$  to  $4V$  to  $18V$ ,  $I_{OUT} = 0A$



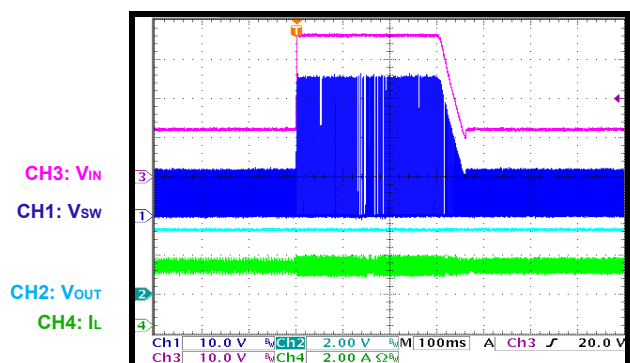
### $V_{IN}$ Ramps Down and Up

$V_{IN} = 18V$  to  $4V$  to  $0V$  to  $4V$  to  $18V$ ,  $I_{OUT} = 3A$



### Load Dump

$V_{IN} = 12V$  to  $36V$  to  $12V$ ,  $I_{OUT} = 3A$



## PCB LAYOUT

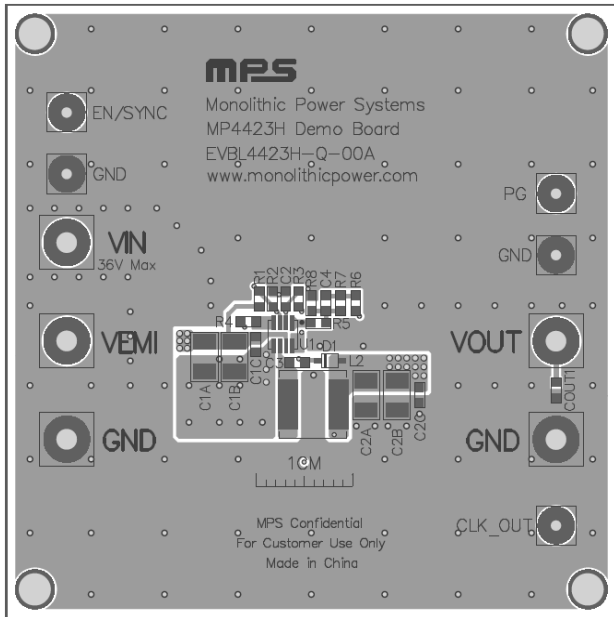


Figure 2: Top Silk and Top Layer

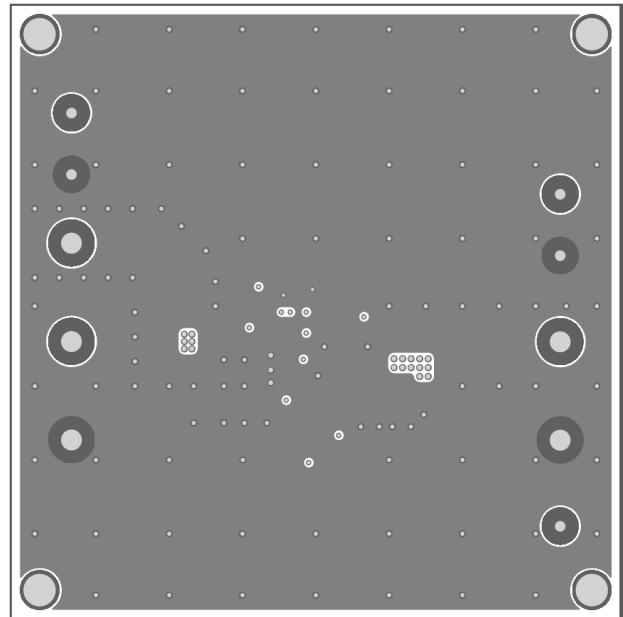


Figure 3: Mid-Layer 1

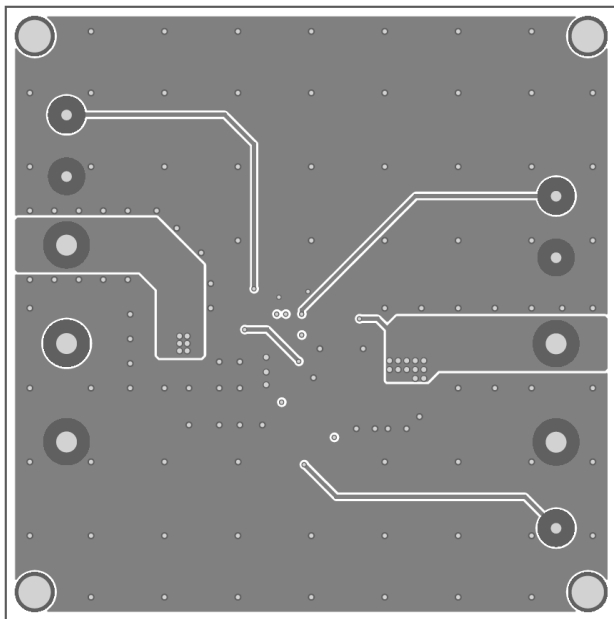


Figure 4: Mid-Layer 2

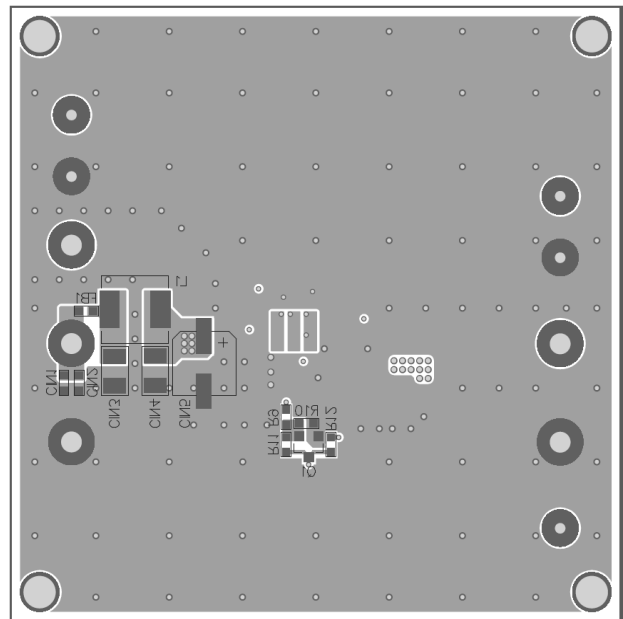


Figure 5: Bottom Silk Layer and Bottom Layer



## REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	9/29/2019	Initial Release	-
1.1	10/21/2021	Updated the footnote below the Applications section	1
		Updated the Quick Start Guide section	2
		Updated the graph and waveform titles in the EVB Test Results section	6–10
		Grammar and formatting updates; updated pagination; updated figure titles; updated headers	All

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