

## DESCRIPTION

The MP62350/MP62351 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62350/MP62351 analog switch has 85mΩ on-resistance and operates from 2.7V to 5.5V input. It is available with guaranteed current limits, making it ideal for load switching applications. The MP62350/MP62351 has built-in protection for both over current and increased thermal stress. For over current, the device will limit the current by changing to a constant current mode.

As the temperature increases as a result of short circuit, then the device will shut off. The device will recover once the device temperature reduces to approx 120°C.

The MP62350/MP62351 included a discharge function that provides a resistive discharge path for the external output capacitor when the part is disabled.

The MP62350/MP62351 is available in 8-pin MSOP and SOIC packages.

## FEATURES

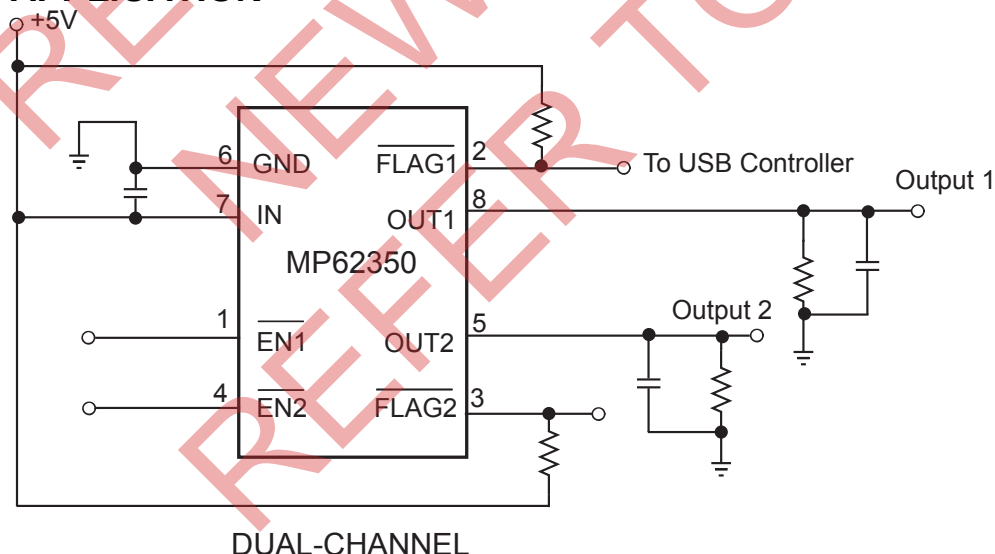
- 500mA Continuous Current
- Accurate Current Limit
- Output Discharge Function
- 2.7V to 5.5V Supply Range
- 140uA Quiescent Current
- 85mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- Active High & Active Low Options
- UL Recognized: Pending

## APPLICATIONS

- Smartphone and PDA
- Portable GPS Device
- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

"MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

## TYPICAL APPLICATION

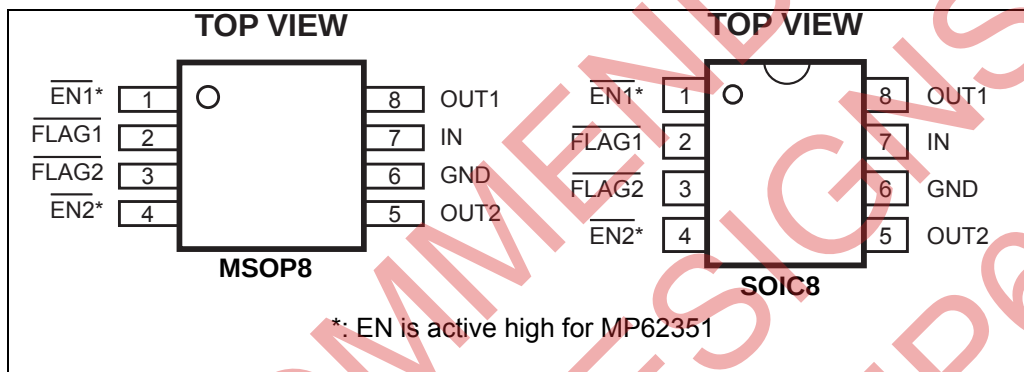


## ORDERING INFORMATION

| Part Number | Enable      | Switch | Maximum Continuous Load Current | Typical Short-Circuit Current @ T <sub>A</sub> =25°C | Package | Temperature    |
|-------------|-------------|--------|---------------------------------|------------------------------------------------------|---------|----------------|
| MP62351ES   | Active High | Dual   | 0.5A                            | 750mA                                                | SOIC8   | –20°C to +85°C |
| MP62351EK   | Active High | Dual   | 0.5A                            | 750mA                                                | MSOP8   |                |
| MP62350ES   | Active Low  | Dual   | 0.5A                            | 750mA                                                | SOIC8   |                |
| MP62350EK   | Active Low  | Dual   | 0.5A                            | 750mA                                                | MSOP8   |                |

\* For Tape & Reel, add suffix –Z (eg. MP62350/MP62351ES–Z). For RoHS Compliant Packaging, add suffix –LF (eg. MP62350/MP62351ES–LF–Z)

## PACKAGE REFERENCE



## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                      |                 |
|----------------------------------------------------------------------|-----------------|
| IN                                                                   | –0.3V to +6.0V  |
| EN, FLAG, OUT to GND                                                 | –0.3V to +6.0V  |
| Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup> |                 |
| SOIC8                                                                | 1.4W            |
| MSOP8                                                                | 0.8W            |
| Junction Temperature                                                 | 150°C           |
| Lead Temperature                                                     | 260°C           |
| Storage Temperature                                                  | –65°C to +150°C |
| Operating Temperature                                                | –20°C to +85°C  |

## Thermal Resistance <sup>(3)</sup>

|       | θ <sub>JA</sub> | θ <sub>JC</sub> |
|-------|-----------------|-----------------|
| SOIC8 | 90              | 42              |
| MSOP8 | 150             | 65              |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)–T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB.

**ELECTRICAL CHARACTERISTICS <sup>(4)</sup>****V<sub>IN</sub>=5V, T<sub>A</sub>=+25°C, unless otherwise noted.**

| Parameter                                        | Condition                                                      | Min  | Typ | Max  | Units |
|--------------------------------------------------|----------------------------------------------------------------|------|-----|------|-------|
| IN Voltage Range                                 |                                                                | 2.7  |     | 5.5  | V     |
| Supply Current                                   | One Channel Enabled, I <sub>OUT</sub> =0, One Switch ON        |      | 90  | 120  | μA    |
| Supply Current                                   | Both Channels Enabled, I <sub>OUT</sub> =0, Both Switches ON   |      | 140 | 160  | μA    |
| Shutdown Current                                 | Device Disable, V <sub>OUT</sub> =float, V <sub>IN</sub> =5.5V |      | 1   |      | μA    |
| Off Switch Leakage                               | Device Disable, V <sub>IN</sub> =5.5V                          |      | 1   |      | μA    |
| Current Limit                                    |                                                                | 550  |     | 1100 | mA    |
| Trip Current                                     | Current Ramp (slew rate≤100A/s) on Output                      |      | 1   | 1.4  | A     |
| Under-voltage Lockout                            | Rising Edge                                                    | 1.95 |     | 2.65 | V     |
| Under-voltage Hysteresis                         |                                                                |      | 250 |      | mV    |
| FET On Resistance                                | I <sub>OUT</sub> =100mA ( -20°C≤T <sub>A</sub> ≤85°C)          |      | 85  | 130  | mΩ    |
| EN Input Logic High Voltage                      |                                                                | 2    |     |      | V     |
| EN Input Logic Low Voltage                       |                                                                |      |     | 0.8  | V     |
| FLAG Output Logic Low Voltage                    | I <sub>SINK</sub> =5mA                                         |      |     | 0.4  | V     |
| FLAG Output High Leakage Current                 | V <sub>IN</sub> =V <sub>FLAG</sub> =5.5V                       |      |     | 1    | μA    |
| Thermal Shutdown                                 |                                                                |      | 140 |      | °C    |
| Thermal Shutdown Hysteresis                      |                                                                |      | 20  |      | °C    |
| V <sub>OUT</sub> Rising Time, Tr <sup>(5)</sup>  | V <sub>IN</sub> =5.5V, CL=1μF, RL=11Ω                          |      | 0.9 |      | ms    |
|                                                  | V <sub>IN</sub> =2.7V, CL=1μF, RL=11Ω                          |      | 1.7 |      | ms    |
| V <sub>OUT</sub> Falling Time, Tf <sup>(6)</sup> | V <sub>IN</sub> =5.5V, CL=1μF, RL=11Ω                          |      |     | 0.5  | ms    |
|                                                  | V <sub>IN</sub> =2.7V, CL=1μF, RL=11Ω                          |      |     | 0.5  | ms    |
| Turn On Time, Ton <sup>(7)</sup>                 | C <sub>L</sub> =100μF, RL=11Ω                                  |      |     | 3    | ms    |
| Turn Off Time, Toff <sup>(8)</sup>               | C <sub>L</sub> =100μF, RL=11Ω                                  |      |     | 10   | ms    |
| Discharge Resistance                             |                                                                |      | 100 |      | Ω     |
| FLAG Deglitch Time                               |                                                                | 4    | 8   | 15   | ms    |
| ENx Input Leakage                                |                                                                |      | 1   |      | μA    |
| Reverse Leakage Current                          | OUTX=5.5V, IN=GND                                              |      | 0.2 |      | μA    |

**Notes:**

- 4) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.  
 5) Measured from 10% to 90%.  
 6) Measured from 90% to 10%.  
 7) Measured from (50%) EN signal to (90%) output signal.  
 8) Measured from (50%) EN signal to (10%) output signal.

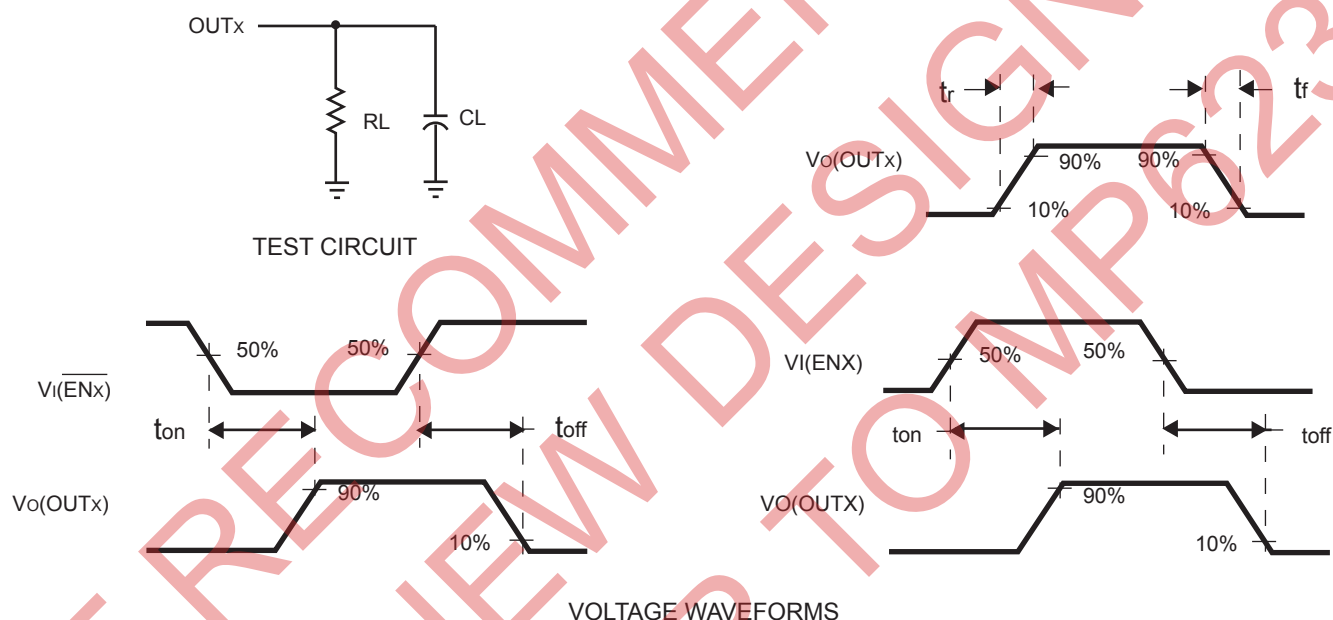
## PIN FUNCTIONS

### MP62350/MP62351

| Pin# | Name                      | Description                                                  |
|------|---------------------------|--------------------------------------------------------------|
| 1    | $\overline{\text{EN1}}$   | Active Low: (MP62350), Active High: (MP62351)                |
| 2    | $\overline{\text{FLAG1}}$ | IN-to-OUT1 Over-current, active-low output flag. Open-Drain. |
| 3    | $\overline{\text{FLAG2}}$ | IN-to-OUT2 Over-current, active-low output flag. Open-Drain. |
| 4    | $\overline{\text{EN2}}$   | Active Low: (MP62350), Active High: (MP62351)                |
| 5    | OUT2                      | IN-to-OUT2 Power-Distribution Switch Output.                 |
| 6    | GND                       | Ground.                                                      |
| 7    | IN                        | Input Voltage. Accepts 2.7V to 5.5V input.                   |
| 8    | OUT1                      | IN-to-OUT1 Power-Distribution Switch Output                  |

## TYPICAL PERFORMANCE CHARACTERISTICS

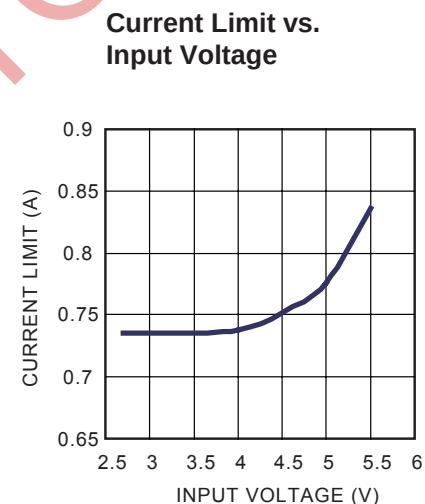
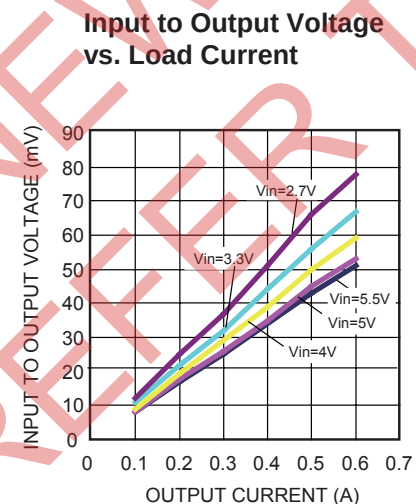
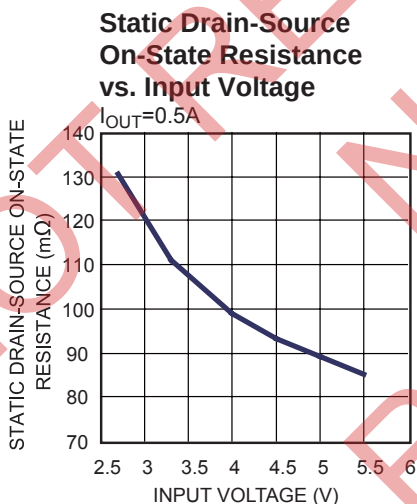
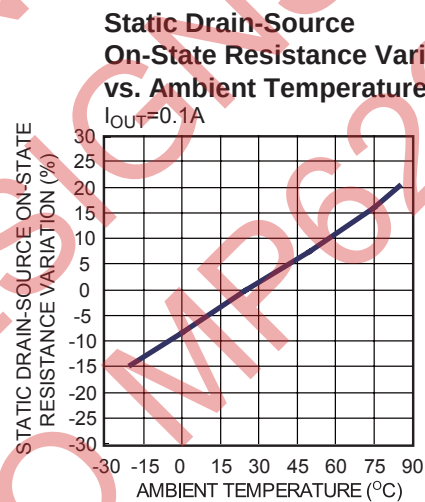
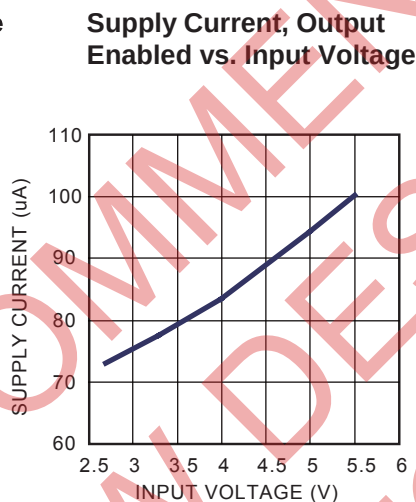
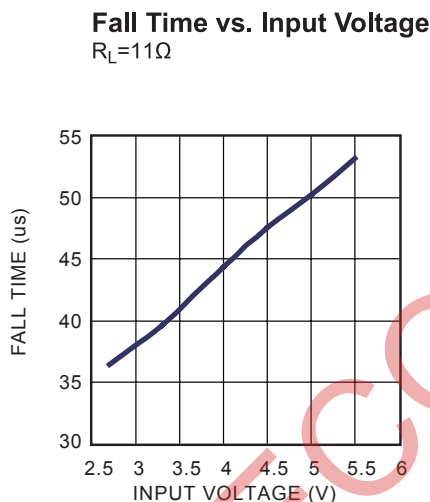
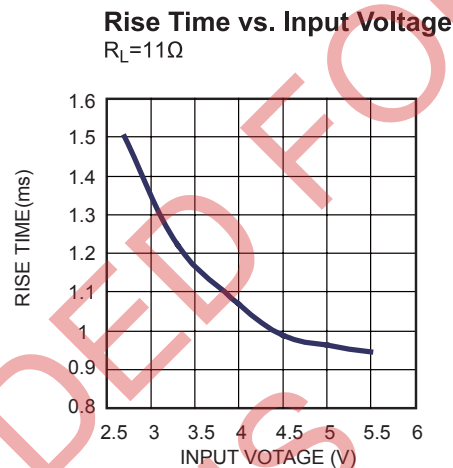
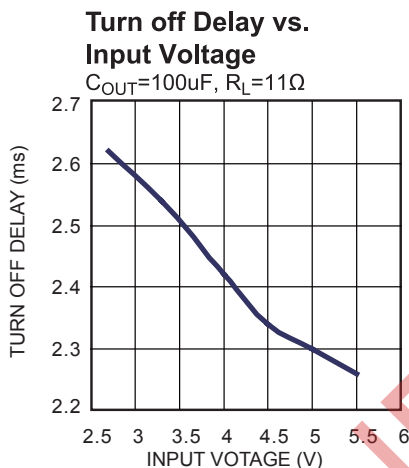
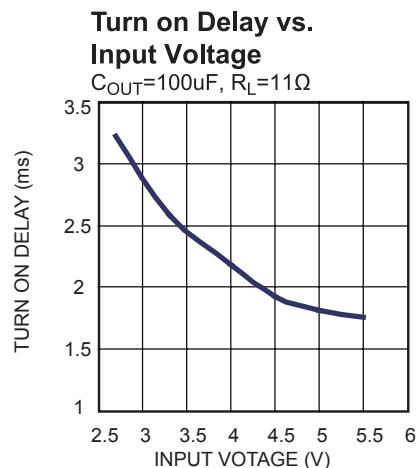
$T_A = +25^\circ\text{C}$ , unless otherwise noted.



**Figure 1—Test Circuit and Voltage Waveforms**

## TYPICAL PERFORMANCE CHARACTERISTICS

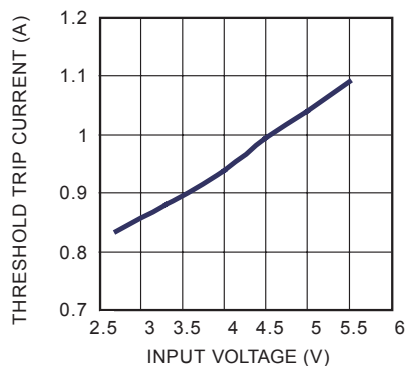
$V_{IN}=5V$ ,  $V_{EN}=0V$ ,  $C_L=1\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.



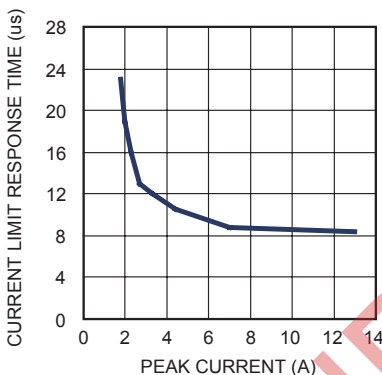
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}=5V$ ,  $V_{EN}=0V$ ,  $C_L=1\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

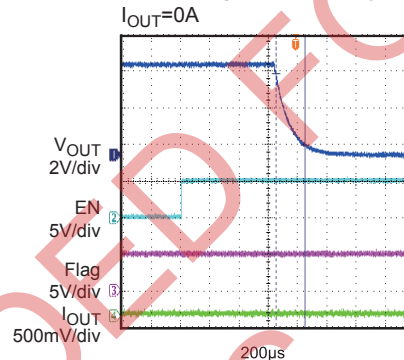
Threshold Trip Current  
vs. Input Voltage



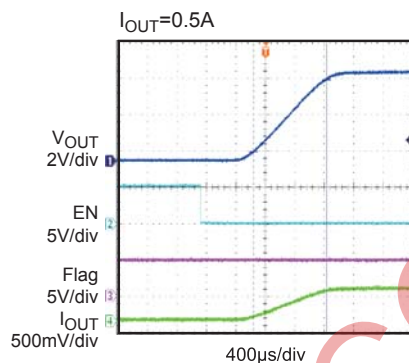
Current Limit Response  
vs. Peak Current



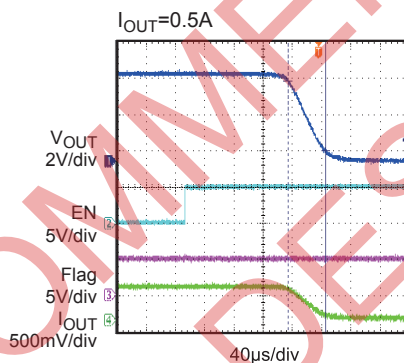
Turn Off Delay and Fall Time  
with Output Discharge



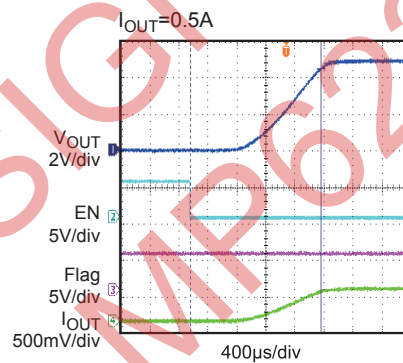
Turn On Delay and Rise Time  
with 1μF Load



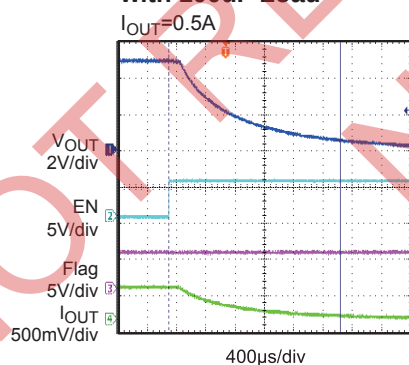
Turn Off Delay and Fall Time  
with 1μF Load



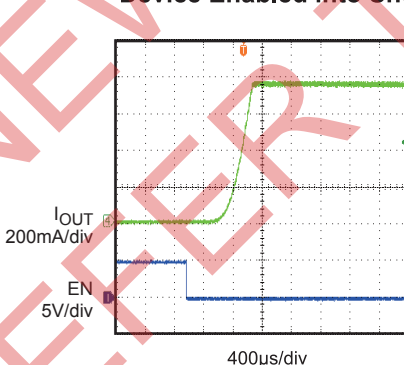
Turn On Delay and Rise Time  
with 100μF Load



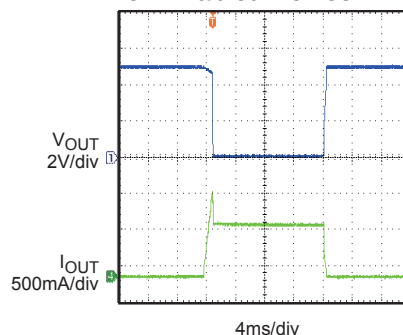
Turn Off Delay and Fall Time  
with 100μF Load



Short Circuit Current,  
Device Enabled into Short



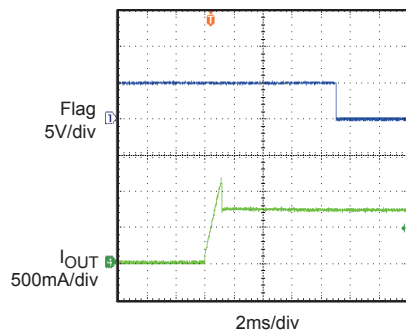
Threshold Trip Current  
with Ramped Load  
on Enabled Device



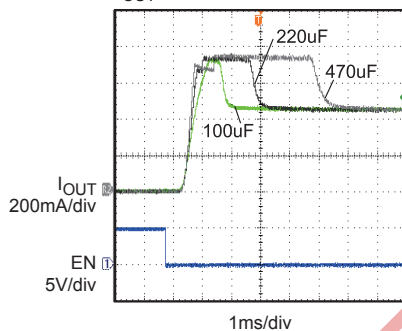
## TYPICAL PERFORMANCE CHARACTERISTICS (*continued*)

$V_{IN}=5V$ ,  $V_{EN}=0V$ ,  $C_L=1\mu F$ ,  $T_A = +25^\circ C$ , unless otherwise noted.

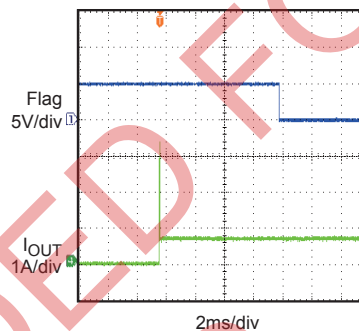
**Ramped Load  
on Enabled Device**



**Inrush Current with  
Different Load Capacitance**  
 $I_{OUT}=0.5A$



**$1\Omega$  Load  
Connected to Enabled Device**





The schematic diagram illustrates the internal architecture of the L64790 dual-channel motor driver. It features two identical channels, each processing an input signal (IN1, IN2) through a logic block, a thermal sense block, a charge pump, a UVLO block, an AMP, a current sense block, and a deglitch block. The output of each channel is OUT1 and OUT2, which are connected to a motor through a 100Ω resistor and a Vref source. The output is also connected to a FLAG1 and FLAG2 pin. The diagram is labeled 'RECOMMENDED' and 'Schematic'.

### Figure 2—Functional Block Diagram



## DETAILED DESCRIPTION

### Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62350/MP62351 switches into to a constant-current mode (current limit value). MP62350/MP62351 will be shutdown only if the overcurrent condition stays long enough to trigger thermal protection.

Trigger overcurrent protection for different overload conditions occurring in applications:

- 1) The output has been shorted or overloaded before the device is enabled or input applied. MP62350/MP62351 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
- 3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. The MP62350/MP62351 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

### Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after an 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during an over temp. or a voltage lockout.

### Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing exceptive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

### Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62350/MP62351 is operating correctly. This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

### Enable

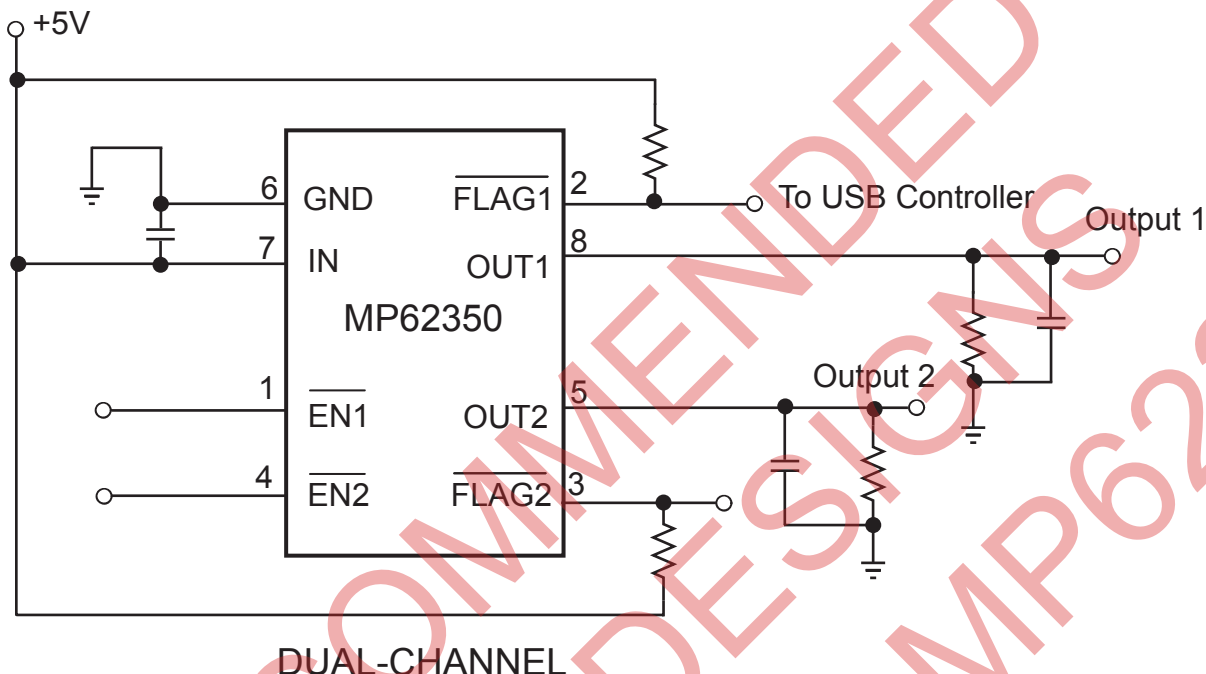
The logic pin disables the chip to reduce the supply current. The device will operate once the enable signal reaches the appropriate level. The input is compatible with both COMS and TTL.

## APPLICATION INFORMATION

### Power-Supply Considerations

Over 10 $\mu$ F capacitor between IN and GND is recommended. This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

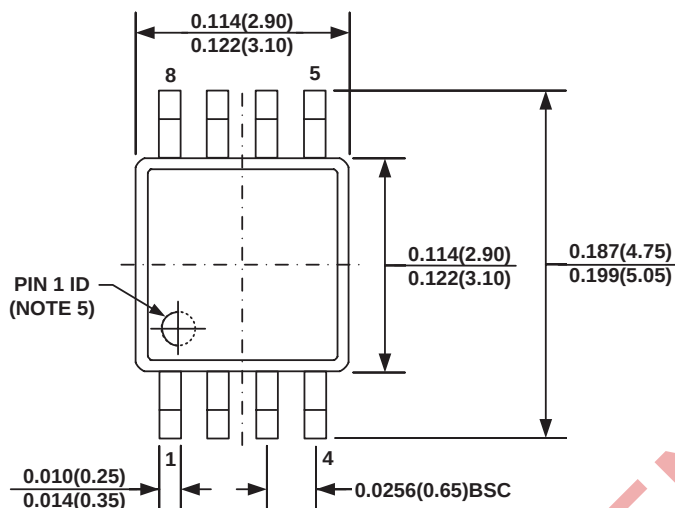


DUAL-CHANNEL

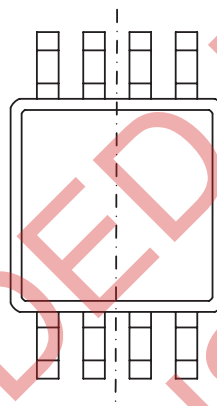
Figure 3—Application Circuit

## PACKAGE INFORMATION

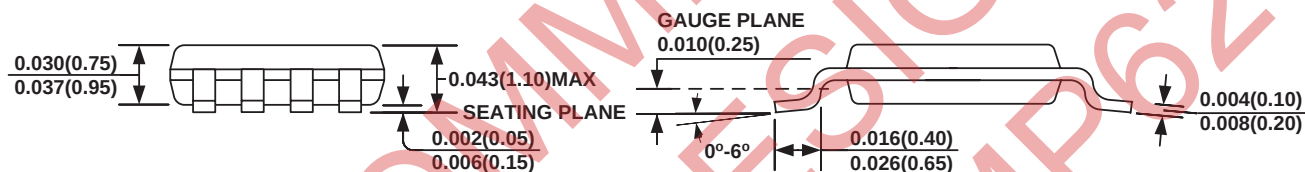
### MSOP8



**TOP VIEW**

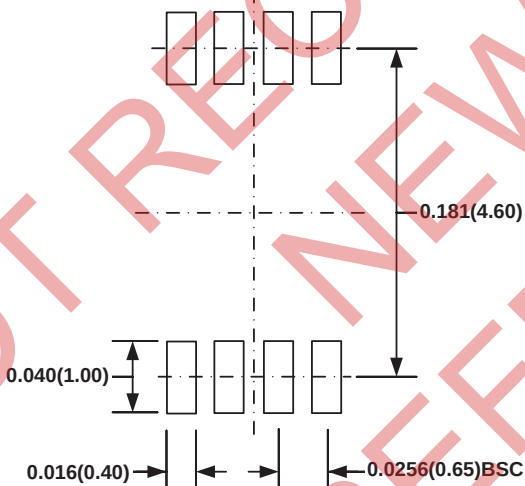


**BOTTOM VIEW**



**FRONT VIEW**

**SIDE VIEW**

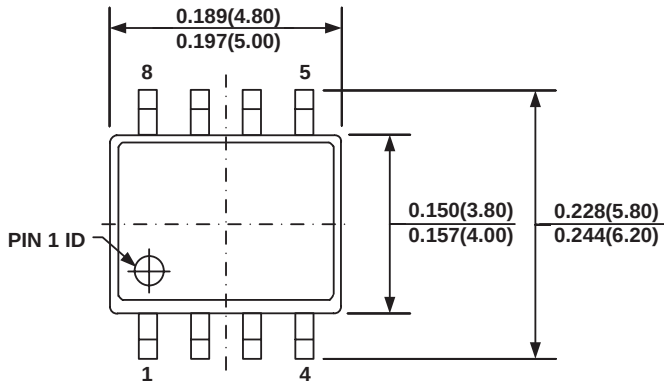


**RECOMMENDED LAND PATTERN**

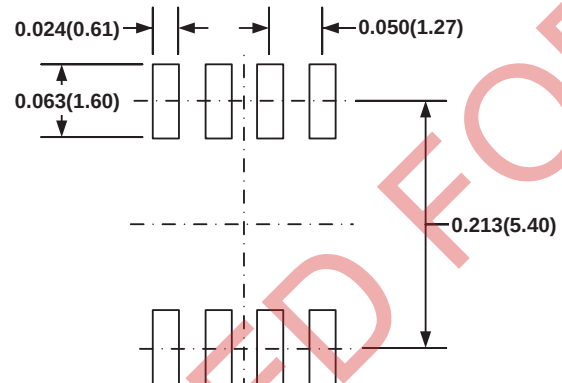
#### NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
- 6) DRAWING MEETS JEDEC MO-187, VARIATION AA.
- 7) DRAWING IS NOT TO SCALE.

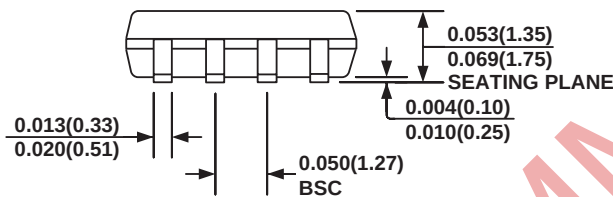
**SOIC8**



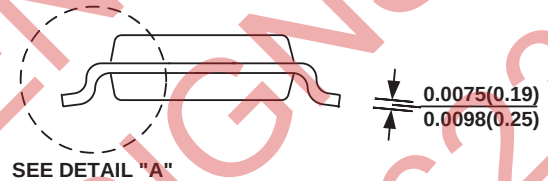
**TOP VIEW**



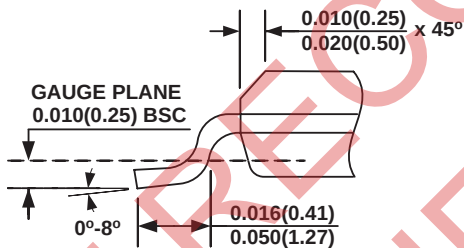
**RECOMMENDED LAND PATTERN**



**FRONT VIEW**



**SIDE VIEW**



**DETAIL "A"**

**NOTE:**

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION AA.
- 6) DRAWING IS NOT TO SCALE.

**NOTICE:** The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.