



# MP6604C

4.5V to 45V, 2.5A,  
Simple Dual H-Bridge Driver (HS/LS)

## DESCRIPTION

The MP6604C is a dual H-bridge motor driver IC designed to drive stepper motors, brushed DC motors, and other loads.

The MP6604C operates across a 4.5V to 45V input voltage ( $V_{IN}$ ) range. It can deliver motor current up to 2.5A per phase, depending on the ambient temperature ( $T_A$ ) and PCB layout.

Internal safety and diagnostic features include over-current protection (OCP), input over-voltage protection (OVP), input under-voltage protection (UVP), and thermal shutdown.

The MP6604C has separate HS and LS input pins for each output pin.

The MP6604C is available in QFN-28 (4mmx5mm) and TSSOP-28EP packages.

## FEATURES

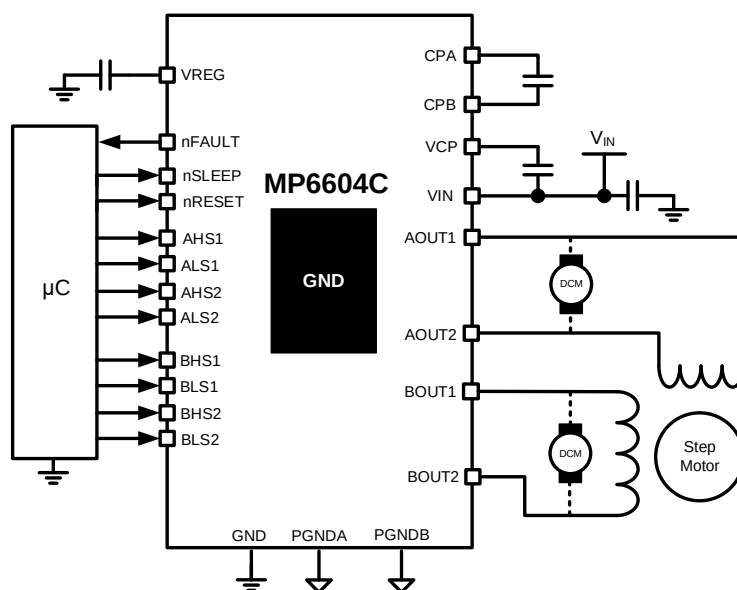
- 4.5V to 45V Operating Input Voltage ( $V_{IN}$ ) Range
- 2.5A Maximum Output Current ( $I_{OUT\_MAX}$ )
- Dual H-Bridge or Quad Half H-Bridge Driver
- Low 150m $\Omega$  On Resistance ( $R_{DS(ON)}$ ) per MOSFET
- Protection Functions Include:
  - Over-Current Protection (OCP)
  - Over-Voltage Protection (OVP)
  - Under-Voltage Protection (UVP)
  - Over-Temperature (OT) Shutdown
  - Fault Indication Output
- Available in QFN-28 (4mmx5mm) and TSSOP-28EP Packages

## APPLICATIONS

- Bipolar Stepper Motors
- Stage Lighting
- 3D Printers
- Laser Printers and Copiers
- Textile Machines

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## TYPICAL APPLICATION



## ORDERING INFORMATION

| Part Number* | Package          | Top Marking | MSL Rating |
|--------------|------------------|-------------|------------|
| MP6604CGV    | QFN-28 (4mmx5mm) | See Below   | 2          |
| MP6604CGF    | TSSOP-28EP       | See Below   | 2a         |

\* For Tape & Reel, add suffix -Z (e.g. MP6604CGV-Z).

\* For Tape & Reel, add suffix -Z (e.g. MP6604CGF-Z).

### TOP MARKING (MP6604CGV)

**MPSYWW**  
**M6604C**  
**LLLLLL**

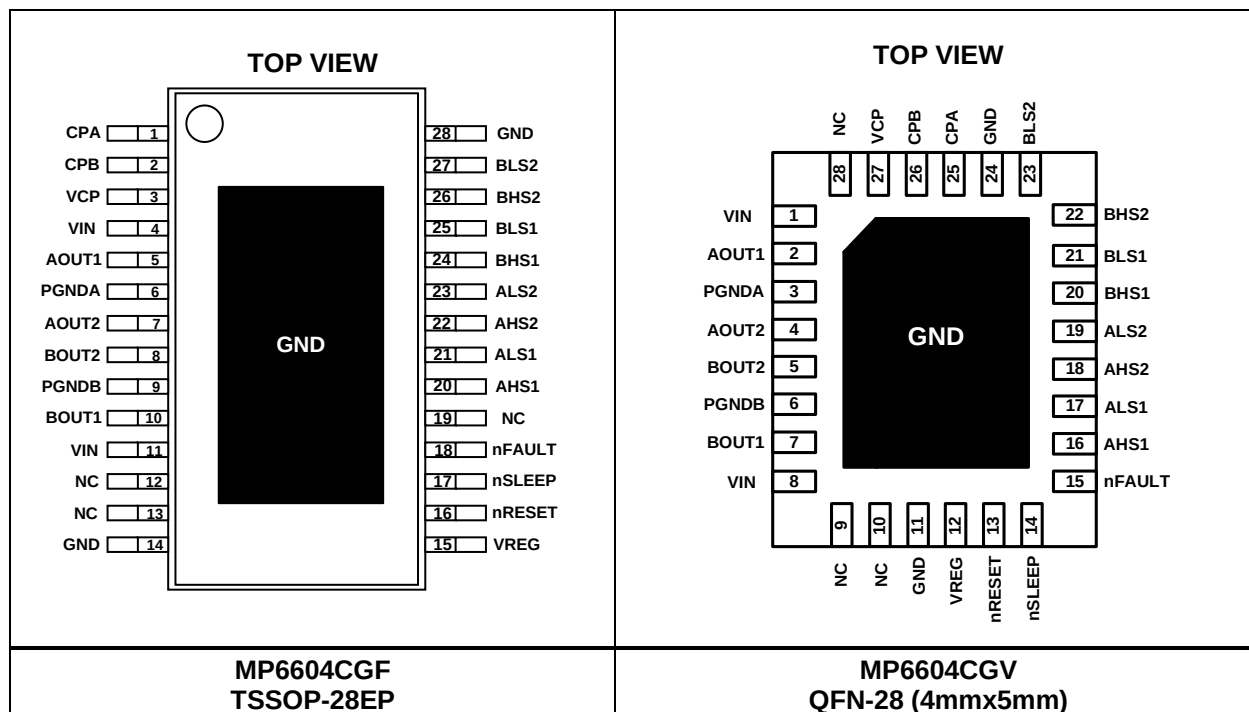
MPS: MPS prefix  
Y: Year code  
WW: Week code  
M6604C: Part number  
LLLLLL: Lot number

### TOP MARKING (MP6604CGF)

**MPSYYWW**  
**MP6604C**  
**LLLLLLLLLL**

MPS: MPS prefix  
YY: Year code  
WW: Week code  
MP6604C: Part number  
LLLLLLLLLL: Lot number

## PACKAGE REFERENCE



## PIN FUNCTIONS

| Pin #<br>(QFN-28) | Pin #<br>(TSSOP-28EP) | Name   | Description                                                                                                                                                                  |
|-------------------|-----------------------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1, 8              | 4, 11                 | VIN    | <b>Input supply voltage.</b> Decouple the VIN pin to ground using a minimum 100nF ceramic capacitor. Additional bulk capacitance may be required.                            |
| 2                 | 5                     | AOUT1  | <b>Bridge A output terminal 1.</b>                                                                                                                                           |
| 3                 | 6                     | PGNDA  | <b>Power ground for H-bridge A outputs.</b>                                                                                                                                  |
| 4                 | 7                     | AOUT2  | <b>Bridge A output terminal 2.</b>                                                                                                                                           |
| 5                 | 8                     | BOUT2  | <b>Bridge B output terminal 2.</b>                                                                                                                                           |
| 6                 | 9                     | PGNDB  | <b>Power ground for H-bridge B outputs.</b>                                                                                                                                  |
| 7                 | 10                    | BOUT1  | <b>Bridge B output terminal 1.</b>                                                                                                                                           |
| 11, 24            | 14, 28                | GND    | <b>Signal ground.</b>                                                                                                                                                        |
| 12                | 15                    | VREG   | <b>Internal regulator.</b> Connect a 1μF, 16V ceramic capacitor (X7R) to ground.                                                                                             |
| 13                | 16                    | nRESET | <b>Reset input.</b> Pull the nRESET pin active low to reset the protection circuits and disable the outputs. This pin is pulled down internally.                             |
| 14                | 17                    | nSLEEP | <b>Sleep mode input.</b> Pull the nSLEEP pin logic low to enter low-power sleep mode. This pin has an internal pull-down resistor.                                           |
| 15                | 18                    | nFAULT | <b>Fault indication.</b> The nFAULT pin is an open-drain output that pulls to logic low if a fault is detected. If nFAULT is used, it requires an external pull-up resistor. |
| 16                | 20                    | AHS1   | <b>AOUT1 high-side MOSFET (HS-FET) control input.</b> A high input turns on the AOUT1 HS-FET. AHS1 is pulled down internally.                                                |
| 17                | 21                    | ALS1   | <b>AOUT1 low-side MOSFET (LS-FET) control input.</b> A high input turns on the AOUT1 LS-FET. ALS1 is pulled down internally.                                                 |
| 18                | 22                    | AHS2   | <b>AOUT2 HS-FET control input.</b> A high input turns on the AOUT2 HS-FET. AHS2 is pulled down internally.                                                                   |
| 19                | 23                    | ALS2   | <b>AOUT2 LS-FET control input.</b> A high input turns on the AOUT2 LS-FET. ALS2 is pulled down internally.                                                                   |
| 20                | 24                    | BHS1   | <b>BOUT1 HS-FET control input.</b> A high input turns on the BOUT1 HS-FET. BHS1 is pulled down internally.                                                                   |
| 21                | 25                    | BLS1   | <b>BOUT1 LS-FET control input.</b> A high input turns on the BOUT1 LS-FET. BLS1 is pulled down internally.                                                                   |
| 22                | 26                    | BHS2   | <b>BOUT2 HS-FET control input.</b> A high input turns on the BOUT2 HS-FET. BHS2 is pulled down internally.                                                                   |
| 23                | 27                    | BLS2   | <b>BOUT2 LS-FET control input.</b> A high input turns on the BOUT2 LS-FET. BLS2 is pulled down internally.                                                                   |
| 25                | 1                     | CPA    | <b>Charge pump capacitor.</b> Connect a 100nF ceramic capacitor rated for the input voltage (VIN) between the CPA and CPB terminals.                                         |
| 26                | 2                     | CPB    |                                                                                                                                                                              |
| 27                | 3                     | VCP    | <b>Charge pump output.</b> The VCP pin requires a 1μF, 16V ceramic capacitor connected to VIN.                                                                               |

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

|                                                                         |                             |
|-------------------------------------------------------------------------|-----------------------------|
| Supply voltage ( $V_{IN}$ )                                             | -0.3V to +48V               |
| xOUTx voltage ( $V_{AOUT1}$ , $V_{AOUT2}$ , $V_{BOUT1}$ , $V_{BOUT2}$ ) | -0.7V to +48V               |
| VCP, CPB                                                                | $V_{IN}$ to $V_{IN} + 6.5V$ |
| PGNDx to GND                                                            | -0.3V to +0.3V              |
| All other pins to GND                                                   | -0.3V to +6.5V              |
| Continuous power dissipation ( $T_A = 25^\circ C$ ) <sup>(2)</sup>      |                             |
| QFN-28 (4mmx5mm)                                                        | 3.125W                      |
| TSSOP-28EP                                                              | 3.9W                        |
| Storage temperature                                                     | -55°C to +150°C             |
| Junction temperature                                                    | 150°C                       |
| Lead temperature (solder)                                               | 260°C                       |

## ESD Ratings

|                            |        |
|----------------------------|--------|
| Human body model (HBM)     | ±2000V |
| Charged device model (CDM) | ±2000V |

## Recommended Operating Conditions <sup>(3)</sup>

|                                   |                 |
|-----------------------------------|-----------------|
| Supply voltage ( $V_{IN}$ )       | 4.5V to 45V     |
| PGNDx to GND                      | -0.2V to +0.2V  |
| Operating junction temp ( $T_J$ ) | -40°C to +125°C |

## Thermal Resistance <sup>(4)</sup> $\theta_{JA}$ $\theta_{JC}$

|                  |    |   |    |
|------------------|----|---|----|
| QFN-28 (4mmx5mm) | 40 | 9 | °C |
| TSSOP-28EP       | 32 | 6 | °C |

### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature,  $T_J$  (MAX), the junction-to-ambient thermal resistance,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable continuous power dissipation at any ambient temperature is calculated by  $P_D$  (MAX) =  $(T_J$  (MAX) -  $T_A$ ) /  $\theta_{JA}$ . Exceeding the maximum allowable power dissipation can produce an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7, a 4-layer PCB.

## ELECTRICAL CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

| Parameter                                              | Symbol                 | Condition                            | Min  | Typ | Max  | Units       |
|--------------------------------------------------------|------------------------|--------------------------------------|------|-----|------|-------------|
| <b>Power Supply</b>                                    |                        |                                      |      |     |      |             |
| Input supply voltage                                   | $V_{IN}$               |                                      | 4.5  |     | 45   | V           |
| Quiescent current                                      | $I_{INQ}$              | nSLEEP = 1, with no load             |      | 2.8 |      | mA          |
|                                                        | $I_{INSLEEP}$          | nSLEEP = 0                           |      | 0.9 | 10   | $\mu A$     |
| <b>Internal MOSFETs</b>                                |                        |                                      |      |     |      |             |
| Output on resistance                                   | $R_{DS(ON)_HS}$        | $I_{OUT} = 1A$ , $T_J = 25^{\circ}C$ |      | 135 | 170  | m $\Omega$  |
|                                                        | $R_{DS(ON)_LS}$        | $I_{OUT} = 1A$ , $T_J = 25^{\circ}C$ |      | 150 | 185  | m $\Omega$  |
| Body diode forward voltage                             | $V_F$                  | $I_{OUT} = 1A$                       |      |     | 1.1  | V           |
| <b>Control Logic Inputs</b>                            |                        |                                      |      |     |      |             |
| Logic-low input threshold                              | $V_{IL}$               |                                      |      |     | 0.8  | V           |
| Logic-high input threshold                             | $V_{IH}$               |                                      | 2    |     |      | V           |
| Logic input current                                    | $I_{IN\_H}$            | $V_{IN} = 5V$                        | -100 |     | +100 | $\mu A$     |
|                                                        | $I_{IN\_L}$            | $V_{IN} = 0V$                        | -20  |     | +20  | $\mu A$     |
| Internal pull-down resistance                          | $R_{PD}$               | To GND                               |      | 100 |      | k $\Omega$  |
| <b>nFAULT Output</b>                                   |                        |                                      |      |     |      |             |
| Output low voltage                                     | $V_{OL}$               | $I_{OUT} = 5mA$                      |      |     | 0.5  | V           |
| Output high leakage current                            | $I_{OH}$               | $V_{OUT} = 5V$                       |      |     | 1    | $\mu A$     |
| <b>Protection Circuits</b>                             |                        |                                      |      |     |      |             |
| $V_{IN}$ under-voltage lockout (UVLO) rising threshold | $V_{IN\_UVLO\_RISING}$ |                                      |      |     | 4.5  | V           |
| $V_{IN}$ UVLO hysteresis                               | $V_{IN\_UVLO\_HYS}$    |                                      |      | 300 |      | mV          |
| $V_{IN}$ over-voltage protection (OVP) threshold       | $V_{OVP}$              |                                      | 45   |     | 48   | V           |
| Over-current (OC) trip level                           | $I_{OCP1}$             | Sinking                              | 3    | 4.5 |      | A           |
|                                                        | $I_{OCP2}$             | Sourcing                             | 3    | 4.5 |      | A           |
| OC deglitch time                                       | $t_{OCP}$              |                                      |      | 1   |      | $\mu s$     |
| Thermal shutdown                                       | $T_{TSD}$              |                                      |      | 165 |      | $^{\circ}C$ |
| Thermal shutdown hysteresis                            | $T_{TSD\_HYS}$         |                                      |      | 15  |      | $^{\circ}C$ |

## TYPICAL TIMING CHARACTERISTICS

$V_{IN} = 24V$ ,  $T_A = 25^{\circ}C$ , unless otherwise noted.

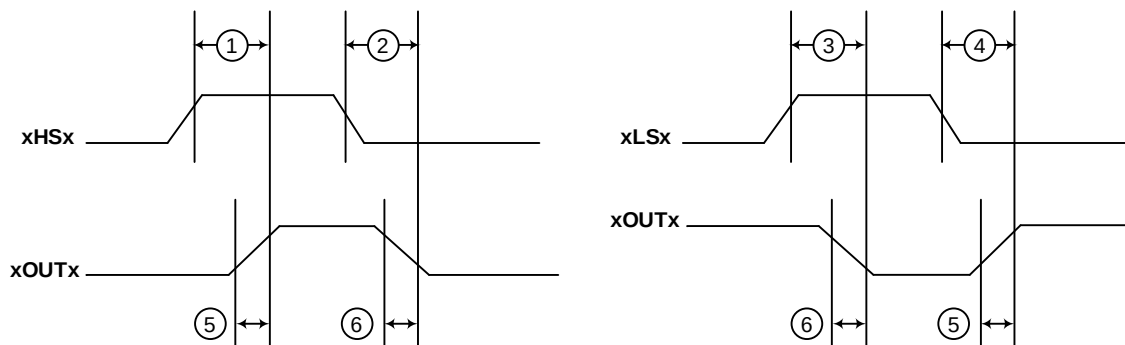


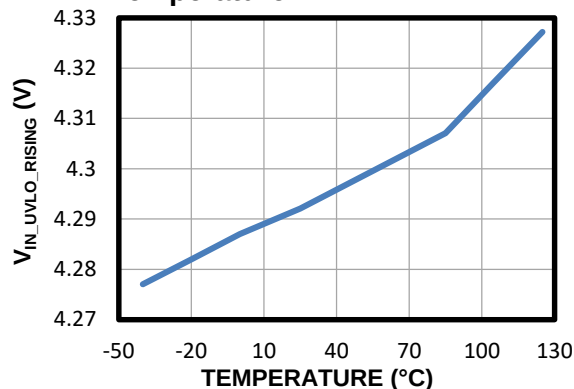
Figure 1: Timing Diagram

Table 1: Timing Characteristics

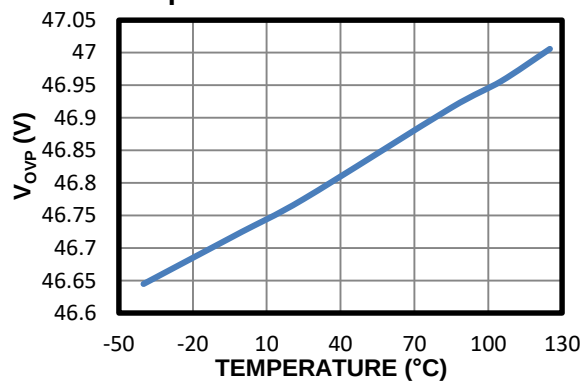
| Parameter                          | Symbol | Condition                             | Min | Typ | Max | Units |
|------------------------------------|--------|---------------------------------------|-----|-----|-----|-------|
| xHSx high to xOUTx high delay time | $t_1$  | 10mA load connected from xOUTx to GND | 40  |     | 360 | ns    |
| xHSx low to xOUTx low delay time   | $t_2$  |                                       | 40  |     | 360 | ns    |
| xLSx high to xOUTx low delay time  | $t_3$  | 10mA load connected from xOUTx to VIN | 40  |     | 360 | ns    |
| xLSx high to xOUTx high delay time | $t_4$  |                                       | 40  |     | 360 | ns    |
| Output rise time                   | $t_5$  | Resistive load                        | 1   |     | 55  | ns    |
| Output fall time                   | $t_6$  | Resistive load                        | 1   |     | 165 | ns    |
| Dead time                          | -      |                                       |     |     | 80  | ns    |

## TYPICAL CHARACTERISTICS

**$V_{IN}$  UVLO Rising Threshold vs. Temperature**

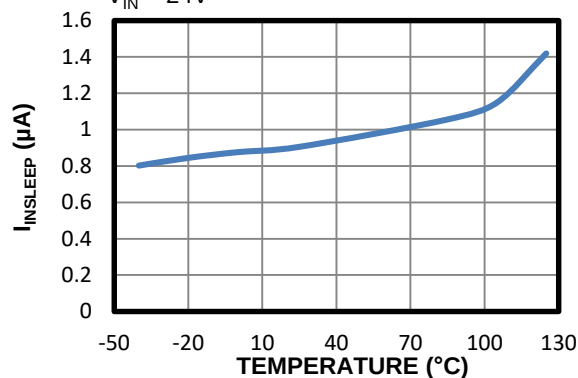


**$V_{IN}$  OVP Threshold vs. Temperature**



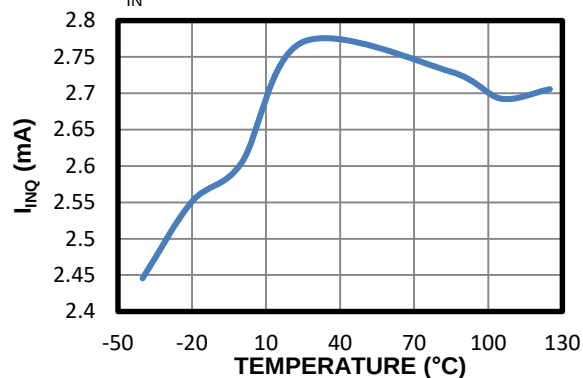
**Quiescent Current ( $I_{INSLEEP}$ ) vs. Temperature**

$V_{IN} = 24V$



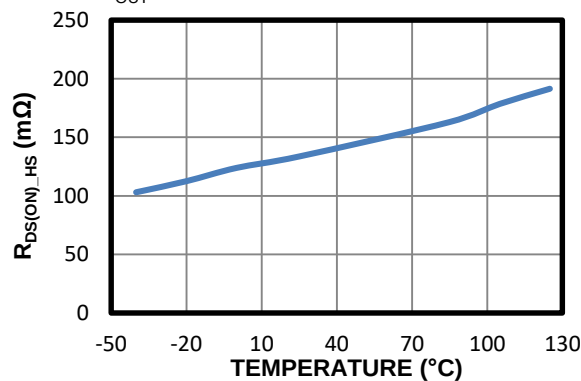
**Quiescent Current ( $I_{INQ}$ ) vs. Temperature**

$V_{IN} = 24V$



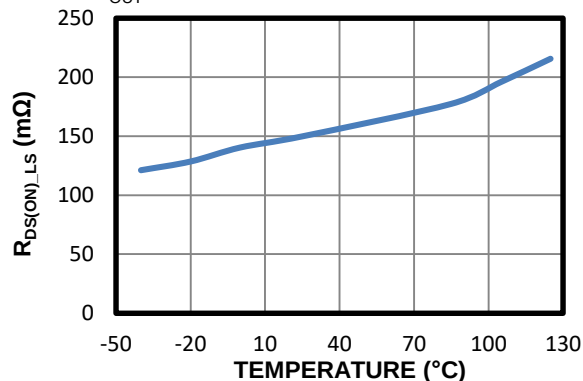
**HS-FET On Resistance vs. Temperature**

$I_{OUT} = 1A$

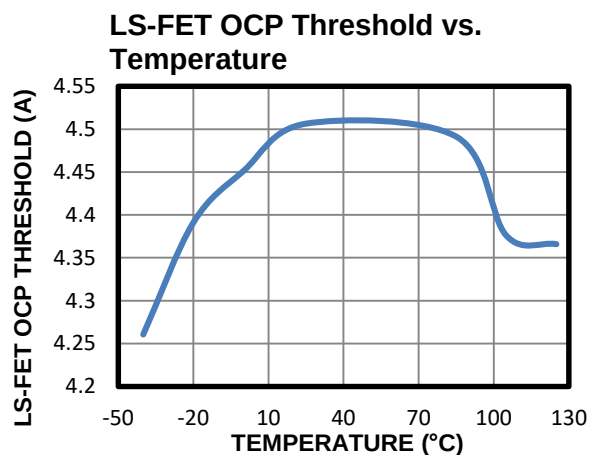
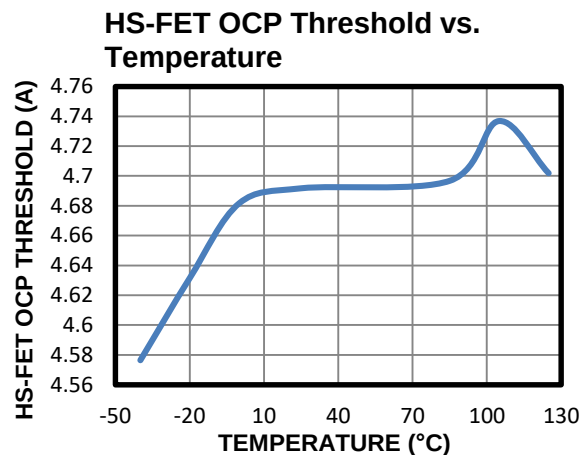


**LS-FET On Resistance vs. Temperature**

$I_{OUT} = 1A$



# TYPICAL CHARACTERISTICS *(continued)*



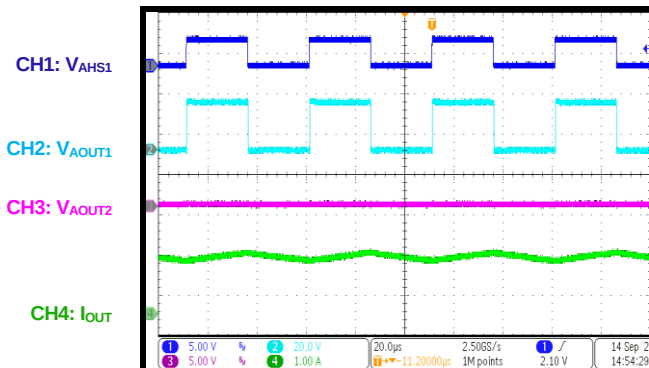


# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 24V$ ,  $nSLEEP = 3.3V$ , AOUT1 switching with 20kHz frequency, AOUT2 LS-FET on,  $T_A = 25^{\circ}C$ , resistor + inductor load:  $8\Omega + 1.5mH$  between AOUT1 and AOUT2, unless otherwise noted.

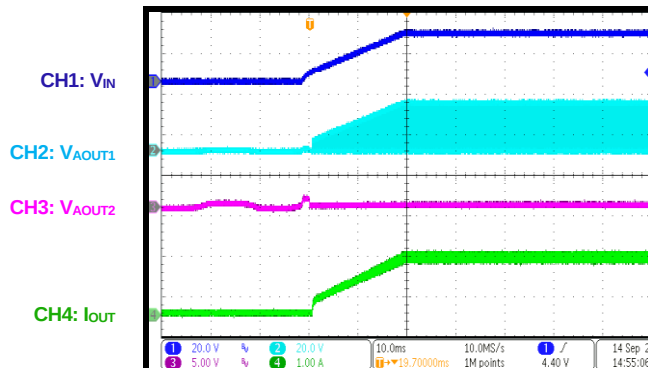
## Steady State

Duty = 50%



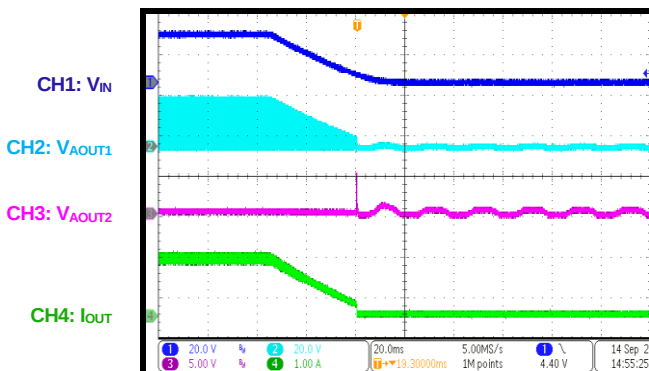
## Power Ramping Up

Duty = 50%



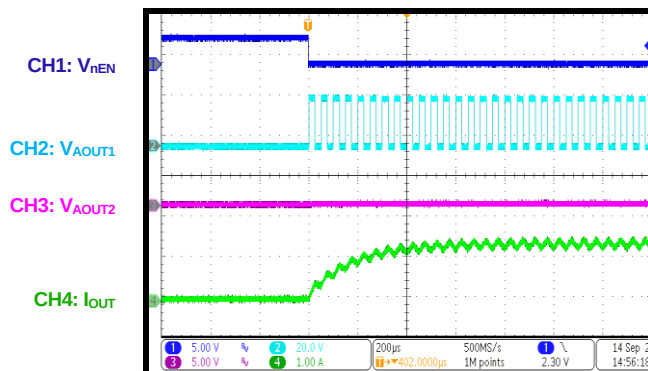
## Power Ramping Down

Duty = 50%



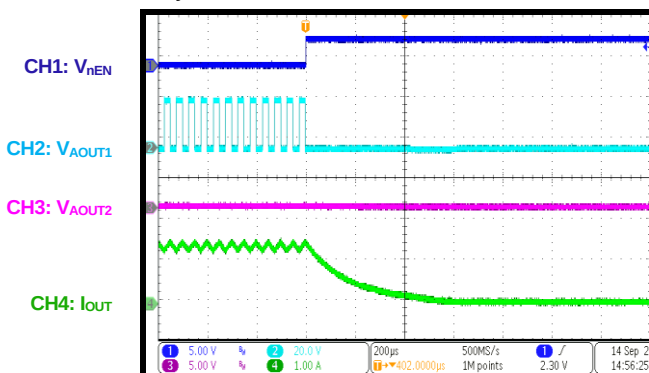
## Start-Up through nEN

Duty = 50%



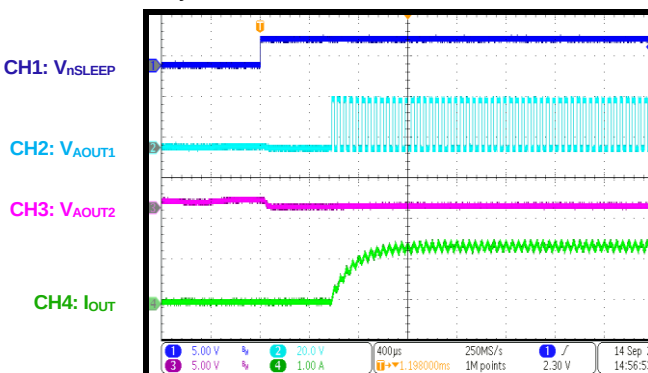
## Shutdown through nEN

Duty = 50%



## SLEEP Recovery

Duty = 50%

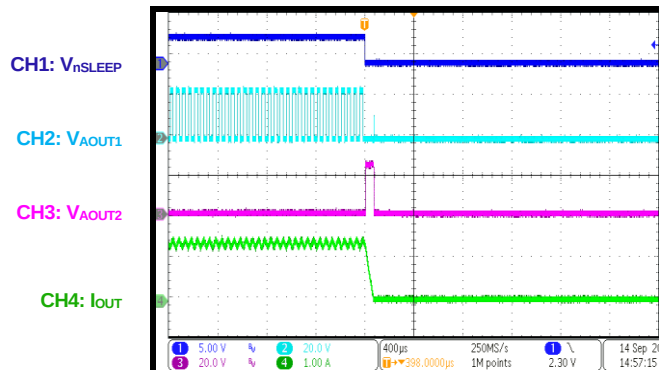


# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 24V$ ,  $nSLEEP = 3.3V$ , AOUT1 switching with 20kHz frequency, AOUT2 LS-FET on,  $T_A = 25^{\circ}C$ , resistor + inductor load:  $8\Omega + 1.5mH$  between AOUT1 and AOUT2, unless otherwise noted.

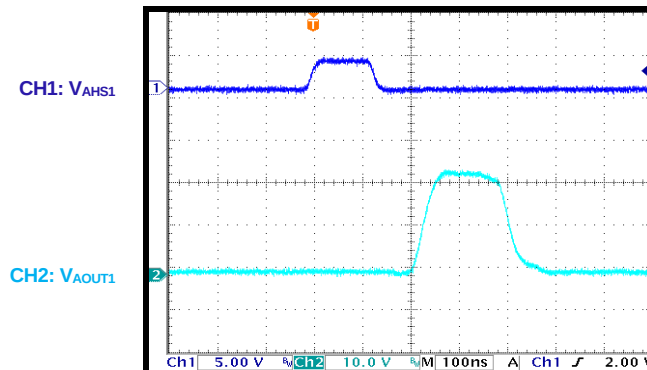
## SLEEP Entry

Duty = 50%



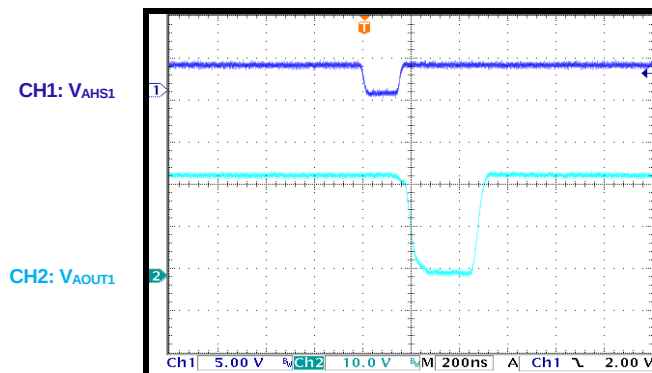
## HS-FET Minimum On Time

No load



## LS-FET Minimum On Time

No load



## FUNCTIONAL BLOCK DIAGRAM

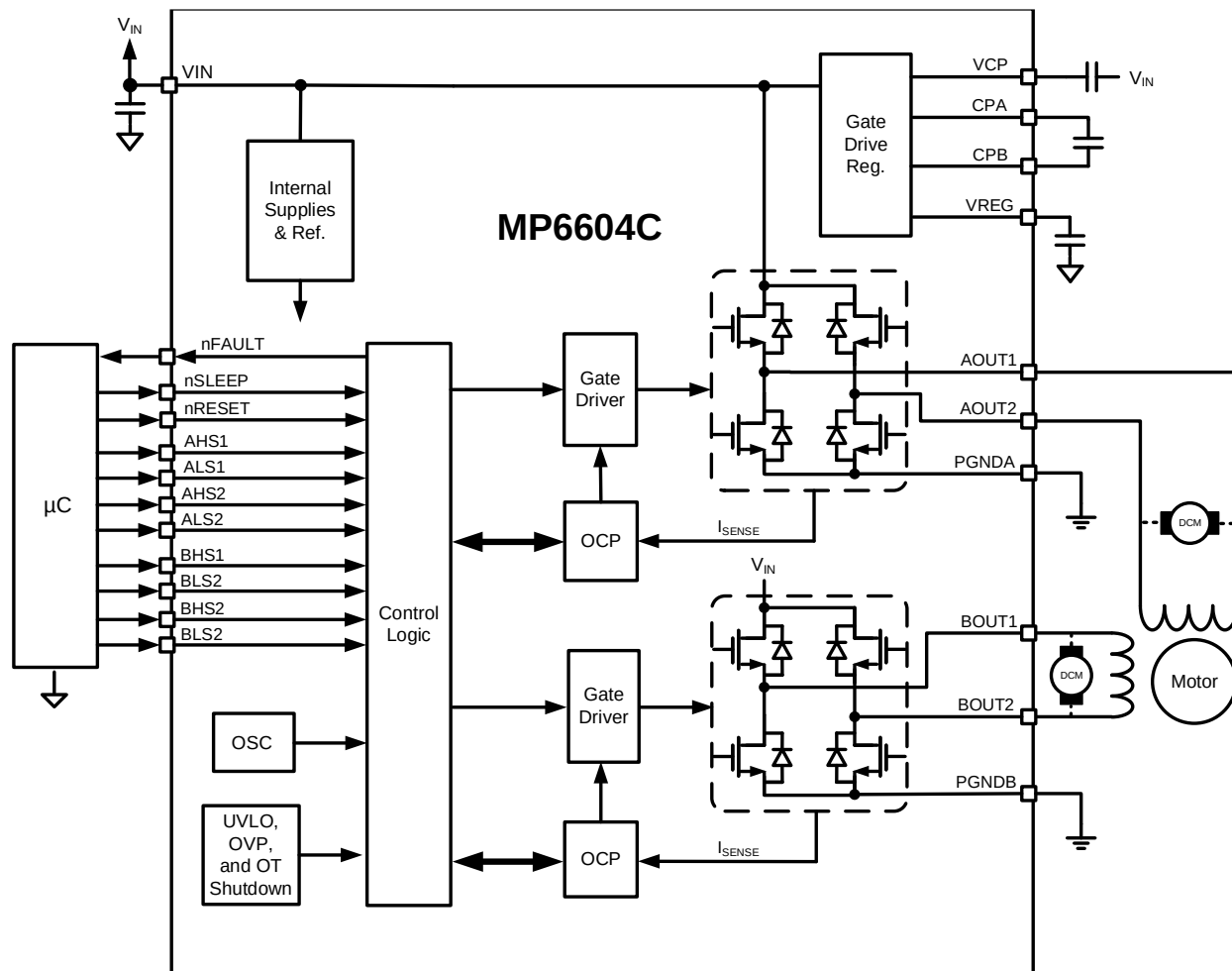


Figure 2: Functional Block Diagram

## OPERATION

The MP6604C is a general-purpose dual H-bridge motor driver designed to drive bipolar stepper motors, brushed DC motors, solenoids, and other loads. It integrates eight N-channel power MOSFETs connected as four half H-bridges, with a 2.5A current capability. The device operates across a wide 4.5V to 45V supply input voltage ( $V_{IN}$ ) range.

### nSLEEP and nRESET

Pull the nSLEEP pin low to force the MP6604C to enter low-power sleep mode. In this mode, the gate drive charge pump stops, and all the internal circuits and H-bridge outputs are disabled. All inputs are ignored when nSLEEP is active low.

When waking up from sleep mode, approximately 600 $\mu$ s must pass before driving the motor. This allows the internal circuitry to stabilize. nSLEEP has an internal pull-down resistor.

Pull the nRESET pin low to reset the latched protection features, including over-current protection (OCP) and over-voltage protection (OVP), as well as to disable the outputs to a high-impedance (Hi-Z) state.

### Input Interface

The MP6604C contains four half H-bridges that operate independently.

The MP6604C has high-side (HS) and low-side (LS) inputs for each of the output pins. Table 2 shows the input logic.

**Table 2: HS and LS Input Logic**

| xHSx | xLSx | xOUTx |
|------|------|-------|
| 0    | 0    | Hi-Z  |
| 0    | 1    | L     |
| 1    | 0    | H     |
| 1    | 1    | Hi-Z  |

Note that all logic inputs have weak, internal pull-down resistors.

### Automatic Synchronous Rectification

If the output high-side MOSFET (HS-FET) and low-side MOSFET (LS-FET) are turned off, then the recirculation current must continue to flow when driving current through an inductive load. This current is typically passed through the MOSFET body diodes. To prevent excess power dissipation in the body diodes, the MP6604C implements automatic synchronous rectification.

If both the HS-FET and LS-FET are turned off, and the voltage on an xOUTx pin ( $V_{xOUTx}$ ) is pulled below ground, then the corresponding LS-FET turns on until the current flowing through it approaches 0A, or the HS-FET turns on. Similarly, if  $V_{xOUTx}$  exceeds  $V_{IN}$ , then the corresponding HS-FET turns on until the current approaches 0A, or the LS-FET turns on.

### Internal Supply Voltages ( $V_{REG}$ and $V_{CP}$ )

The internal regulators generate a 5V supply voltage ( $V_{REG}$ ) for the LS gate drive, and a supply exceeding  $V_{IN}$  by 5V ( $V_{CP}$ ) for the HS gate drive. These supplies require external capacitors.

The VREG pin requires a 1 $\mu$ F ceramic capacitor connected to ground. The VCP pin requires a 1 $\mu$ F ceramic capacitor connected to  $V_{IN}$ . Both capacitors should be X7R ceramic capacitors, and rated for a voltage of at least 16V.

Connect the charge pump flying capacitor between the CPA and CPB pins using a 100nF ceramic capacitor (X7R) that is rated for at least the maximum  $V_{IN}$ .

### nFAULT

The MP6604C provides a nFAULT pin to report to the system if a fault condition such as OCP, OVP, or over-temperature protection (OTP) occur. nFAULT is an open-drain output, and is pulled low during fault conditions. If used, nFAULT should be pulled high via an external pull-up resistor.

### Over-Current Protection (OCP)

OCP circuitry limits the current through the HS-FET and LS-FET by disabling the gate driver. If the over-current (OC) limit threshold is reached and lasts for longer than the OC deglitch time ( $t_{OCP}$ ), then all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. The driver remains disabled until the device is reset by pulling nRESET low or by cycling the power on the MP6604C.

OC conditions on the HS and LS devices (e.g. an OC condition to ground, supply, or across a motor winding) all result in an OC shutdown.

### Over-Voltage Protection (OVP)

If  $V_{IN}$  exceeds the OVP threshold ( $V_{OVP}$ ), then the H-bridge output is disabled and nFAULT is pulled low. The driver remains disabled until the

device is reset by pulling nRESET low or cycling the power on the MP6604C.

### Input Under-Voltage Lockout (UVLO) Protection

If  $V_{IN}$  falls below the under-voltage lockout (UVLO) threshold ( $V_{IN\_UVLO}$ ), then all circuitry in the device is disabled and the internal logic resets. Once  $V_{IN}$  exceeds  $V_{IN\_UVLO}$ , the device starts up again and resumes normal operation.

### Thermal Shutdown

If the die temperature exceeds safe limits, all the MOSFETs in the H-bridge are disabled and nFAULT is pulled low. Once the die temperature returns to a safe level, the MP6604C automatically starts up again and resumes normal operation.

## APPLICATION INFORMATION

### Selecting the External Components

Bypass the two VIN pins to GND using a minimum 100nF ceramic capacitor with X7R dielectrics, placed as close to the IC as possible. Place an additional 1μF to 10μF ceramic capacitor close to the 100nF capacitor. Depending on the supply impedance and distance to other large capacitors, an electrolytic bulk capacitor may also be required to stabilize VIN.

Connect a 100nF ceramic capacitor rated for  $V_{IN}$  between the CPA and CPB pins. Connect a 1μF, 16V ceramic capacitor between the VIN and VCP pins.

Connect a 1μF, 16V ceramic capacitor with X7R dielectrics from the VREG pin to GND.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 3 and Figure 4, and follow the guidelines below:

1. Place the supply bypass and charge pump capacitors as close to the IC as possible ideally adjacent to the pins on the same PCB layer.
2. Each VIN pin requires a bypass capacitor.
3. Place as much copper on the long pads as possible.
4. Place large copper areas on the pads and the device's outer copper layer.
5. The thermal pad should be soldered directly to the copper on the PCB.
6. Add thermal vias to transfer heat to the other PCB layers.

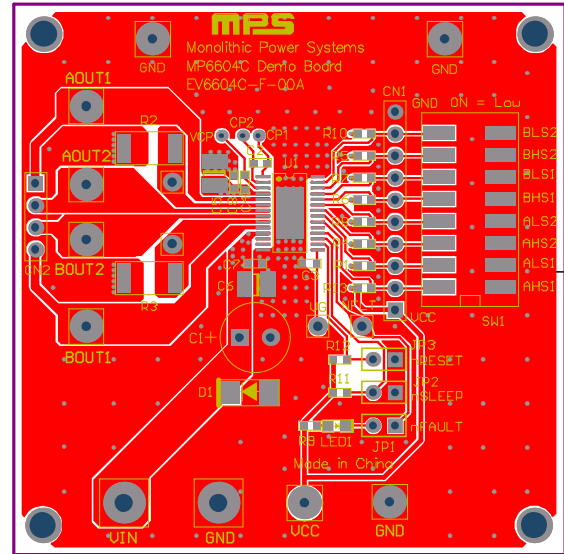


Figure 3: Recommended PCB Layout (MP6604CGF)

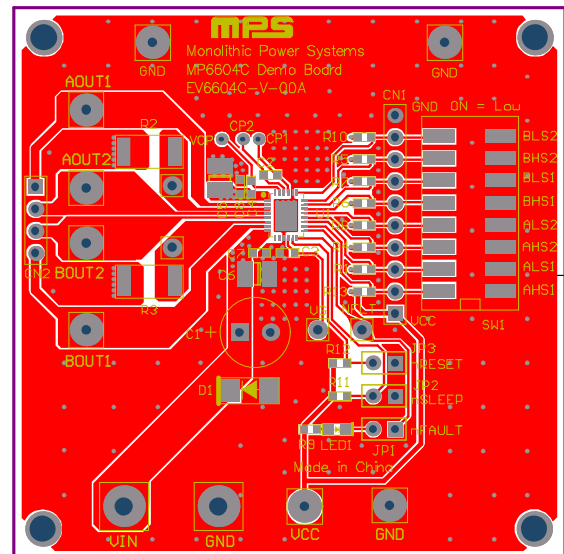


Figure 4: Recommended PCB Layout (MP6604CGV)

## TYPICAL APPLICATION CIRCUIT

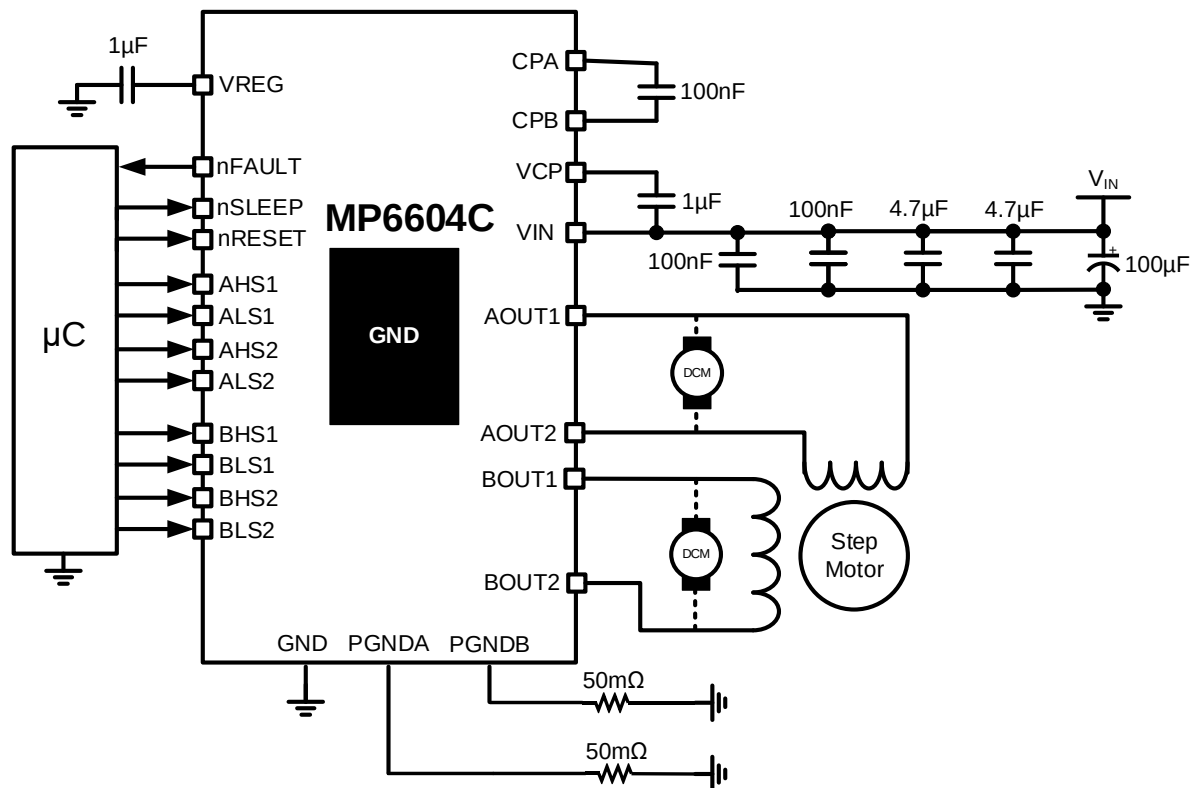
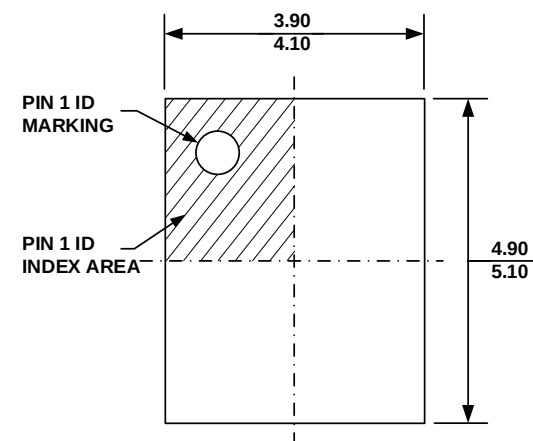


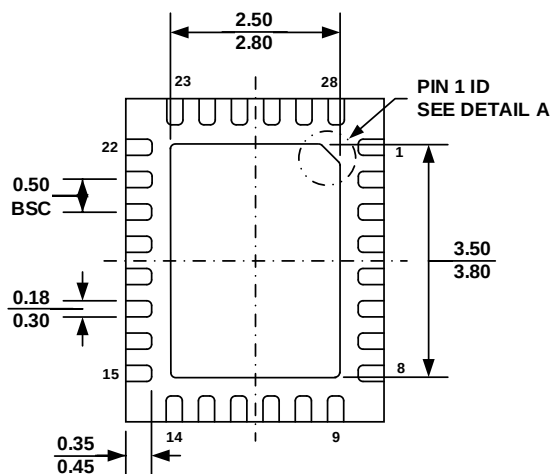
Figure 5: Typical Application Circuit

## PACKAGE INFORMATION

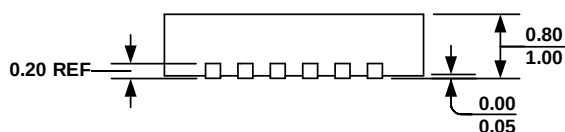
### QFN-28 (4mmx5mm)



**TOP VIEW**

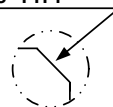


**BOTTOM VIEW**

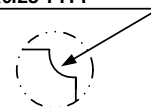


### SIDE VIEW

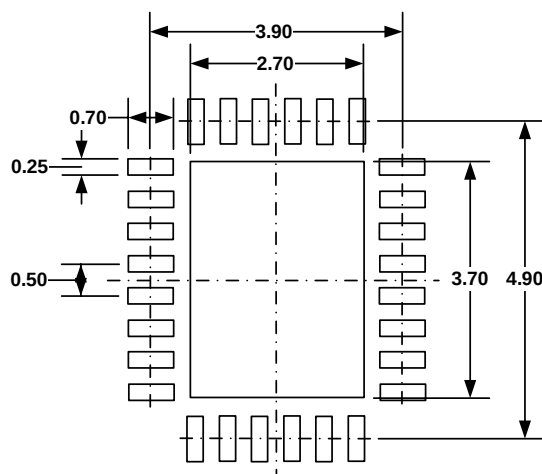
**PIN 1 ID OPTION A**  
**0.30x45° TYP.**



**PIN 1 ID OPTION B  
R0.25 TYP.**



**DETAIL A**



### RECOMMENDED LAND PATTERN

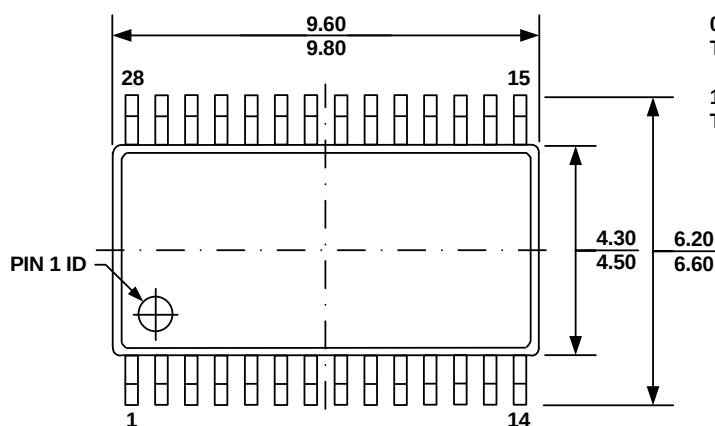
**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
- 5) DRAWING IS NOT TO SCALE.

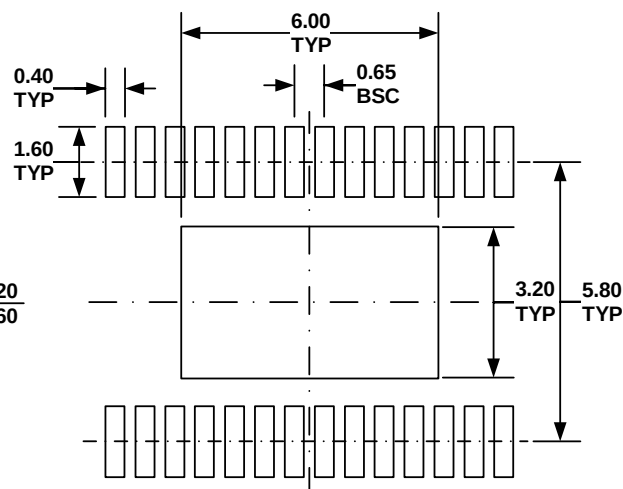


# PACKAGE INFORMATION (continued)

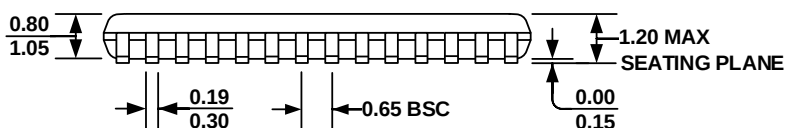
## TSSOP-28EP



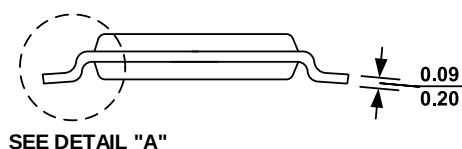
**TOP VIEW**



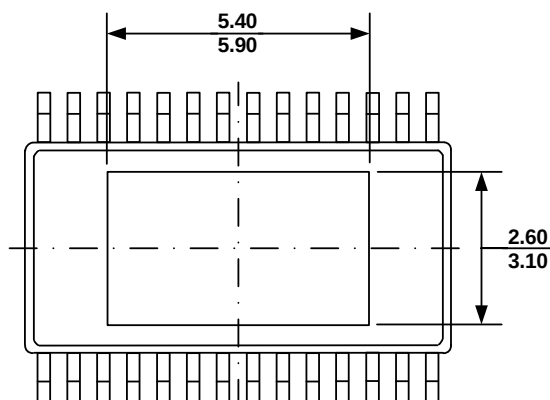
**RECOMMENDED LAND PATTERN**



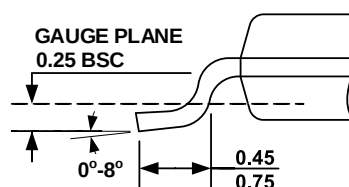
**FRONT VIEW**



**SIDE VIEW**



**BOTTOM VIEW**

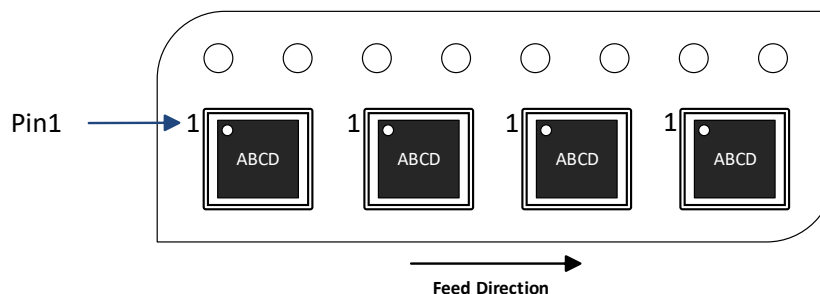
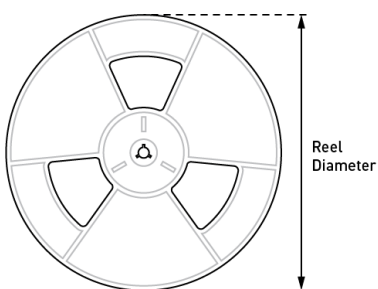


**DETAIL "A"**

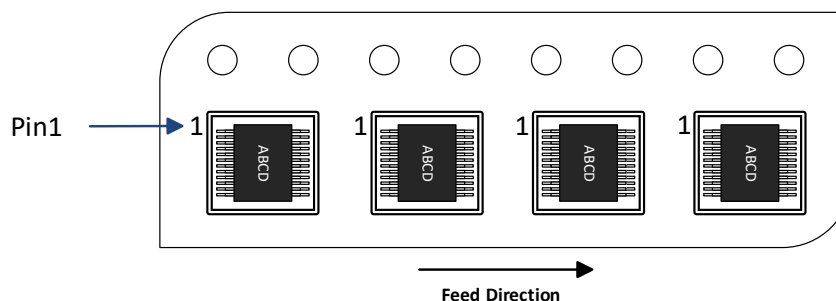
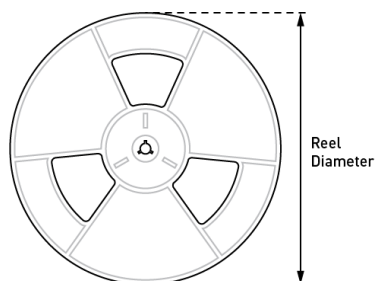
### NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
- 5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
- 6) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION



| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|----------------|----------------|---------------|--------------------|--------------------|
| MP6604CGV-Z | QFN-28 (4mmx5mm)    | 5000           | N/A            | 13in          | 12mm               | 8mm                |



| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|-------------|---------------------|----------------|----------------|---------------|--------------------|--------------------|
| MP6604CGF-Z | TSSOP-28EP          | 2500           | 50             | 13in          | 16mm               | 8mm                |

## REVISION HISTORY

| Revision # | Revision Date | Description                                                                                      | Pages Updated |
|------------|---------------|--------------------------------------------------------------------------------------------------|---------------|
| 1.0        | 12/8/2022     | Initial Release                                                                                  | -             |
| 1.1        | 5/12/2023     | Updated the MSL Rating of the MP6604CGV orderable SKU to “2” in the Ordering Information section | 2             |

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