MPQ4436A

45V, 6A, Low-I_Q, Fixed-Output, Synchronous Step-Down Converter, AEC-Q100 Qualified

DESCRIPTION

The MPQ4436A is a configurable-frequency, synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides up to 6A of highly efficient output current (I_{OUT}), with current mode control for fast loop response.

The wide 3.3V to 45V input voltage (V_{IN}) range accommodates a variety of step-down applications in automotive input environments. A 1.7µA shutdown mode quiescent current (I_Q) allows the part to be used in battery-powered applications.

High power conversion efficiency across a wide load range is achieved by scaling down the switching frequency (f_{SW}) under light-load conditions to reduce the switching and gate driver losses.

An open-drain power good (PG) signal indicates whether the output is within 95% to 105% of its nominal voltage.

Frequency foldback helps prevent inductor current runaway during start-up. Thermal shutdown provides reliable, fault-tolerant operation. High duty cycle and low-dropout mode are provided for automotive cold-crank conditions.

The MPQ4436A is available in a QFN-20 (4mmx4mm) package.

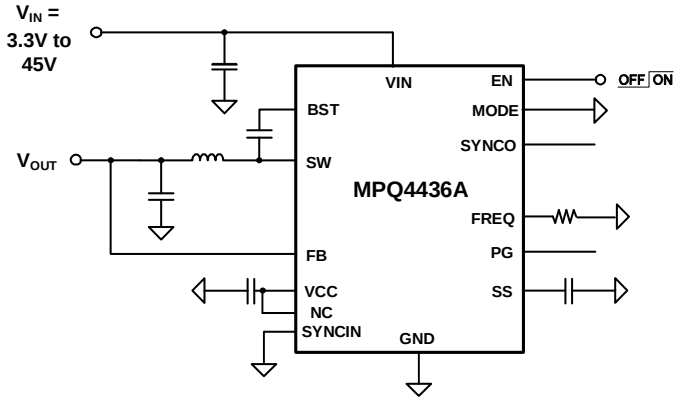
FEATURES

- Wide 3.3V to 45V Operating Input Voltage (V_{IN}) Range
- 6A Continuous Output Current (I_{OUT})
- 1.7µA Low Shutdown Supply Current
- 18µA Sleep Mode Quiescent Current (I_Q)
- Internal 48mΩ High-Side MOSFET (HS-FET) and 20mΩ Low-Side MOSFET (LS-FET)
- 350kHz to 1000kHz Configurable Switching Frequency (f_{SW}) for V_{OUT} < 5V Car Battery Applications
- Synchronizable to an External Clock
- Out-of-Phase Synchronized Clock Output
- Fixed Output Version: 3.3V, 5V
- Frequency Spread Spectrum (FSS) for Low EMI
- Symmetric V_{IN} for Low EMI
- Power Good (PG) Output
- External Soft Start (SS)
- 100ns Minimum On Time
- Selectable Advanced Asynchronous Modulation (AAM) Mode or Forced Continuous Conduction Mode (FCCM)
- Low-Dropout Mode
- Hiccup Over-Current Protection (OCP)
- Available in a QFN-20 (4mmx4mm) Package
- Available in a Wettable Flank Package
- Available in AEC-Q100 Grade 1

APPLICATIONS

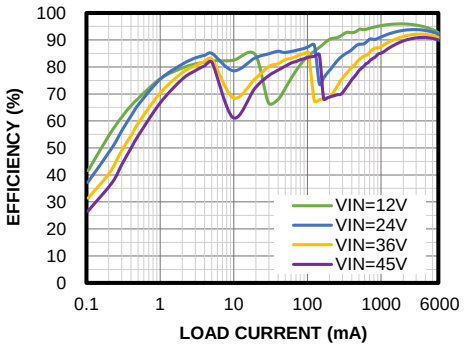
- Automotive Infotainment
- Automotive Clusters
- Advanced Driver Assistance Systems (ADAS)
- Industrial Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, f_{SW} = 470kHz, L = 4.7µH
(DCR = 15mΩ), AAM mode



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MPQ4436AGRE-33-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1
MPQ4436AGRE-5-AEC1***	QFN-20 (4mmx4mm)	*See Below*	1

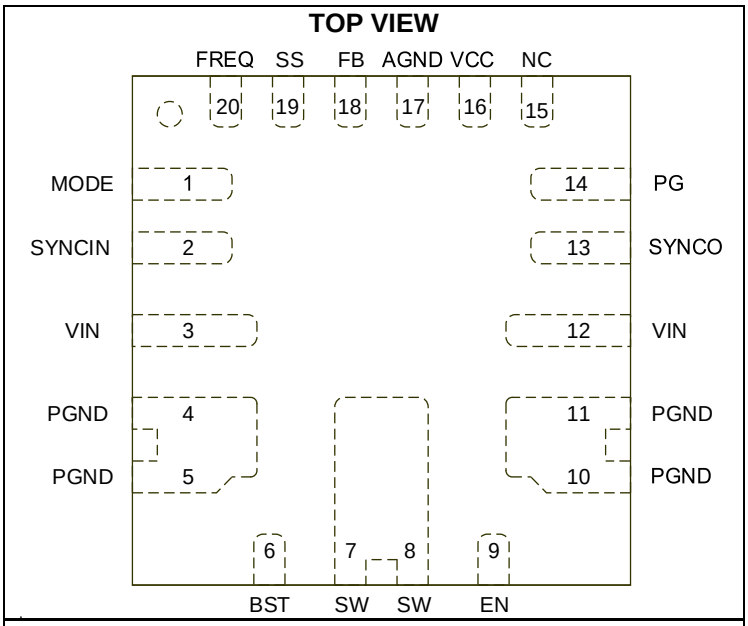
* For Tape & Reel, add suffix -Z (e.g. MPQ4436GRE-33-AEC1-Z).
**Moisture Sensitivity Level Rating
***Wettable flank

TOP MARKING

MPSYWW
MP4436
LLLLLL
E

MPS: MPS prefix
Y: Year code
WW: Week code
MP4436: Part number
LLLLLL: Lot number
E: Wettable flank

PACKAGE REFERENCE



QFN-20 (4mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1	MODE	**AAM or FCCM selection pin.** Pull this pin high to put the part in forced continuous conduction mode (FCCM). Pull it low to make the part operate in advanced asynchronous modulation (AAM) mode under light loads. Do not leave this pin floating.
2	SYNCIN	**SYNC input.** Connect a 51kΩ resister between SYNCIN and GND. Apply a 350kHz to 1000kHz clock signal to this pin to synchronize the internal oscillator frequency to the external clock. Connect this pin to GND if not used; do not float this pin.
3, 12	VIN	**Input supply.** VIN supplies power to all of the internal control circuitry and the power MOSFET connected to SW. It is recommended to place a decoupling capacitor to ground close to VIN to minimize switching spikes.
4, 5, 10, 11	PGND	**Power ground.**
6	BST	**Bootstrap.** BST is the positive power supply for the high-side MOSFET (HS-FET) driver connected to SW. Connect a bypass capacitor between BST and SW. See the Application Information section on page 32 to calculate the size of this capacitor.
7, 8	SW	**Switch node.** SW is the output of the internal power MOSFET.
9	EN	**Enable.** Pull this pin below 0.85V to shut down the chip. Pull it above 1V to enable the chip.
13	SYNCO	**SYNC output.** This pin outputs a clock signal that is 180° out of phase with the internal oscillator signal, or 180° out of phase with the clock signal applied at SYNCIN pin. Leave this pin floating if not used.
14	PG	**Power good (PG) indicator.** PG's output is an open drain. A pull-up resistor connected to the power source is required if PG is used. If the output voltage (V_{OUT}) is within 95% to 105% of the nominal voltage, this pin goes high. If V_{OUT} is above 106.5% or below 93.5% of the nominal voltage, this pin goes low.
15	NC	**Not connected.** Connect this pin to the VCC pin or V_{OUT}, which must be no less than 3V. Do not float this pin.
16	VCC	**Bias supply.** This supplies power to the internal control circuit and gate drivers. A decoupling capacitor to ground is required close to this pin. See the Application Information section on page 32 to calculate the size of this capacitor.
17	AGND	**Analog ground.**
18	FB	**Feedback input.** Connect the FB pin directly to the output. Avoid placing vias on the FB traces.
19	SS	**Soft start (SS) input.** Place a capacitor from SS to GND to set the soft-start time (t_{SS}). The MPQ4436A sources 6µA from SS to the soft-start capacitor (C_{SS}) at start-up. As the SS voltage (V_{SS}) rises, the feedback threshold voltage increases to limit inrush current during start-up.
20	FREQ	**Switching frequency setting.** Connect a resistor from this pin to GND to set the switching frequency (f_{SW}). See the f_{SW} vs. R_{FREQ} curve in the Typical Performance Characteristics section on page 15 to set the frequency.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN}, EN ..... -0.3V to +50V
SW ..... -0.3V to $V_{IN\ (MAX)}$ + 0.3V
BST ..... V_{SW} + 5.5V
All other pins ..... -0.3V to +5.5V
Continuous power dissipation (T_A = 25°C) (2) (4)
QFN-20 (4mmx4mm) 2.84W
Operating junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±750V

Recommended Operating Conditions

Supply voltage (V_{IN}) ..... 3.3V to 45V
Operating junction temp (T_J) .... -40°C to +150°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (4mmx4mm)		
JESD51-7 (3)	44	9 °C/W
EVQ4436A-R-00A (4)	23	2.5 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.
4) Measured on an MPS standard EVB: 9cmx9cm, 2oz copper thickness, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
V_{IN} under-voltage lockout (UVLO) rising threshold	$V_{IN\_UVLO\_RISING}$		2.8	3	3.2	V
V_{IN} UVLO falling threshold	$V_{IN\_UVLO\_FALLING}$		2.5	2.7	2.9	V
V_{IN} UVLO hysteresis	$V_{IN\_UVLO\_HYS}$			280		mV
VCC voltage	V_{CC}	I_{VCC} = 0A	4.6	4.9	5.2	V
VCC regulation		I_{VCC} = 30mA		1	4	%
VCC current limit	I_{LIMIT_VCC}	V_{CC} = 4V	100			mA
V_{IN} quiescent current	I_Q	FB high, no load, (sleep mode)		18	26	µA
V_{IN} quiescent current (switching) (5)	I_{Q_ACTIVE}	MODE = GND (AAM), switching, no load,		20		µA
		MODE = high (FCCM), switching, f_{SW} = 2MHz, no load		40		mA
		MODE = high (FCCM), switching, f_{SW} = 470kHz, no load		9.5		mA
V_{IN} shutdown current	I_{SHDN}	EN = 0V		1.7	2.5	µA
Output voltage accuracy of the MPQ4436A-33	V_{OUT}	T_J = 25°C	3234	3300	3366	mV
			3201	3300	3399	
Output voltage accuracy of the MPQ4436A-5	V_{OUT}	T_J = 25°C	4900	5000	5100	mV
			4850	5000	5150	
Switching frequency	f_{SW}	R_{FREQ} = 62kΩ	420	470	520	kHz
		R_{FREQ} = 26.1kΩ	820	1000	1180	
Minimum on time (5)	t_{ON_MIN}			100		ns
Minimum off time (5)	t_{OFF_MIN}			80		ns
SYNCIN voltage rising threshold	V_{SYNC_RISING}		1.8			V
SYNCIN voltage falling threshold	$V_{SYNC\_FALLING}$				0.4	V
SYNCIN clock range	f_{SYNC}	External clock	350		1000	kHz
SYNCO high voltage	V_{SYNCO_HIGH}	I_{SYNCO} = -1mA	3.3	4.5		V
SYNCO low voltage	V_{SYNCO_LOW}	I_{SYNCO} = 1mA			0.4	V
SYNCO phase shift		Tested under SYNCIN		180		deg
High-side (HS) current limit	I_{LIMIT}	Duty cycle = 30%	10	13	16	A
Low-side (LS) valley current limit	I_{LIMIT_VALLEY}		8	10	12	A
ZCD current	I_{ZCD}	AAM mode	-0.15	0.1	0.35	A
LS reverse current limit	$I_{LIMIT\_REVERSE}$	FCCM	2	4.5	6.5	A
Switch leakage current	I_{SW_LKG}			0.01	1	µA
High-side MOSFET (HS-FET) on resistance	$R_{DS(ON)\_HS}$	V_{BST} - V_{SW} = 5V		48	80	mΩ
Low-side MOSFET (LS-FET) on resistance	$R_{DS(ON)\_LS}$	V_{CC} = 5V		20	40	mΩ
Soft-start current	I_{SS}	V_{SS} = 0V	4	6	8	µA

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 2V, T_J = -40°C to +125°C, typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
EN rising threshold	V_{EN_RISING}		0.8	1	1.2	V
EN falling threshold	$V_{EN\_FALLING}$		0.65	0.85	1.05	V
EN hysteresis voltage	V_{EN_HYS}			180		mV
MODE rising threshold	V_{MODE_RISING}		1.8			V
MODE falling threshold	$V_{MODE\_FALLING}$				0.4	V
PG rising threshold (V_{FB} / V_{OUT})	PG_{RISING}	V_{FB} rising	92%	95%	98%	V_{OUT}
		V_{FB} falling	102%	105%	108%	
PG falling threshold (V_{FB} / V_{OUT})	$PG_{FALLING}$	V_{FB} falling	90.5%	93.5%	96.5%	
		V_{FB} rising	103.5%	106.5%	109.5%	
PG output voltage low	V_{PG_LOW}	I_{SINK} = 1mA		0.1	0.3	V
PG rising delay	$t_{PG\_R\_DELAY}$			35		µs
PG falling delay	$t_{PG\_F\_DELAY}$			35		µs
Thermal shutdown (5)	t_{SD}			170		°C
Thermal shutdown hysteresis (5)	t_{SD_HYS}			20		°C

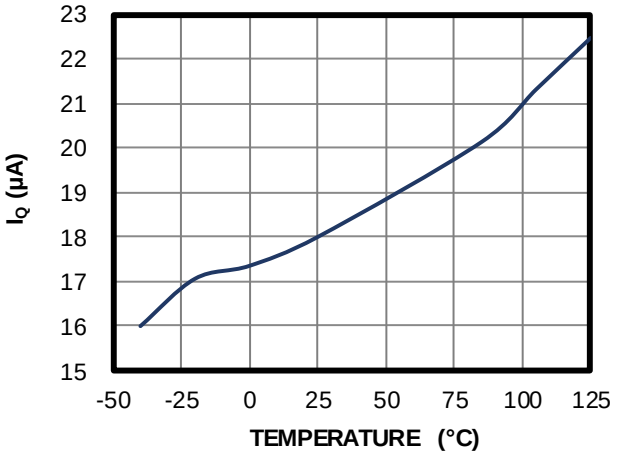
Note:

5) Derived from bench characterization, not tested in production.

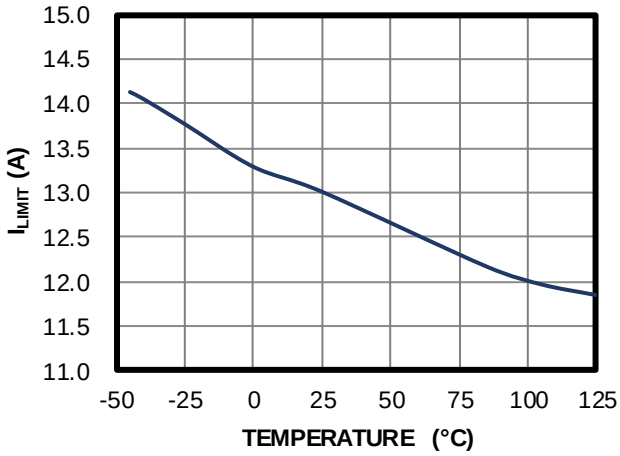
TYPICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

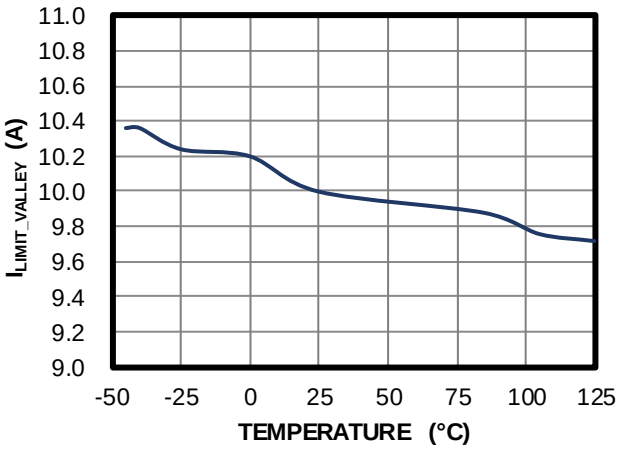
I_Q vs. Temperature



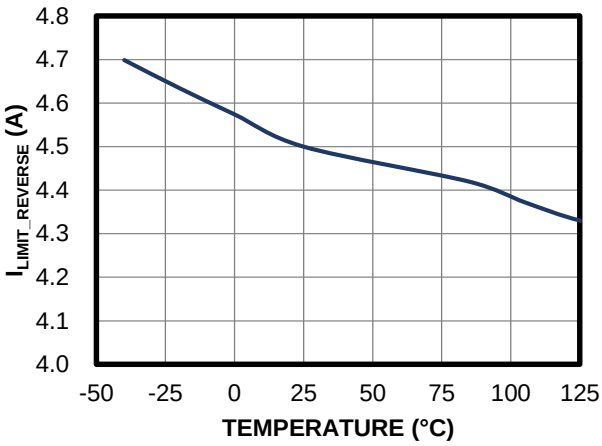
I_{LIMIT} vs. Temperature



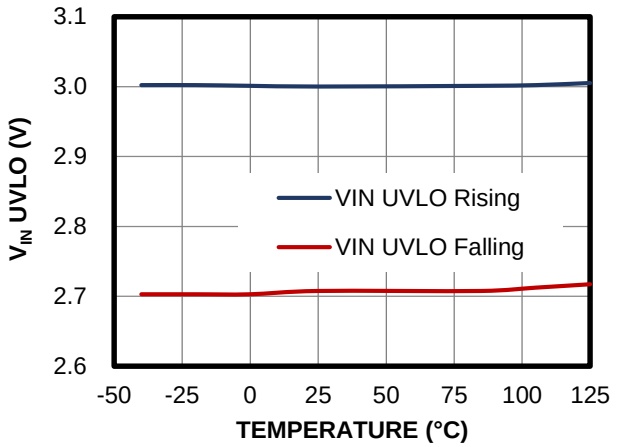
Valley Current Limit vs. Temperature



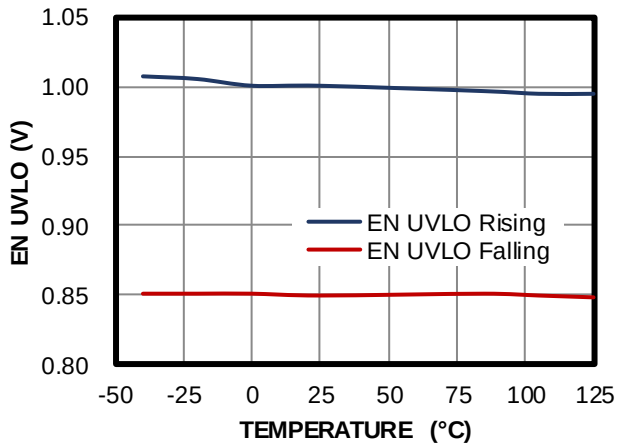
Reverse Current Limit vs. Temperature



V_{IN} UVLO Threshold vs. Temperature



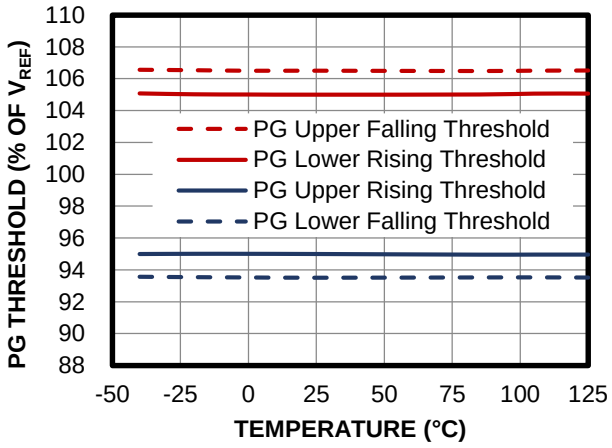
EN UVLO Threshold vs. Temperature



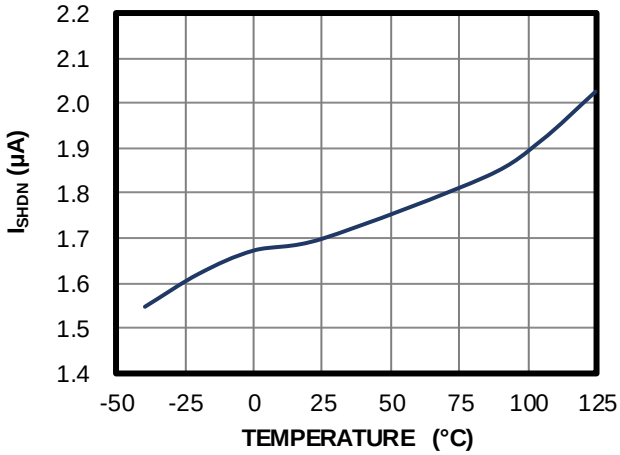
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

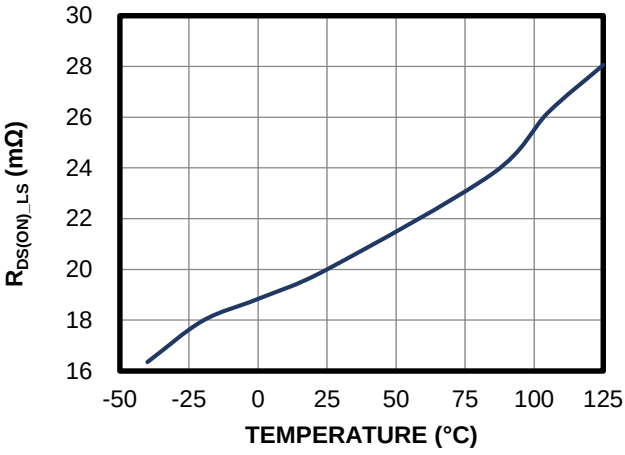
PG Rising/Falling Threshold vs. Temperature



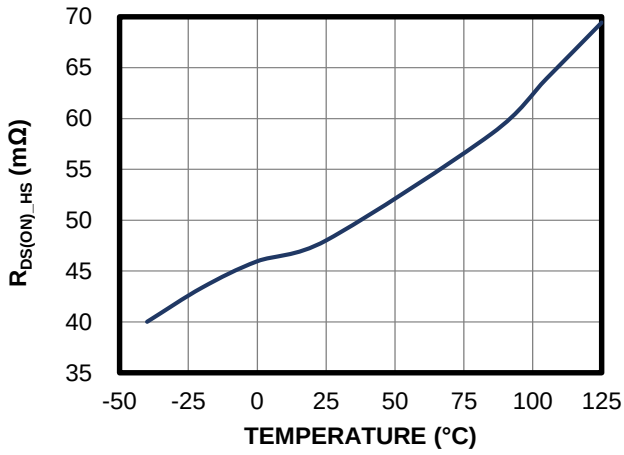
V_{IN} Shutdown Current vs. Temperature



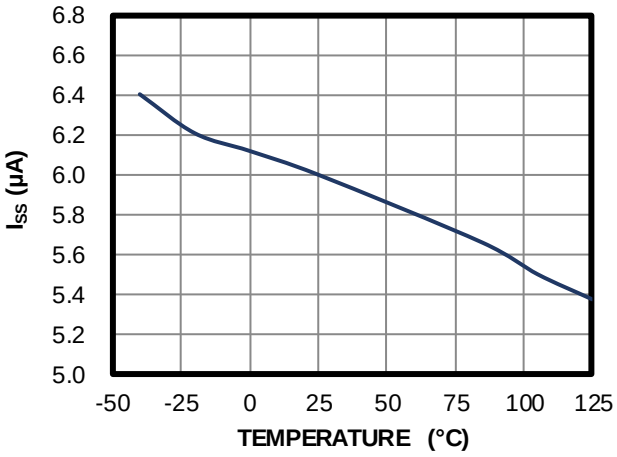
$R_{DS(ON)\_LS}$ vs. Temperature



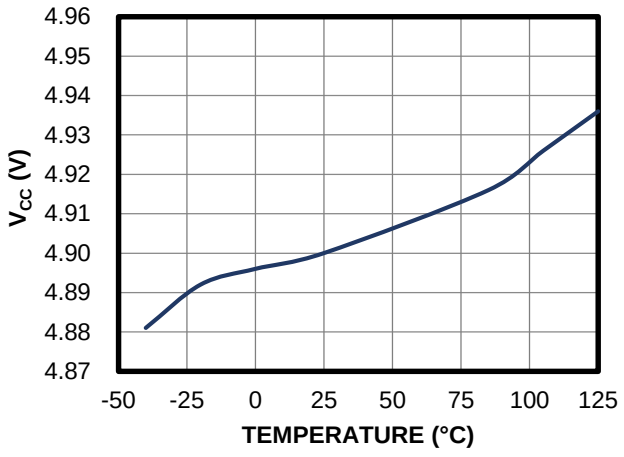
$R_{DS(ON)\_HS}$ vs. Temperature



Soft-Start Current vs. Temperature



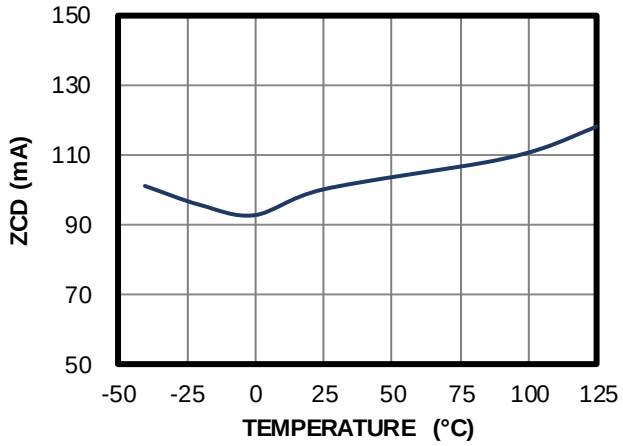
V_{CC} vs. Temperature



TYPICAL CHARACTERISTICS *(continued)*

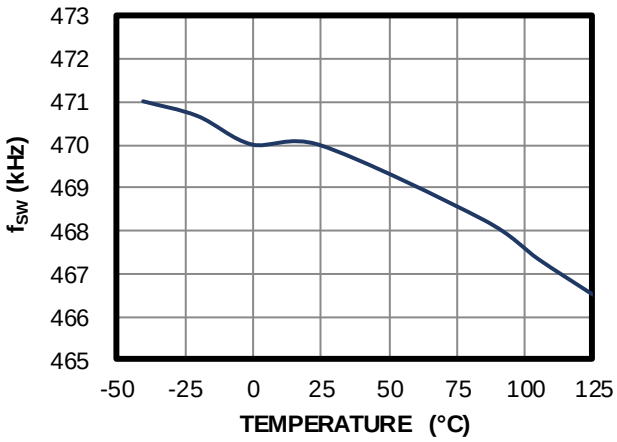
V_{IN} = 12V, T_J = -40°C to +125°C, unless otherwise noted.

ZCD vs. Temperature



f_{SW} vs. Temperature

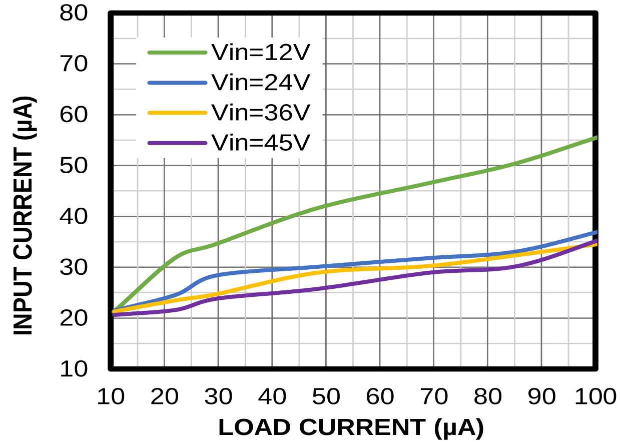
R_{FREQ} = 62kΩ



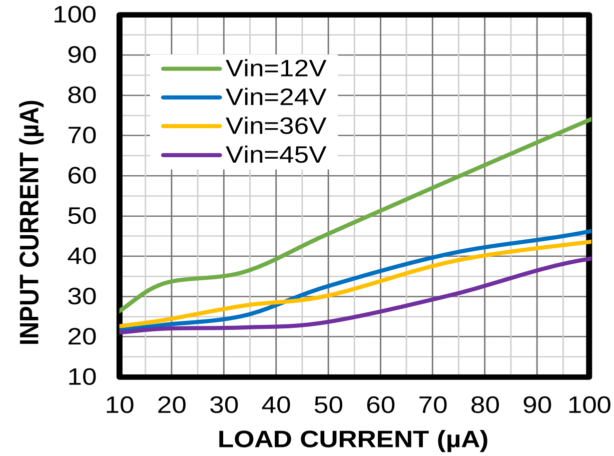
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH [(6)], f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

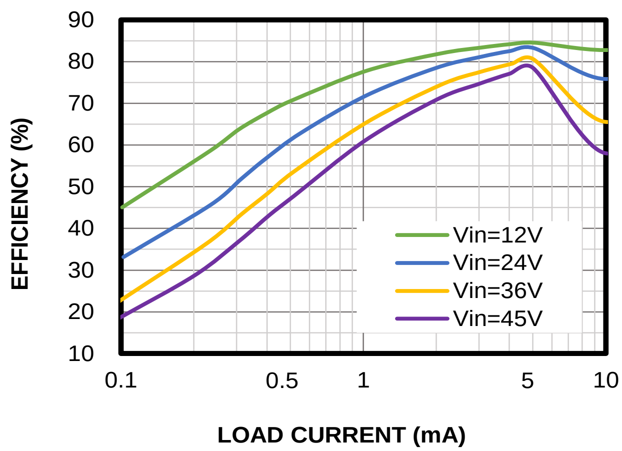
Input Current vs. Load Current
AAM mode, V_{OUT} = 3.3V



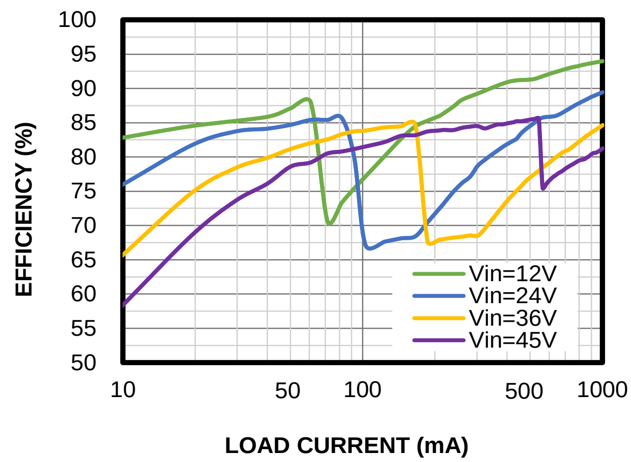
Input Current vs. Load Current
AAM mode, V_{OUT} = 5V



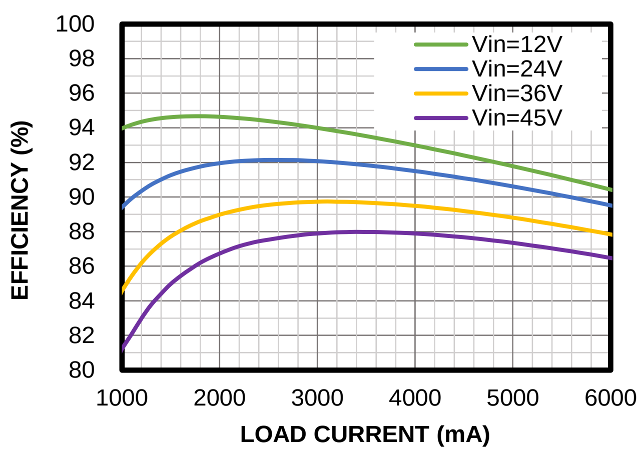
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



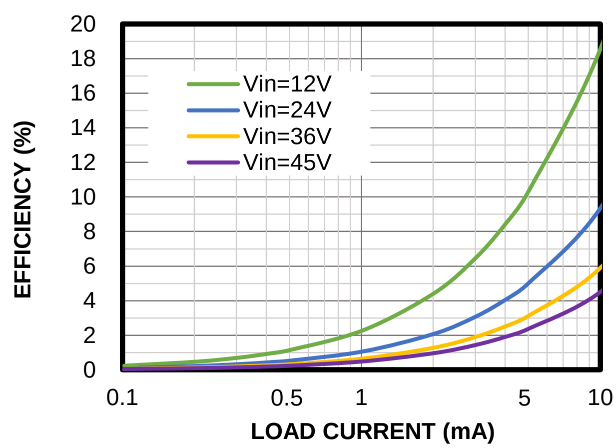
Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 3.3V



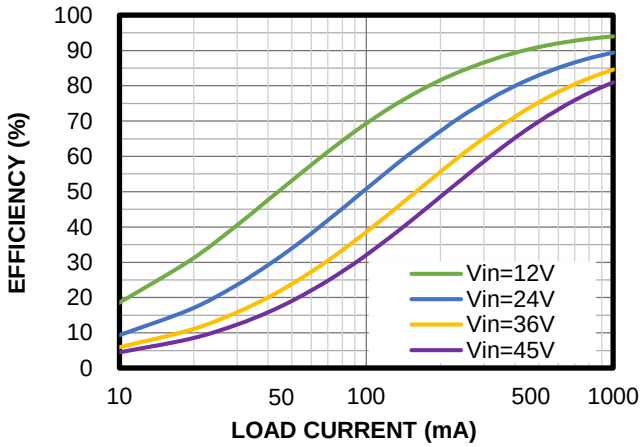
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



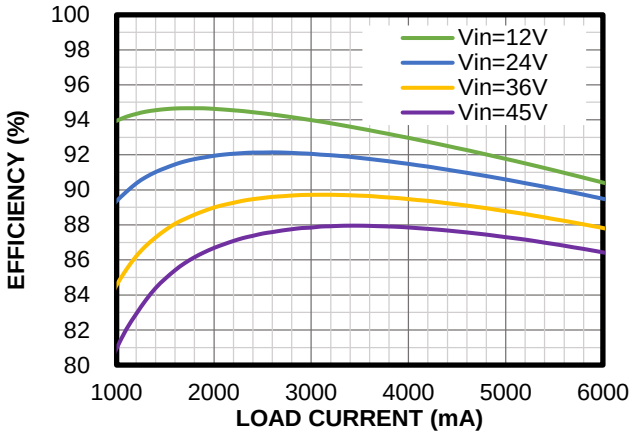
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (6), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

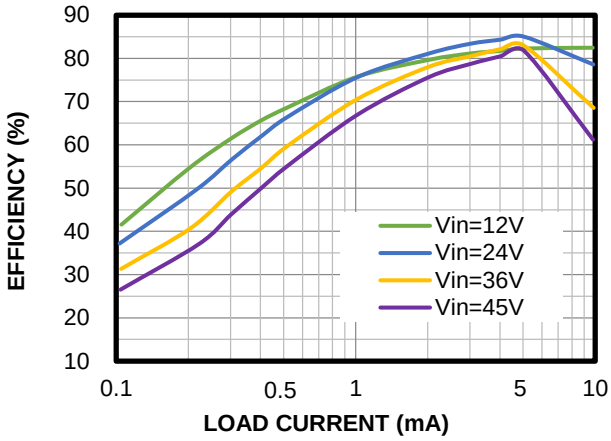
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



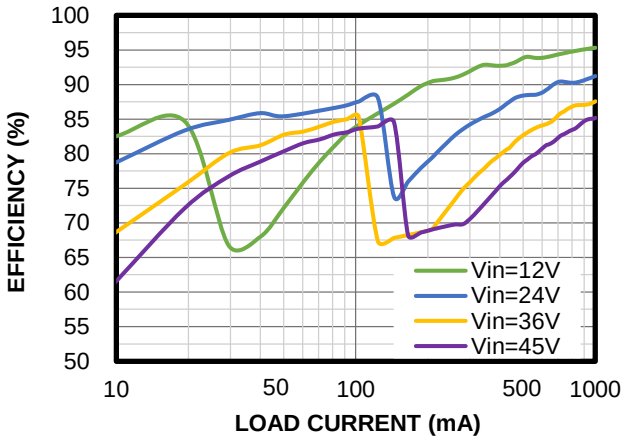
Efficiency vs. Load Current
FCCM, V_{OUT} = 3.3V



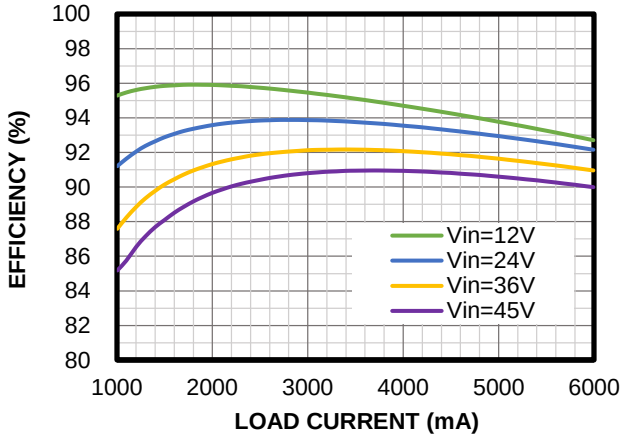
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



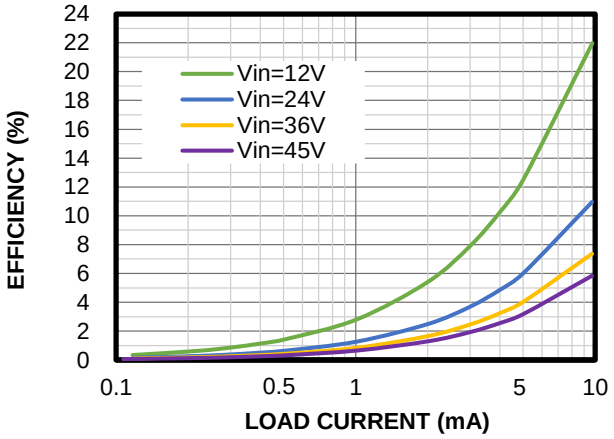
Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
AAM mode, V_{OUT} = 5V



Efficiency vs. Load Current
FCCM, V_{OUT} = 5V

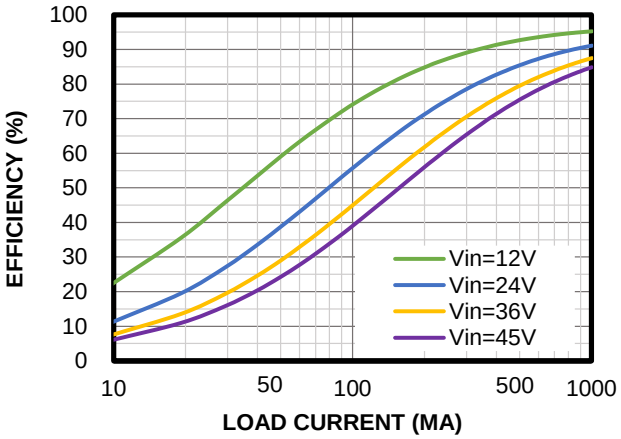


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (6), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

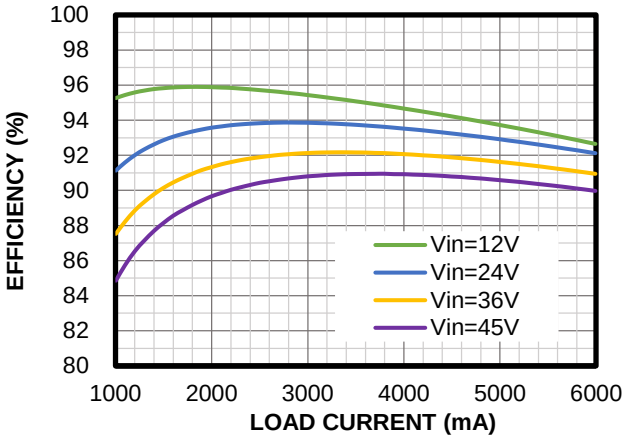
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



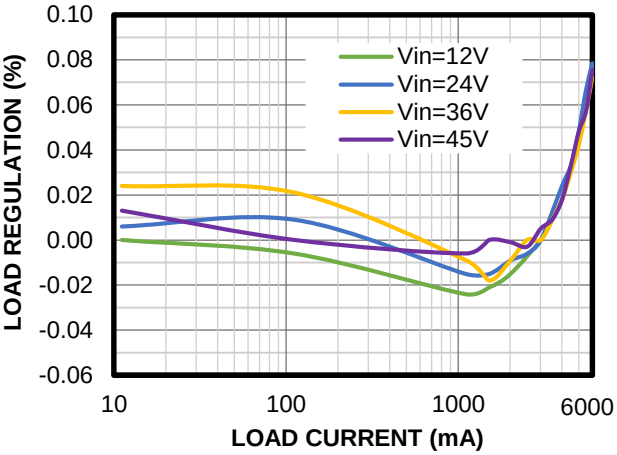
Efficiency vs. Load Current

FCCM, V_{OUT} = 5V



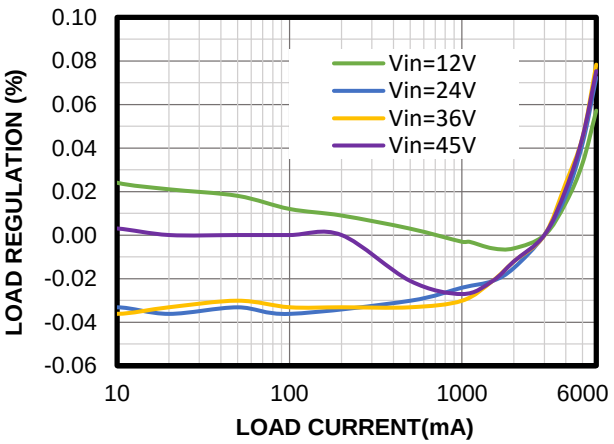
Load Regulation

AAM mode, V_{OUT} = 3.3V



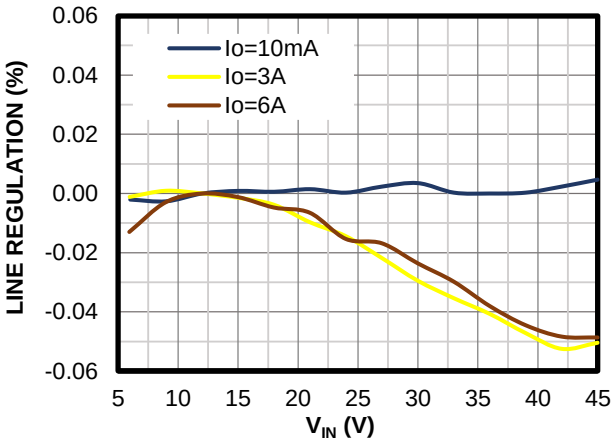
Load Regulation

FCCM, V_{OUT} = 3.3V



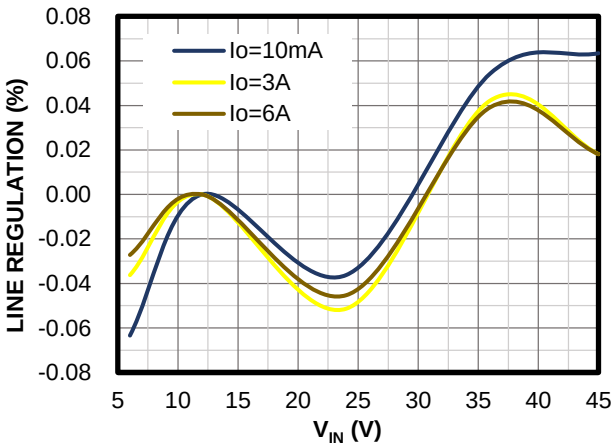
Line Regulation

AAM mode, V_{OUT} = 3.3V



Line Regulation

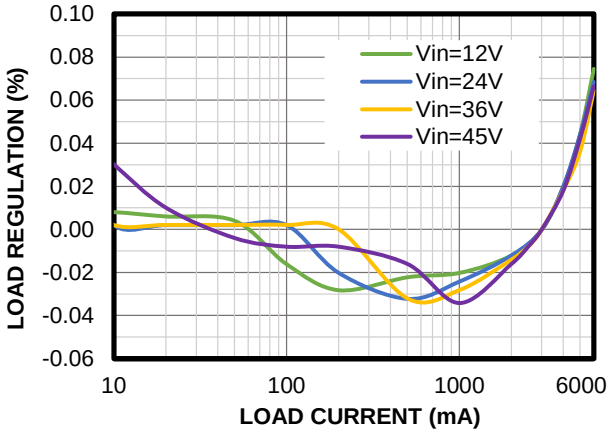
FCCM, V_{OUT} = 3.3V



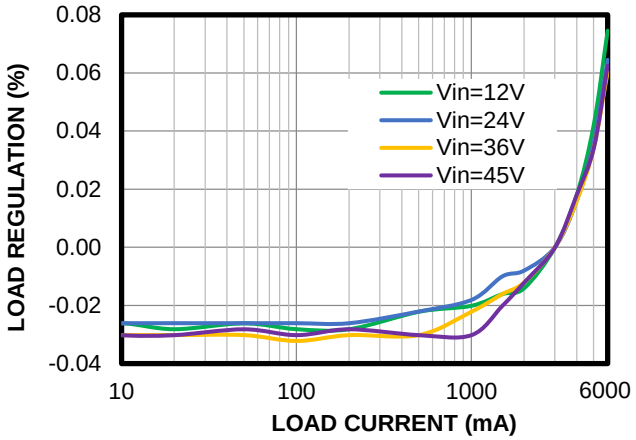
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (6), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

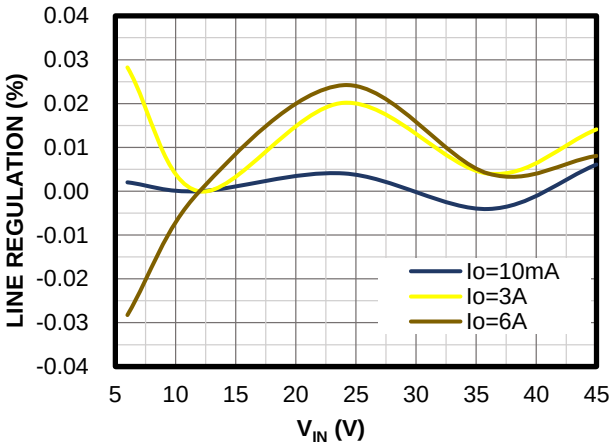
Load Regulation
AAM mode, V_{OUT} = 5V



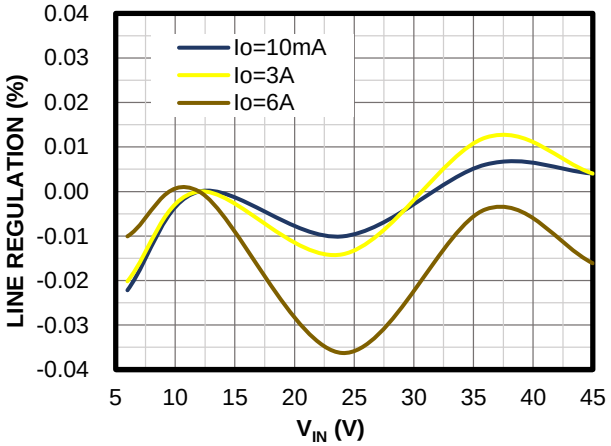
Load Regulation
FCCM, V_{OUT} = 5V



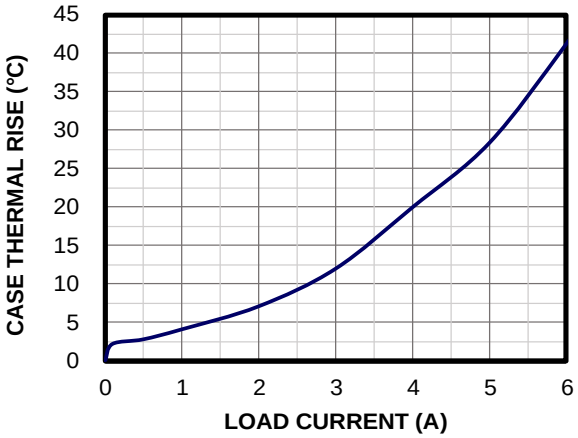
Line Regulation
AAM mode, V_{OUT} = 5V



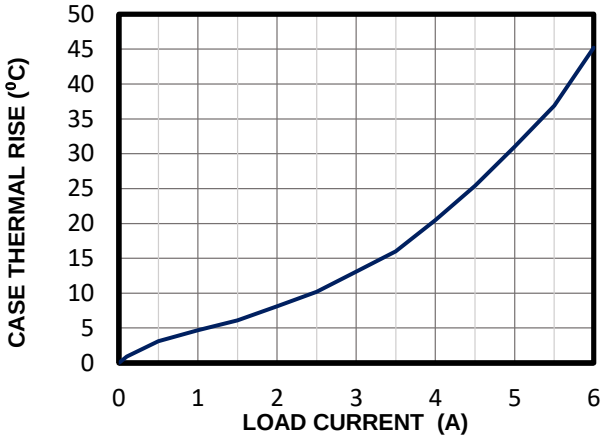
Line Regulation
FCCM, V_{OUT} = 5V



Case Thermal Rise
V_{OUT} = 3.3V



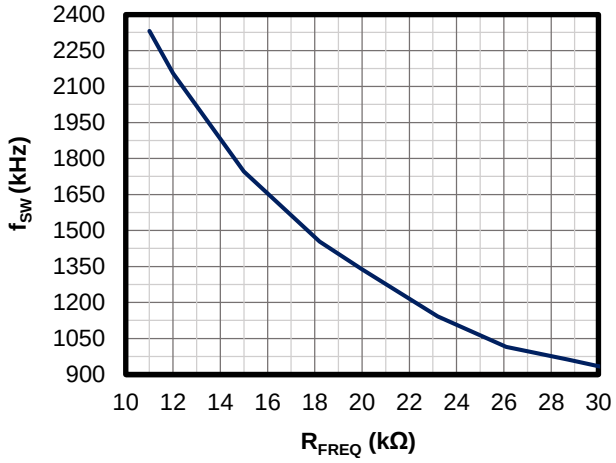
Case Thermal Rise
V_{OUT} = 5V



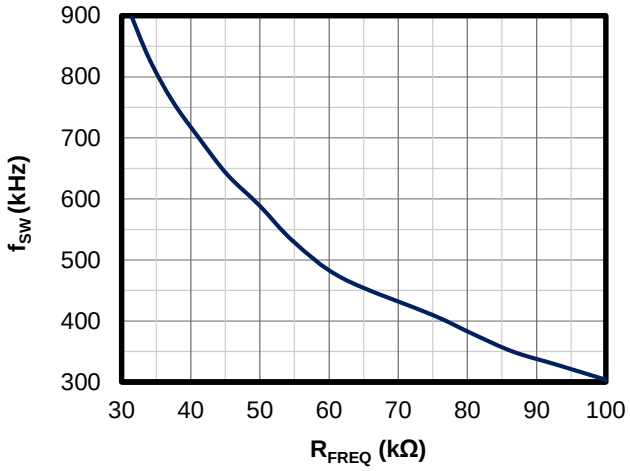
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH (6), f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

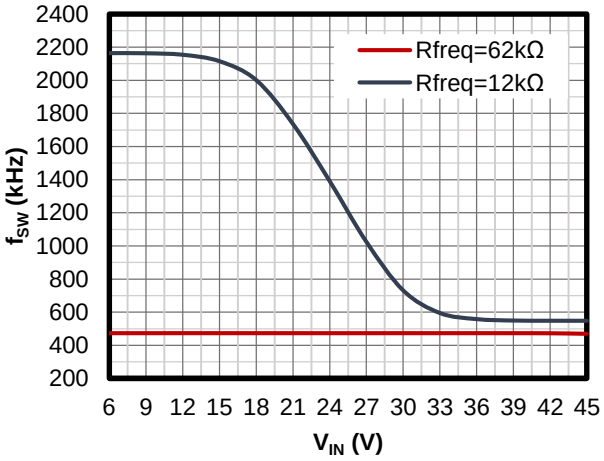
f_{SW} vs. R_{FREQ}
R_{FREQ} = 10kΩ to 30kΩ



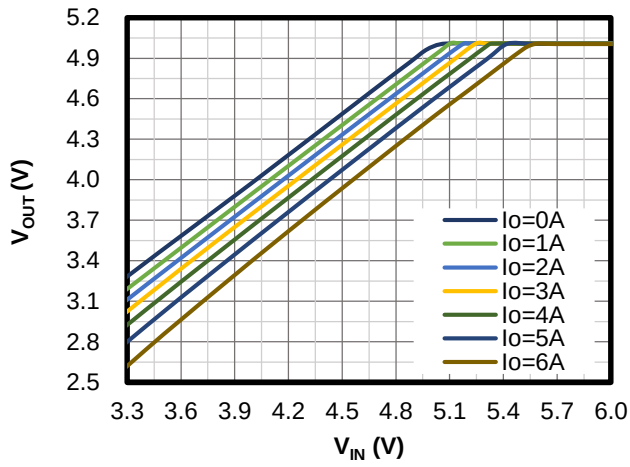
f_{SW} vs. R_{FREQ}
R_{FREQ} = 30kΩ to 100kΩ



f_{SW} vs. V_{IN}



Low-Dropout Mode
V_{OUT} = 5V

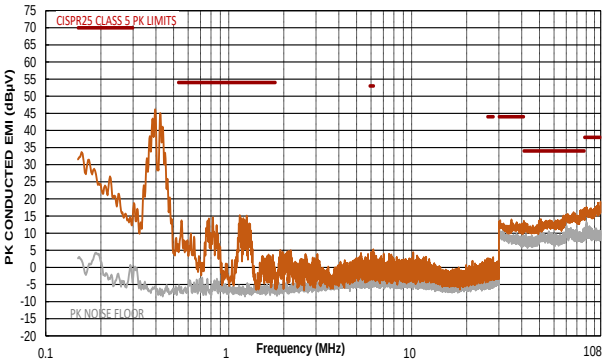


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (6), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.(7)

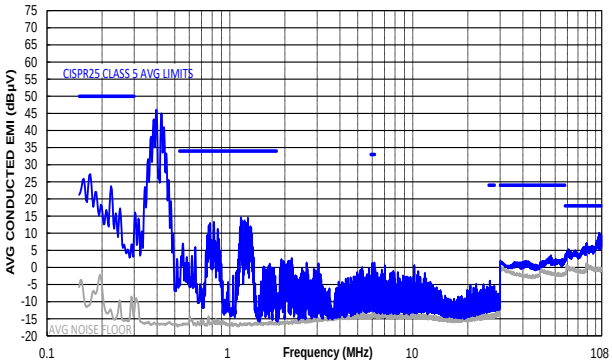
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



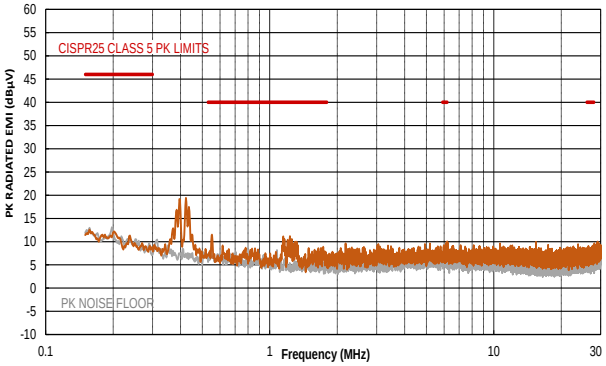
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



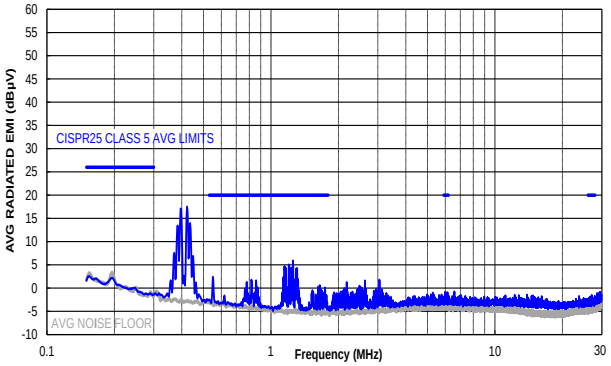
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



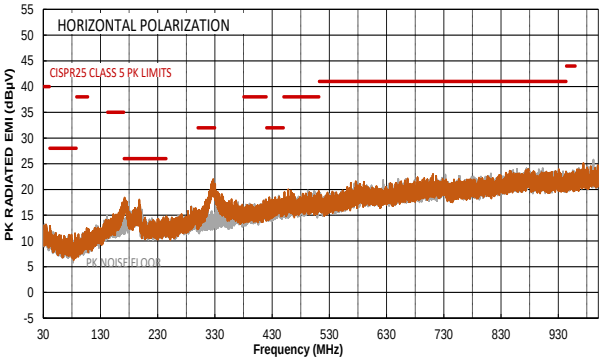
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



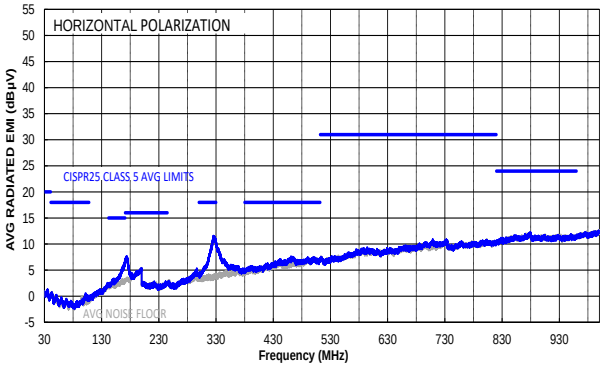
CISPR25 Class 5 Peak Radiated Horizontal

30MHz to 1GHz



CISPR25 Class 5 Average Radiated Horizontal

30MHz to 1GHz

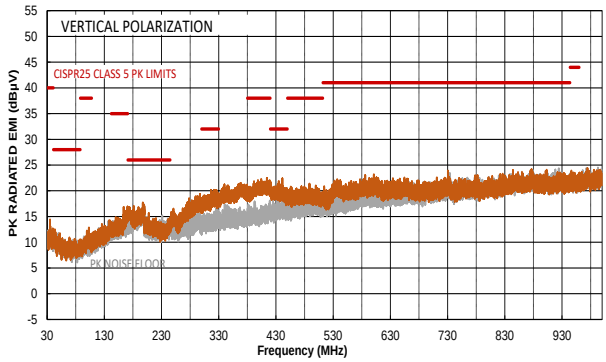


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A, L = 4.7µH (6), f_{SW} = 410kHz, T_A = 25°C, unless otherwise noted.(7)

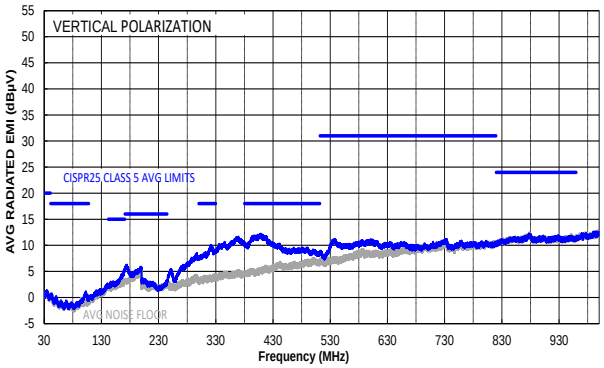
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 1GHz



Notes:

6) Inductor part number: XAL6060-472MEC. DCR = 15mΩ.

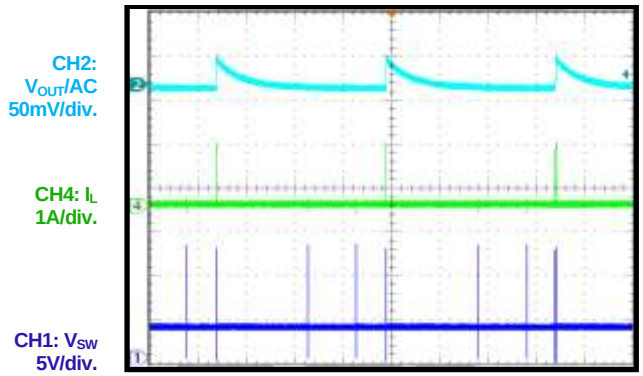
7) The EMC test results are based on the application circuit with EMI filters (see Figure 11 on page 36).

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

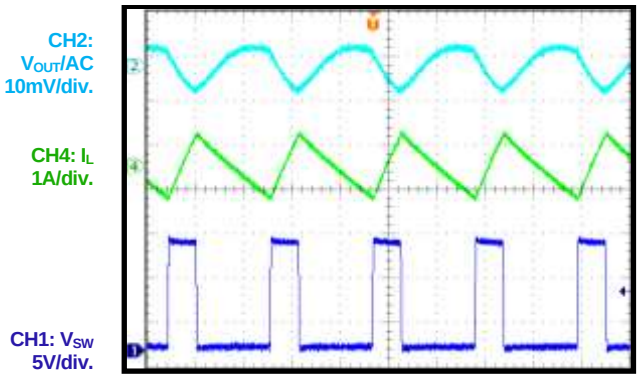
Steady State

I_{OUT} = 0A, AAM mode



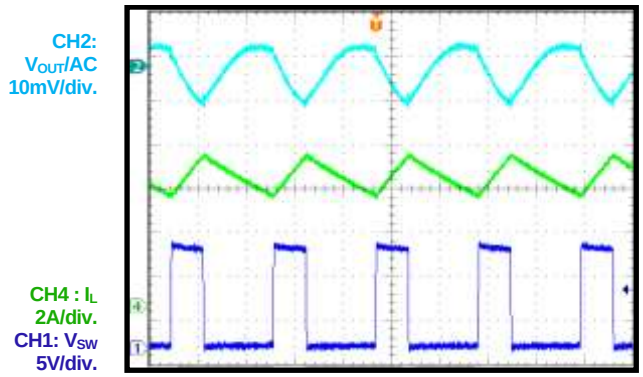
Steady State

I_{OUT} = 0A, FCCM



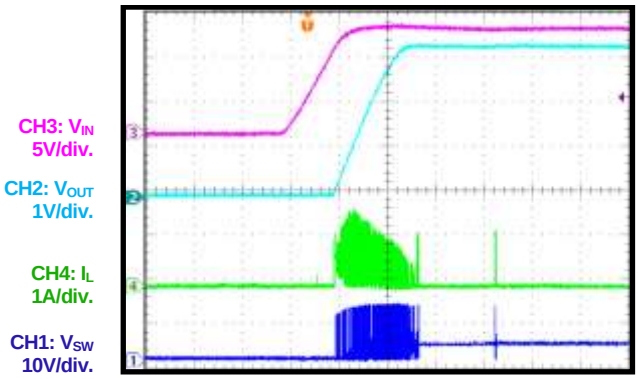
Steady State

I_{OUT} = 6A



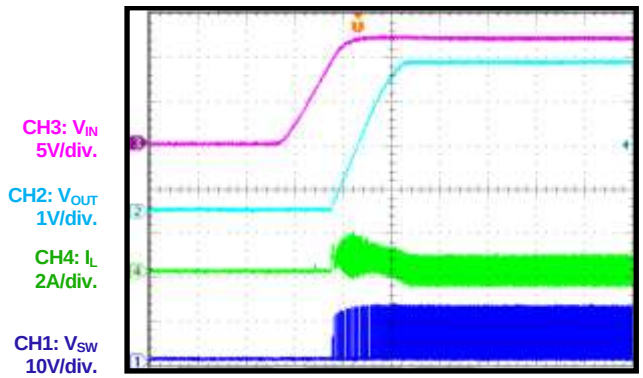
Start-Up through VIN

I_{OUT} = 0A, AAM mode



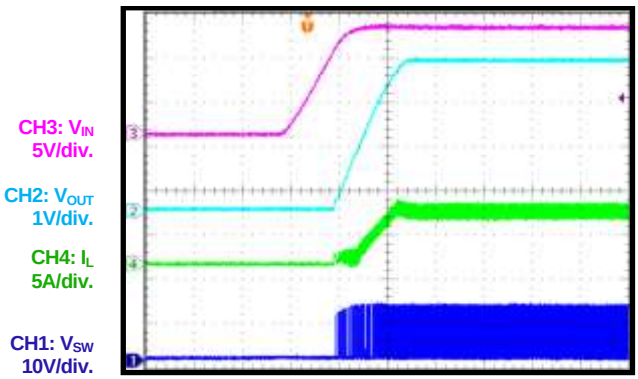
Start-Up through VIN

I_{OUT} = 0A, FCCM



Start-Up through VIN

I_{OUT} = 6A

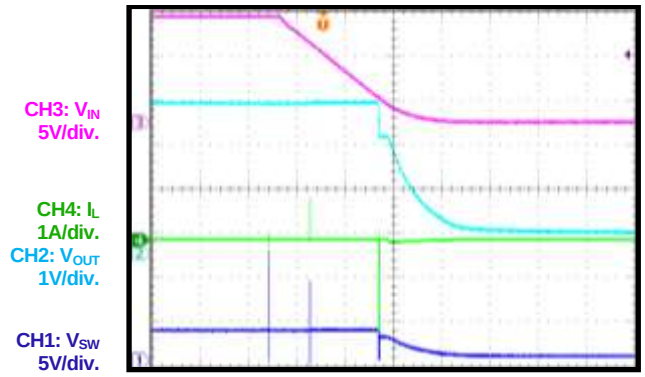


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

Shutdown through VIN

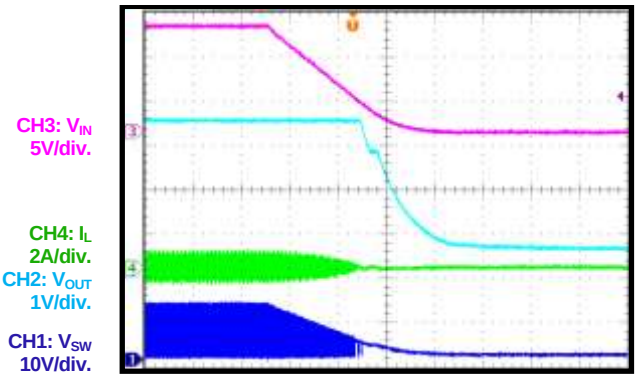
I_{OUT} = 0A, AAM mode



10ms/div.

Shutdown through VIN

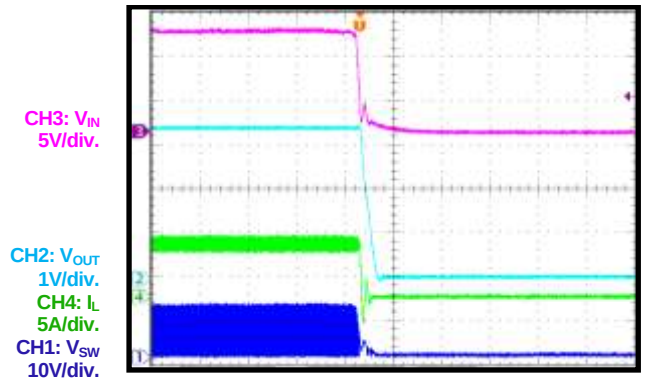
I_{OUT} = 0A, FCCM



10ms/div.

Shutdown through VIN

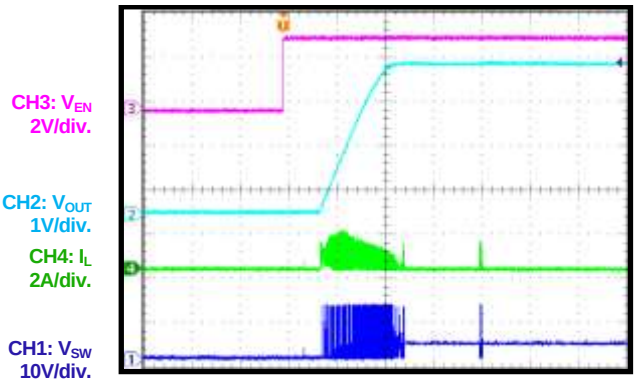
I_{OUT} = 6A



400µs/div.

Start-Up through EN

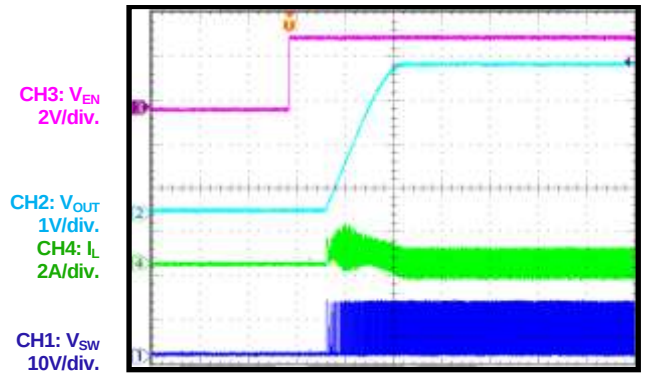
I_{OUT} = 0A, AAM mode



1ms/div.

Start-Up through EN

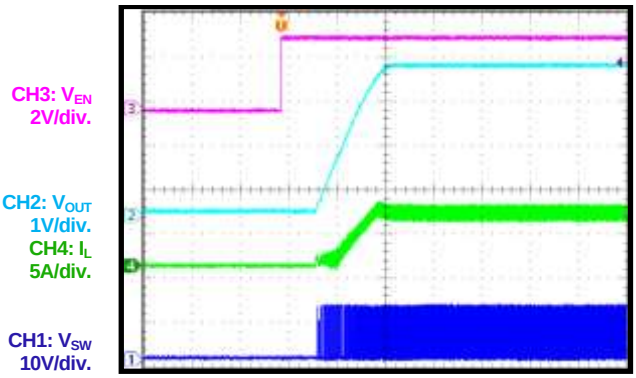
I_{OUT} = 0A, FCCM



1ms/div.

Start-Up through EN

I_{OUT} = 6A



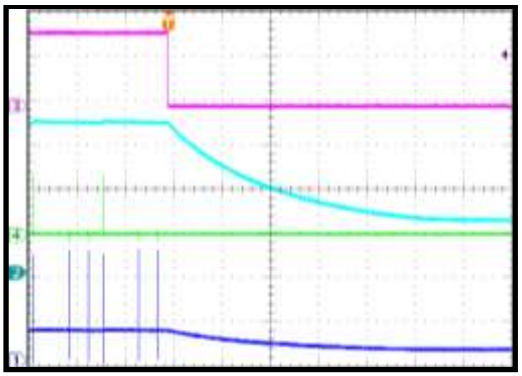
1ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

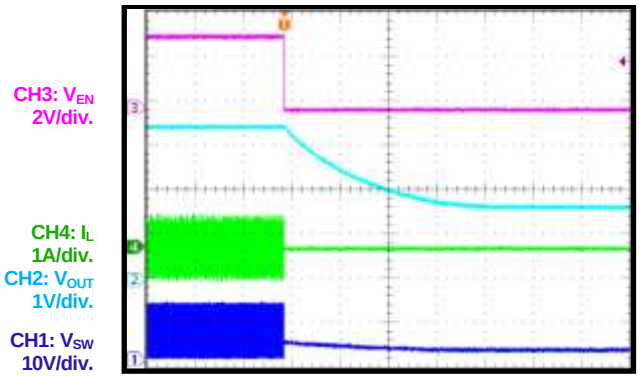
Shutdown through EN

I_{OUT} = 0A, AAM mode



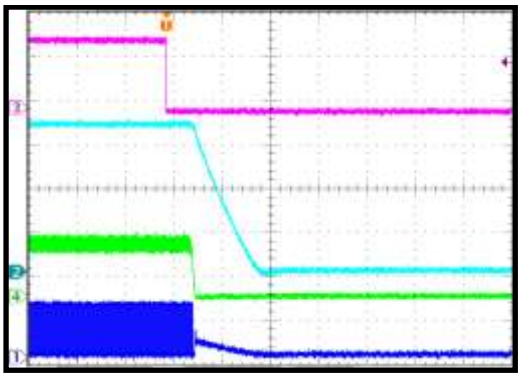
Shutdown through EN

I_{OUT} = 0A, FCCM



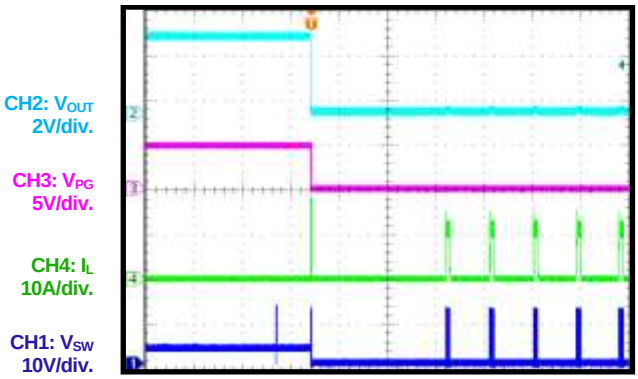
Shutdown through EN

I_{OUT} = 6A



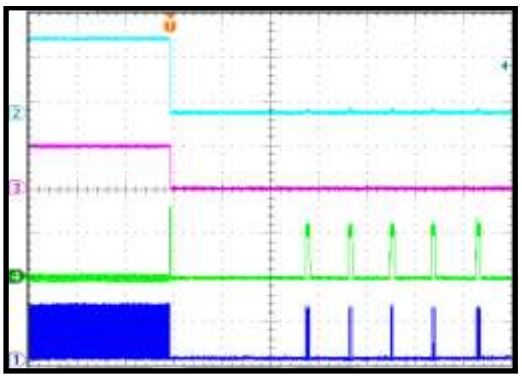
SCP Entry

I_{OUT} = 0A, AAM mode



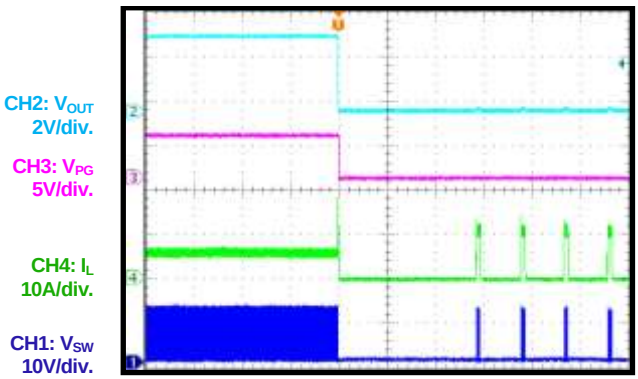
SCP Entry

I_{OUT} = 0A, FCCM



SCP Entry

I_{OUT} = 6A

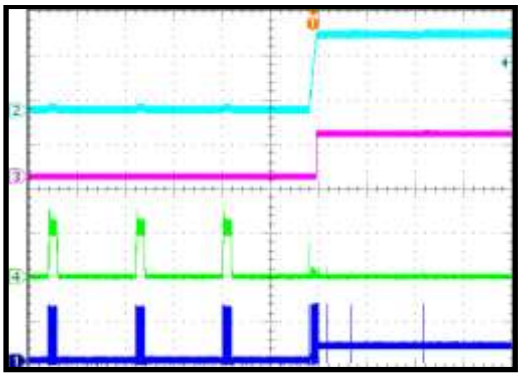


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

SCP Recovery

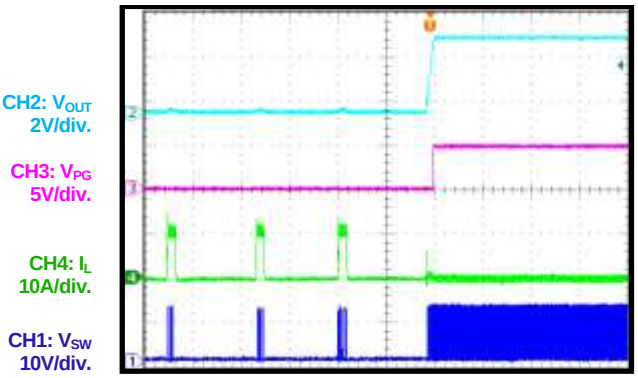
I_{OUT} = 0A, AAM mode



10ms/div.

SCP Recovery

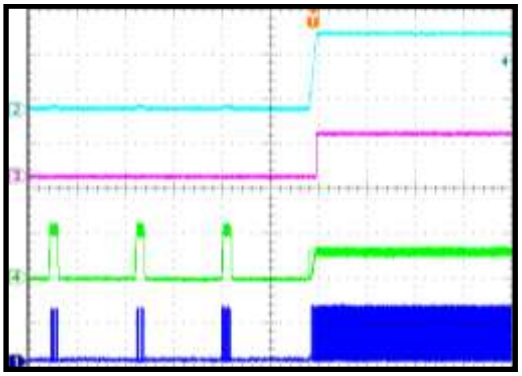
I_{OUT} = 0A, FCCM



10ms/div.

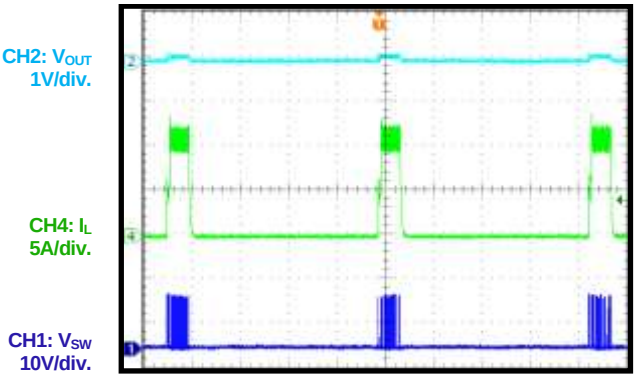
SCP Recovery

I_{OUT} = 6A



10ms/div.

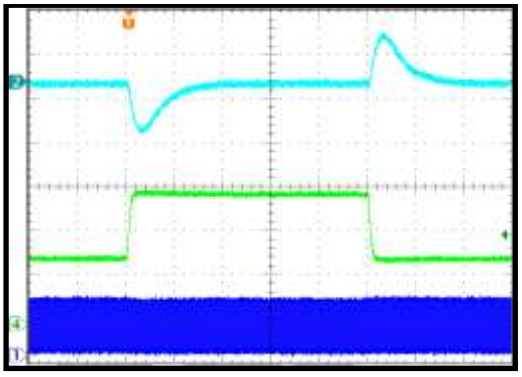
SCP Steady State



4ms/div.

Load Transient

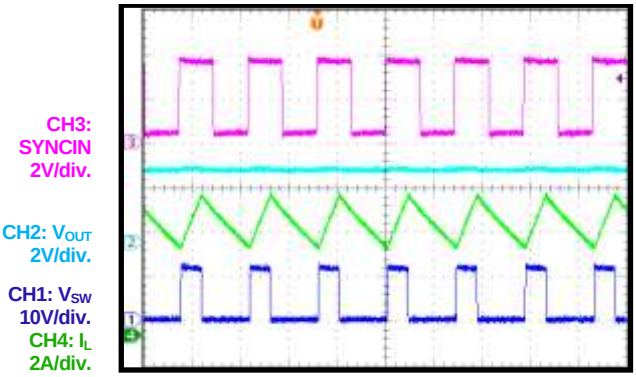
I_{OUT} = 3A to 6A, 1.6A/µs



100µs/div.

SYNCIN Operation

I_{OUT} = 6A, SYNC frequency = 350kHz



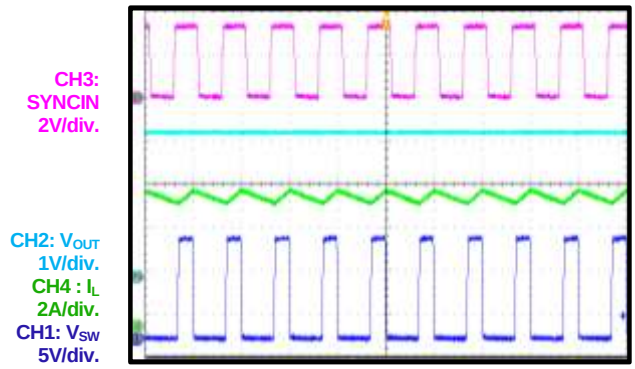
2µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

SYNCIN Operation

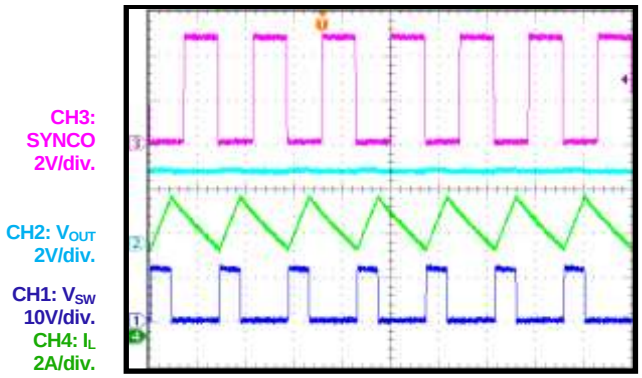
I_{OUT} = 6A, SYNC frequency = 1000kHz



1µs/div.

SYNCO Operation

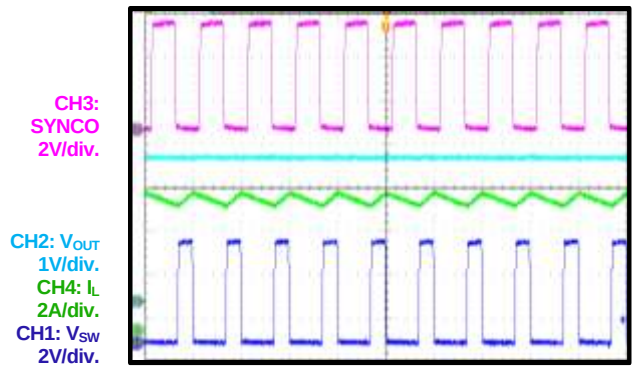
I_{OUT} = 6A, SYNC frequency = 350kHz



2µs/div.

SYNCO Operation

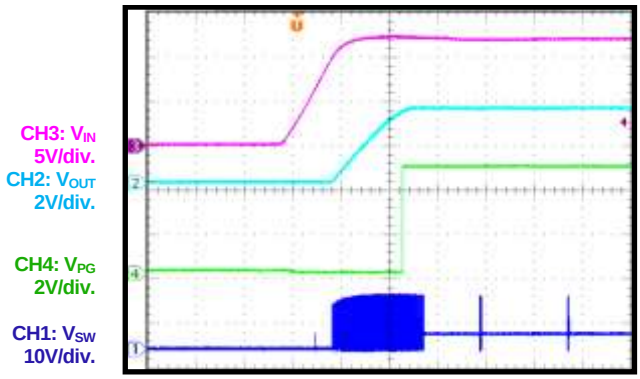
I_{OUT} = 6A, SYNC frequency = 1000kHz



1µs/div.

PG Start-Up through VIN

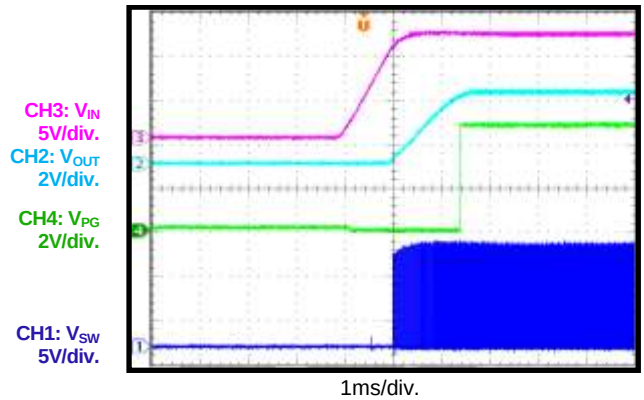
I_{OUT} = 0A



1ms/div.

PG Start-Up through VIN

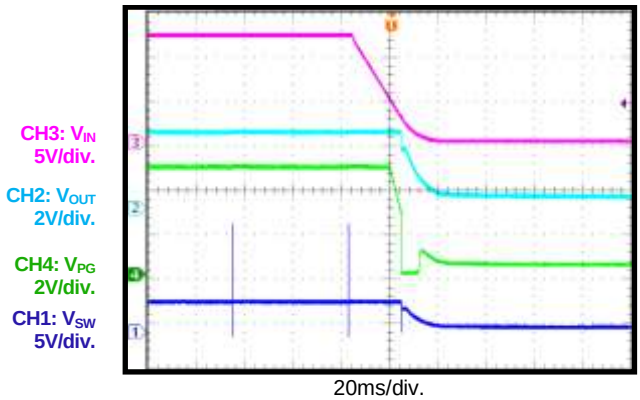
I_{OUT} = 6A



1ms/div.

PG Shutdown through VIN

I_{OUT} = 0A



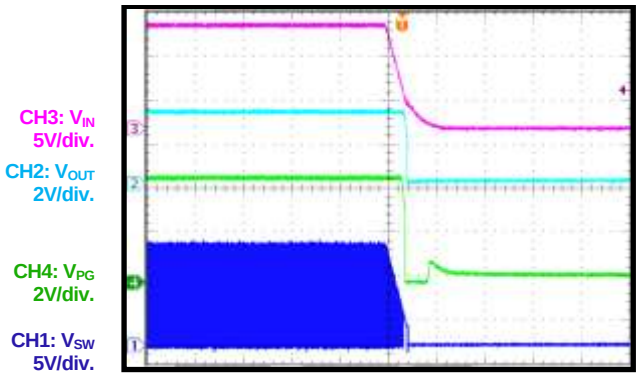
20ms/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

PG Shutdown through VIN

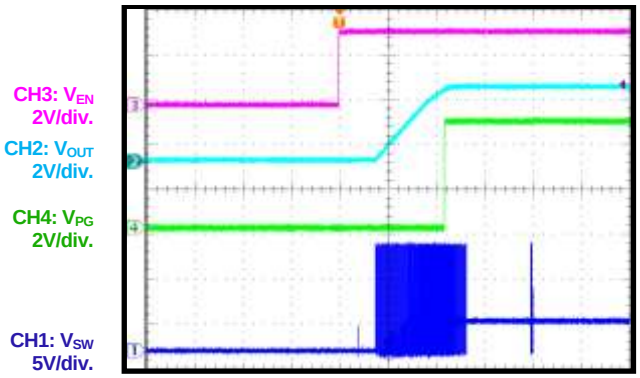
I_{OUT} = 6A



20ms/div.

PG Start-Up through EN

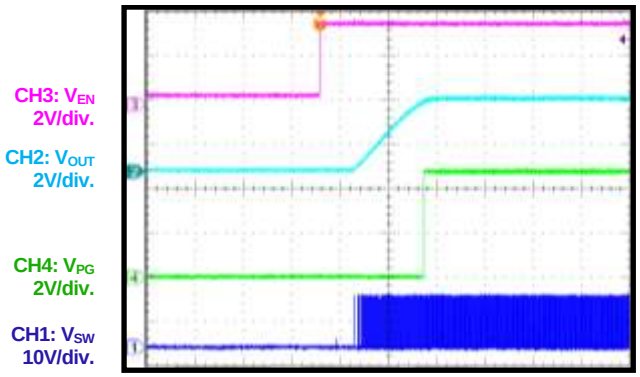
I_{OUT} = 0A



1ms/div.

PG Start-Up through EN

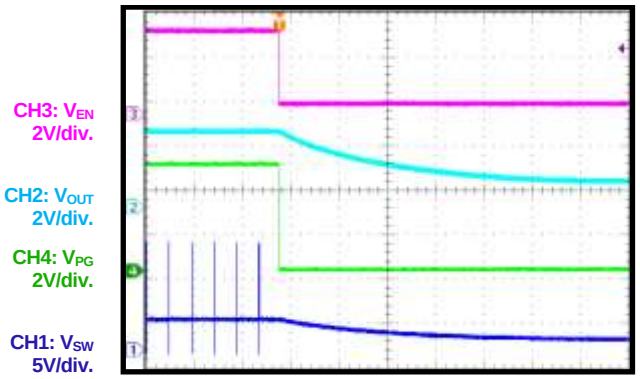
I_{OUT} = 6A



1ms/div.

PG Shutdown through EN

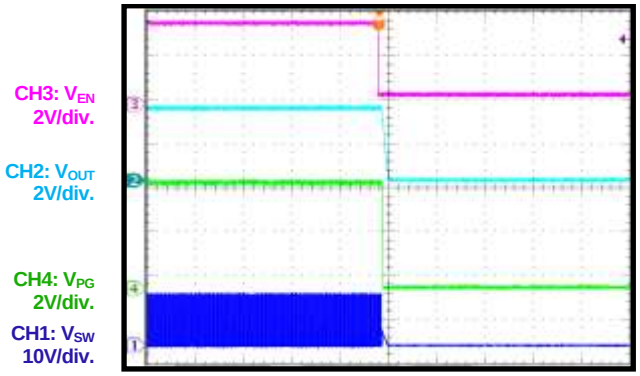
I_{OUT} = 0A



100ms/div.

PG Shutdown through EN

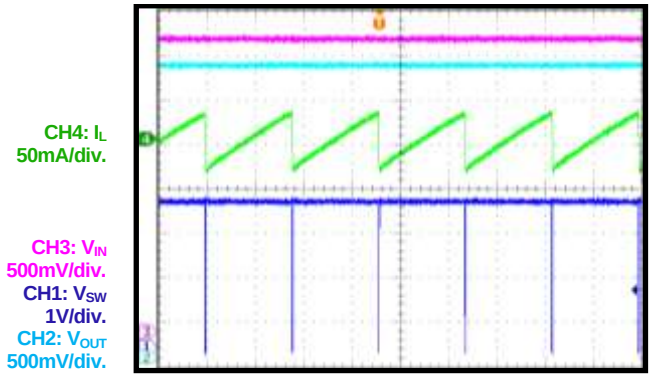
I_{OUT} = 6A



1ms/div.

Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 0A



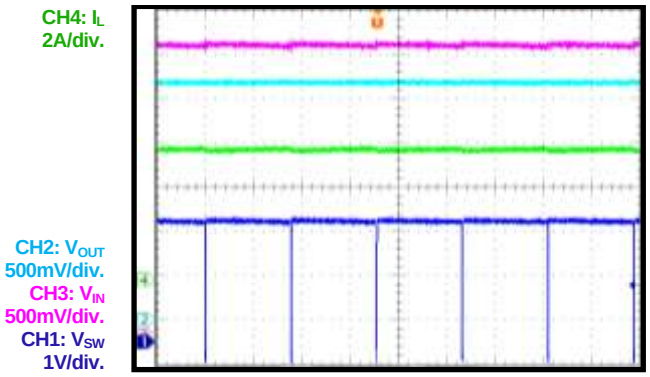
4µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, f_{SW} = 470kHz, AAM mode, T_A = 25°C, unless otherwise noted.

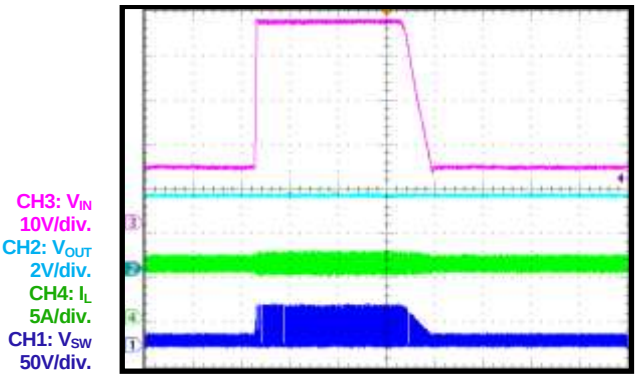
Low-Dropout Mode

V_{IN} = 3.3V, V_{OUT} set to 3.3V, I_{OUT} = 6A



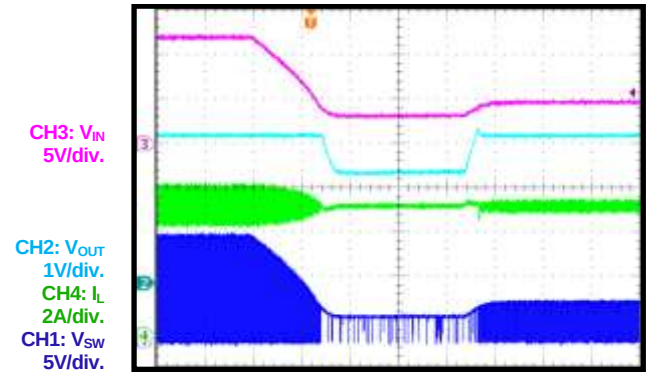
Load Dump

V_{IN} = 12V to 36V, I_{OUT} = 6A



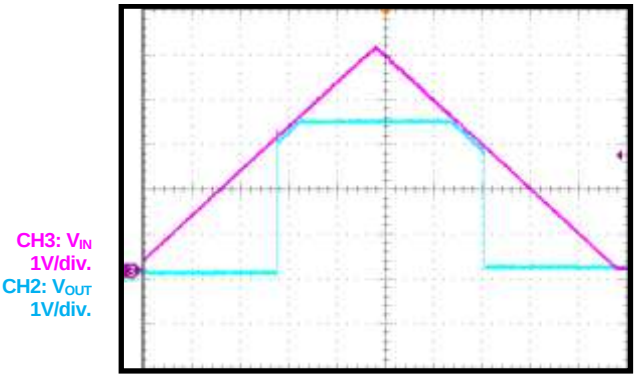
Cold Crank

V_{IN} = 12V to 3.3V to 5V, I_{OUT} = 6A



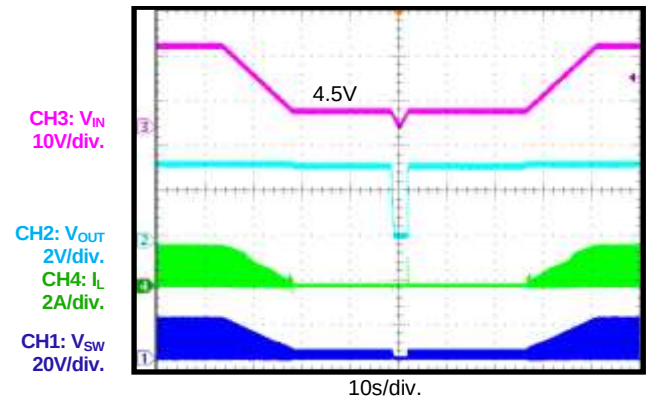
V_{IN} Ramping Up and Down

I_{OUT} = 0.1A



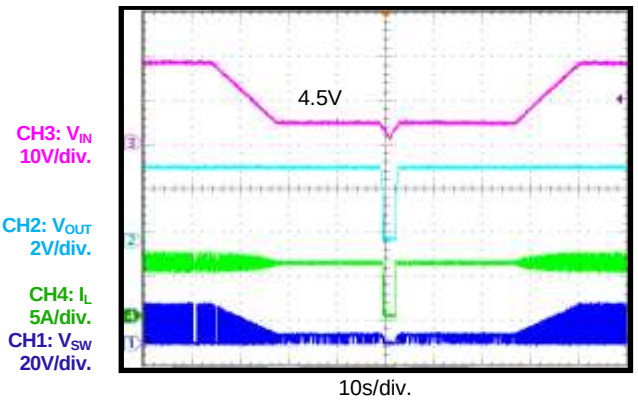
V_{IN} Ramping Down and Up

I_{OUT} = 1mA



V_{IN} Ramping Down and Up

I_{OUT} = 6A



FUNCTIONAL BLOCK DIAGRAM

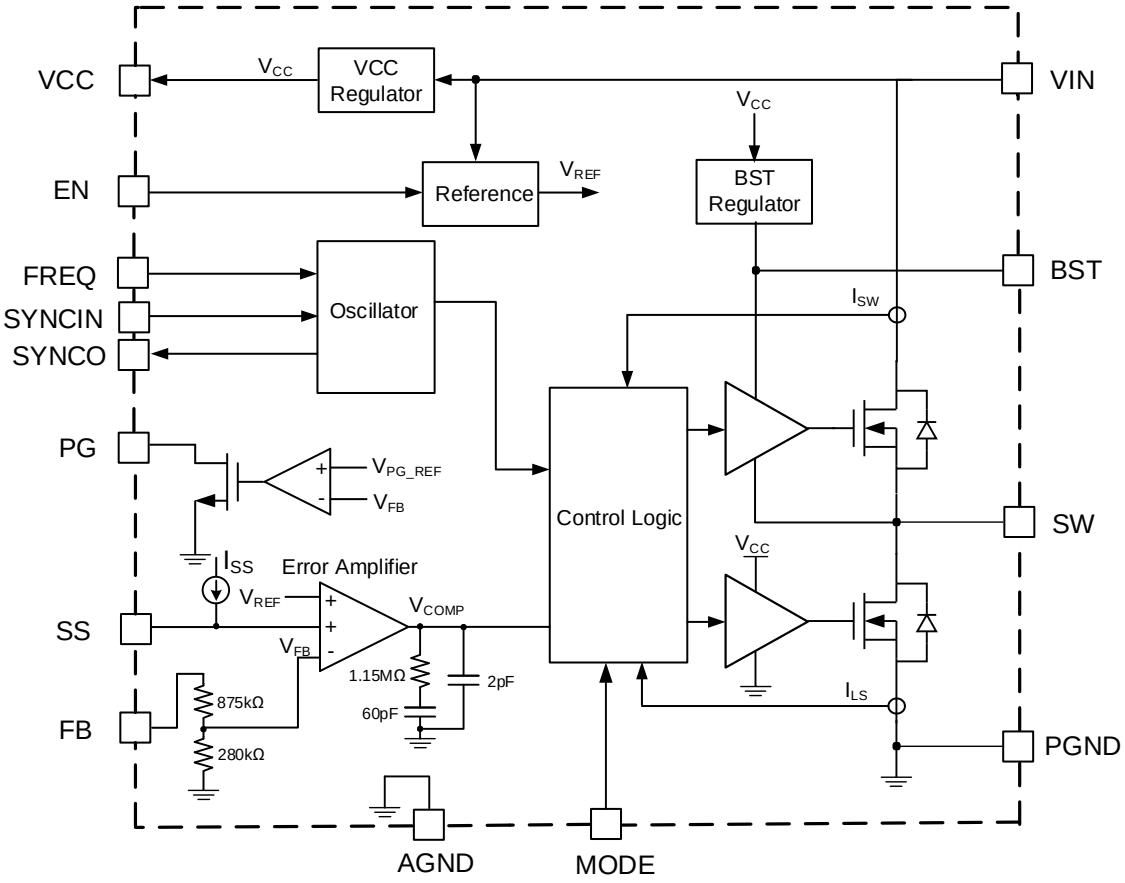


Figure 1: Functional Block Diagram (3.3V Fixed Output Version)

FUNCTIONAL BLOCK DIAGRAM *(continued)*

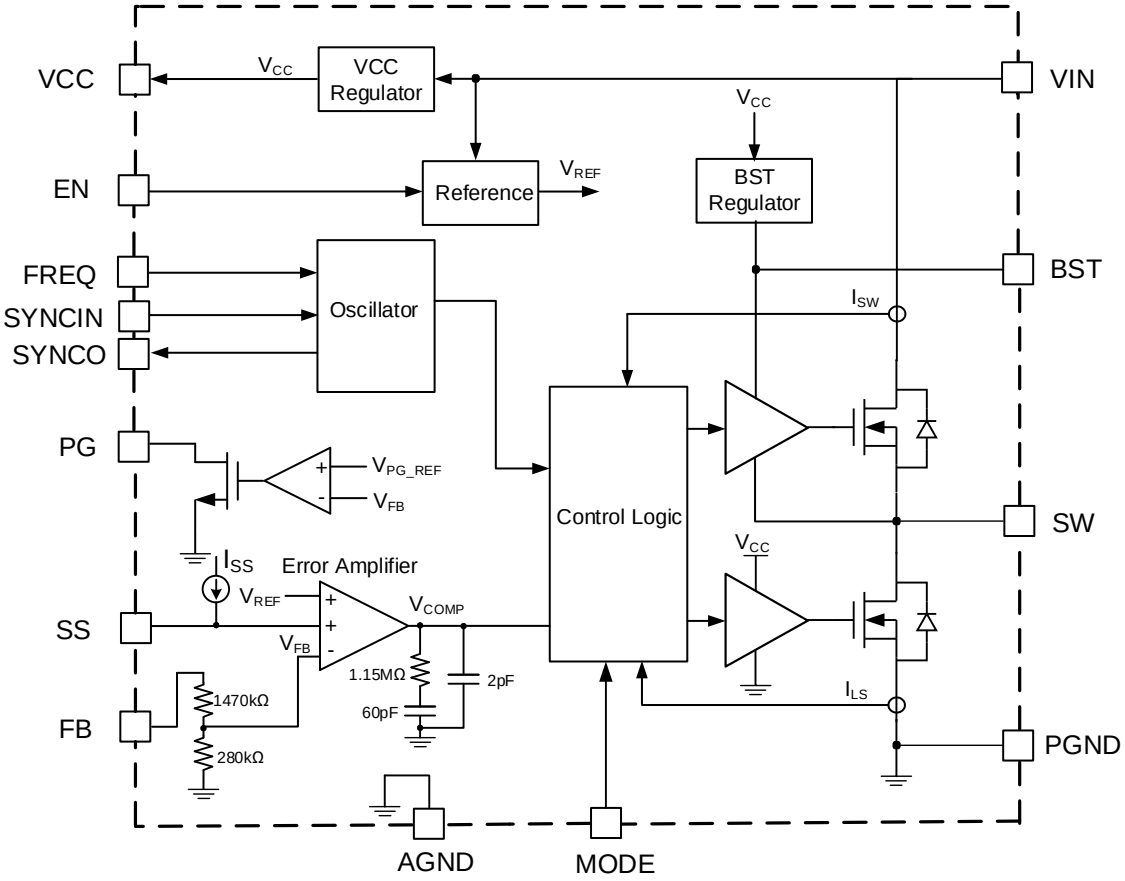


Figure 2: Functional Block Diagram (5V Fixed Output Version)

Timing Sequence

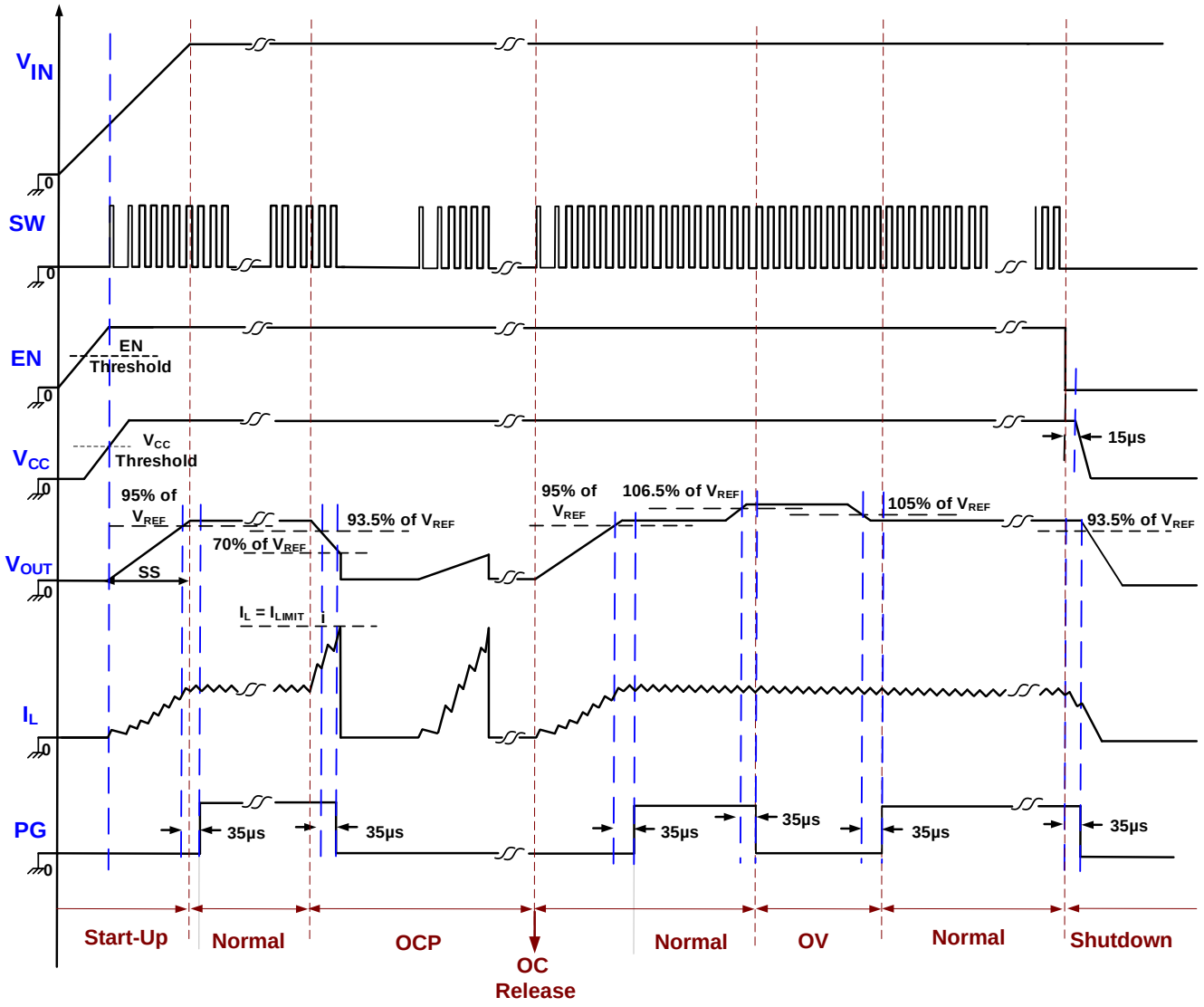


Figure 3: Timing Sequence

OPERATION

The MPQ4436A is a synchronous, step-down switching regulator with integrated internal high-side and low-side power MOSFETs (HS-FET and LS-FET, respectively). It provides 6A of highly efficient output current (I_{OUT}) with current mode control.

It features a wide input voltage (V_{IN}) range, configurable switching frequency (f_{SW}), external soft start (SS), and precision current limiting. Its very low operational quiescent current (I_Q) makes it ideal for battery-powered applications.

Pulse-Width Modulation (PWM) Control

At moderate to high output currents, the MPQ4436A operates in fixed-frequency, peak current control mode to regulate the output voltage (V_{OUT}). A PWM cycle is initiated by the internal clock. At the rising edge of the clock, the HS-FET turns on and remains on until its current reaches the value set by the internal COMP voltage (V_{COMP}). Once the HS-FET is on, it remains on for at least 100ns.

When the HS-FET is off, the LS-FET turns on immediately and remains on until the next cycle starts. Once the LS-FET is on, it remains on for at least 80ns before next cycle starts.

If the current in the HS-FET does not reach the COMP-set current value within one PWM period, then the HS-FET remains on, saving a turn-off operation. If the on time lasts about 10µs, then the HS-FET is forced off even though COMP is not reached.

Light-Load Operation

Under light-load conditions, the MPQ4436A can work in two different operation modes by setting the MODE pin to one of two different statuses .

The MPQ4436A works in forced continuous conduction mode (FCCM) when the MODE pin is pulled above 1.8V. In this mode, the part works with a fixed frequency from no load to full load. The advantage of FCCM is the controllable frequency and lower output ripple at light loads.

The MPQ4436A works in asynchronous advanced modulation (AAM) mode when the MODE pin is pulled below 0.4V. AAM is meant to optimize the efficiency during light-load and no-load conditions.

When AAM mode is enabled, the MPQ4436A first enters asynchronous operation as long as the inductor current (I_L) approaches 0A at light load. If the load is further decreased or there is no load that makes V_{COMP} decrease to the set value, the MPQ4436A enters AAM mode. In AAM mode, the internal clock is reset every time V_{COMP} crosses over the set value. The crossover time is taken as the benchmark of the next clock. When the load increases and V_{COMP} exceeds the set value, the operation mode is discontinuous conduction mode (DCM) or CCM, which has a constant f_{SW} (see Figure 4).

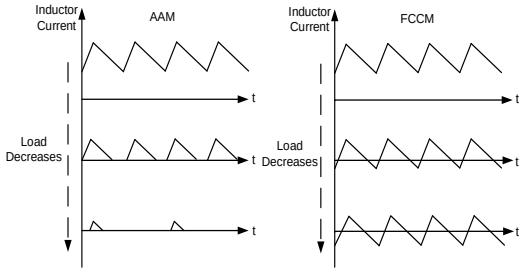


Figure 4: AAM and FCCM

Error Amplifier (EA)

The error amplifier (EA) compares the FB pin's voltage (V_{FB}) with the internal reference voltage (V_{REF}, typically 0.815V) and outputs a current proportional to the difference between the two. This current is then used to charge the compensation network to form V_{COMP}, which is used to control the power MOSFET current.

During operation, the minimum V_{COMP} is clamped to 0.9V, and the maximum V_{COMP} is clamped to 2V. COMP is internally pulled down to GND in shutdown mode.

Internal VCC Regulator

Most of the internal circuitry is powered by the internal 4.9V VCC regulator. This regulator takes V_{IN} as the input and operates across the full V_{IN} range. When V_{IN} exceeds 4.9V, VCC is in full regulation. When V_{IN} is below this point, the output VCC voltage (V_{CC}) degrades.

Bootstrap (BST) Charging

The bootstrap (BST) capacitor (C_{BST}) is charged and regulated to about 5V by the dedicated internal BST regulator. When the voltage between the BST and SW nodes is below its

regulation value, a PMOS pass transistor connected from VCC to BST turns on to charge C_{BST}. External circuitry should provide enough voltage headroom to facilitate charging. When the HS-FET is on, BST is above VCC, so C_{BST} cannot be charged.

At higher duty cycles, the time period available for BST charging is shorter, so C_{BST} may not be charged sufficiently. If the external circuit has not had sufficient voltage and time to charge C_{BST}, extra external circuitry can be used to ensure that the bootstrap voltage (V_{BST}) is within the normal operation range.

Low-Dropout Mode and BST Refresh

To improve dropout, the MPQ4436A is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage is greater than 2.5V. When the voltage from BST to SW drops below 2.5V, the HS-FET turns off using an under-voltage lockout (UVLO) circuit, which allows the LS-FET to conduct and refresh the charge on C_{BST}. In DCM or pulse-skip mode (PSM), the LS-FET is forced on to refresh V_{BST}.

Since the supply current sourced from C_{BST} is low, the HS-FET remains on for more switching cycles than are required to refresh the capacitor. Therefore, the effective duty cycle of the switching regulator is high.

The effective duty cycle during dropout of the regulator is mainly influenced by the voltage drops across the power MOSFET, inductor resistance, the low-side diode, and PCB resistance.

Enable (EN) Control

EN is a digital control pin that turns the regulator on and off (see Figure 5).

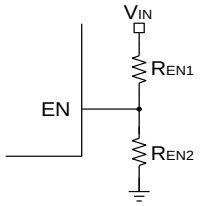


Figure 5: Enable Divider Circuit

It offers two main features:

1. EN is enabled by an external logic (H/L) signal. When EN is pulled below the falling voltage threshold (0.85V), the chip is put into the lowest shutdown current mode. Forcing this pin above the EN rising threshold voltage (1V) turns on the part.
2. EN can configure V_{IN} UVLO. With high enough V_{IN}, the chip can be enabled and disabled by the EN pin. This pin can generate a configurable V_{IN} UVLO and hysteresis.

Frequency Programmable and Foldback

The MPQ4436A's oscillating frequency is programmed either by an external resistor (R_{FREQ}) from the FREQ pin to ground, or by a logic-level SYNC signal. To get an expected f_{SW}) select the R_{FREQ} value following the f_{SW} vs. R_{FREQ} curve (see the Typical Performance Characteristics section on page 15).

When f_{SW} is high, it folds back at high input voltages to avoid triggering the minimum on time (t_{ON_MIN}) and the output going out of regulation. The recommended f_{SW} range for car battery applications is 350kHz to 1000kHz. Table 1 lists the recommended R_{FREQ} values for common frequencies. Higher frequencies can be used in applications that do not have a critical f_{SW} limit, as well as applications with a low, stable V_{IN}.

Table 1: R_{FREQ} vs. f_{SW}

R_{FREQ} (kΩ)	f_{SW} (kHz)
86.6	350
80.6	380
75	410
62	470
59	500
54.9	530
49.9	590
45.3	640
41.2	700
37.4	760
34	830
30.9	910
28.7	960
26.1	1000

Frequency Spread Spectrum (FSS)

The MPQ4436A uses a 12kHz modulation frequency with a 128-step triangular profile to spread the internal oscillator frequency over a 20% (±10%) window (see Figure 6 on page 30). The steps are fixed and independent of the set oscillator frequency to optimize frequency spread spectrum (FSS) performance.

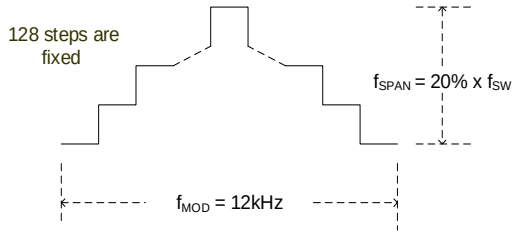


Figure 6: Spread Spectrum Scheme

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter's V_{OUT} from overshooting during start-up.

When the soft-start time (t_{SS}) starts, an internal current source begins charging the external soft-start capacitor (C_{SS}). When the soft-start voltage (V_{SS}) falls below the V_{REF}, V_{SS} overrides V_{REF} and the EA uses V_{SS} as the reference. When V_{SS} exceeds V_{REF}, V_{REF} is used as the reference. C_{SS} can be calculated with Equation (1):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} = 6.25 \times t_{SS}(ms) \quad (1)$$

The SS pins can be used for tracking and sequencing.

Pre-Biased Start-Up

For the MPQ4436A, if $V_{FB} > V_{SS}$ - 150mV at start-up (which means the output has a pre-biased voltage), neither the HS-FET nor LS-FET are turned on until V_{SS} exceeds V_{FB}.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. If the silicon die temperature exceeds its upper threshold (170°C), the power MOSFETs shut down. When the temperature falls below its lower threshold (150°C), the chip is enabled again.

Current Comparator and Current Limit

The power MOSFET current is accurately sensed via a current-sense MOSFET. It is then fed to the high-speed current comparator for current mode control. The current comparator takes this sensed current as one of its inputs.

When the HS-FET turns on, the comparator is blanked until the end of the turn-on transition to avoid noise. Then the comparator compares the power MOSFET current with V_{COMP}. When the sensed current exceeds V_{COMP}, the comparator outputs low to turn off the HS-FET. The internal power MOSFET's maximum current is internally limited cycle by cycle.

Hiccup Protection

If the output is shorted to ground, causing V_{OUT} to drop below 70% of its nominal voltage, the IC shuts down momentarily and begins discharging C_{SS}. It restarts with a full SS when C_{SS} is fully discharged. This hiccup process repeats until the fault condition is removed.

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank any start-up glitches. When the SS block is enabled, it first holds V_{SS} low to ensure the remaining circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} going low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disabled.

Power Good (PG) Output

The MPQ4436A includes an open-drain power good (PG) output that indicates the output. A pull-up resistor connected to the power source is required if PG is used. If V_{OUT} is within 95% to 105% of the nominal voltage, the PG pin goes high. If V_{OUT} is above 106.5% or below 93.5% of the nominal voltage, PG goes low.

SYNCIN and SYNCO

f_{SW} can be synced to the rising edge of the clock signal applied at SYNCIN. The recommended SYNCIN frequency range is 350kHz to 1000kHz. Ensure that the SYNCIN off time is shorter than the internal oscillator period; otherwise the internal clock may turn on the HS-FET before the rising edge of SYNCIN. There is no other special limit on the pulse width of SYNCIN, but there is always parasitic capacitance of the pad. If the pulse width is too short, a clear rising and falling

edge may not be seen due to the parasitic capacitance. A pulse longer than 100ns is recommended in most application .

When applying SYNCIN in AAM mode, pull SYNCIN below its threshold (0.4V) or leave SYNCIN floating before the MPQ4436A starts up, and then adding external SYNCIN clock.

To avoid floating SYNCIN when using this function through an external clock, connect a resistor to GND. Considering SYNCIN's drive capability, it is recommended to use a 10kΩ to 51kΩ resistor.

The SYNCO pin provides a default 180° phase-shifted clock to the internal oscillator. If there is no external SYNCIN clock, then SYNCO provides a 180° phase-shifted clock that is compared to the internal clock. If there is an external SYNCIN clock, then SYNCO provides a 180° phase-shifted clock that is compared to the external SYNCIN clock.

APPLICATION INFORMATION

Setting the BST Capacitor

If using the MPQ4436A in CCM mode only, use a BST capacitor (C_{BST}) with a nominal capacitance of at least 0.2µF. If using AAM mode, the external C_{BST} should be greater than 0.2µF. Alternately, choose C_{BST} using Equation (2) and Equation (3):

$$C_{BST}(\mu F) \geq \frac{75 \times C_{OUT}(\mu F) \times 10^{-3}}{I_{MIN}(\mu A)} \quad (2)$$

$$C_{BST}(\mu F) \geq \frac{80}{I_{MIN}(\mu A) \times L(\mu H)} \quad (3)$$

If the calculated C_{BST} is greater than 6.8µF, contact an MPS FAE to verify the design.

Setting the VCC Capacitor

The VCC capacitor should be 10 times the value of the boost capacitor, and at least 4.7µF nominal. A VCC capacitor greater than 68µF nominal is not recommended.

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply AC current to the converter while maintaining the DC input voltage. For the best performance, use low-ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients.

For most applications, it is recommended to use a 4.7µF to 10µF capacitor. It is strongly recommended to use another, lower-value capacitor (e.g. 0.1µF) with a small package size (0603) to absorb high-frequency switching noise. Place the smaller capacitor as close to VIN and GND as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current (I_{CIN}) in the input capacitor can be estimated with Equation (4):

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, calculated with Equation (5):

$$I_{CIN} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple (ΔV_{IN}) caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (6)$$

Selecting the Output Capacitor

The output capacitor maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low-ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (7)$$

Where L is the inductance, and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes the majority of the output voltage ripple. For simplification, the output voltage ripple (ΔV_{OUT}) can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MPQ4436A can be optimized for a wide range of capacitance and ESR values.

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating at least 25% greater than the maximum load current is recommended for most applications. For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage; however, it also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance is to allow the inductor ripple current to be approximately 30% of the maximum load current. The inductance (L) can be calculated with Equation(10):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum peak inductor current (I_{LP}) can be calculated with Equation (11):

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

V_{IN} UVLO Setting

The MPQ4436A has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 3V, while the falling threshold is about 2.7V. For applications that require a higher UVLO point, an external resistor divider between VIN and EN can be used to achieve a higher equivalent UVLO threshold (see Figure 7).

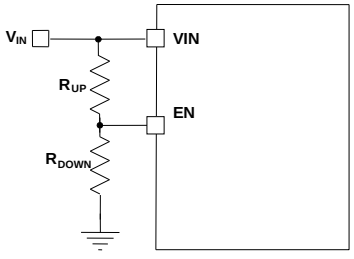


Figure 7: Adjustable UVLO Using EN Divider

The UVLO rising and falling thresholds can be calculated with Equation (12) and Equation (13), respectively:

$$V_{IN\_UVLO\_RISING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_RISING} \quad (12)$$

$$V_{IN\_UVLO\_FALLING} = (1 + \frac{R_{UP}}{R_{DOWN}}) \times V_{EN\_FALLING} \quad (13)$$

Where V_{EN_RISING} is 1V, and $V_{EN\_FALLING}$ is 0.85V.

External BST Diode and Resistor

An external BST diode can enhance the efficiency of the regulator when the duty cycle is high. A power supply between 2.5V and 5V can be used to power the external BST diode. V_{CC} or V_{OUT} is recommended to be this power supply in the circuit (see Figure 8).

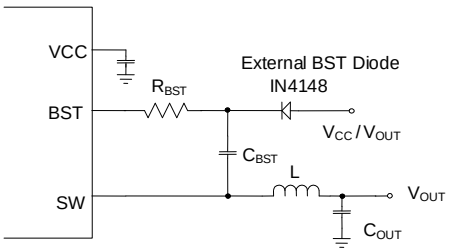


Figure 8: Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the recommended C_{BST} value is 0.1µF to 1µF. A resistor in series with C_{BST} (R_{BST}) can reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at a high V_{IN}. A higher resistance improves SW spike reduction but compromises efficiency. To make a tradeoff between EMI and efficiency, a ≤20Ω R_{BST} is recommended.

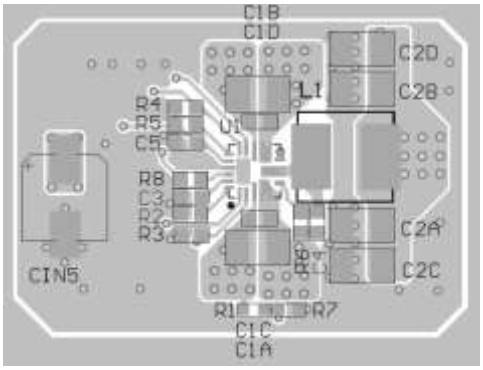
PCB Layout Guidelines [8]

Efficient PCB layout, especially input capacitor placement, is critical for stable operation. A 4-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 9 and follow the guidelines below:

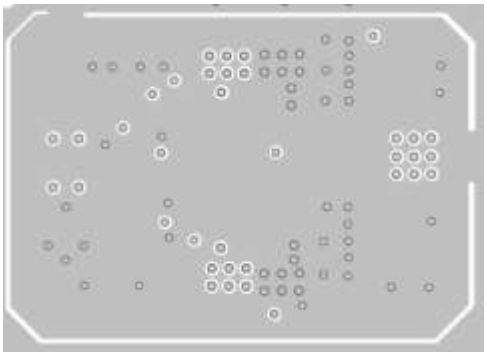
1. Place symmetric input capacitors as close to VIN and GND as possible.
2. Connect a large ground plane directly to PGND.
3. If the bottom layer is a ground plane, add vias near PGND.
4. Ensure that the high-current paths at GND and VIN have short, direct, and wide traces.
5. Place the ceramic input capacitor, especially the small package size (0603) input bypass capacitor, as close to VIN and PGND as possible to minimize high-frequency noise.
6. Keep the connection between the input capacitor and VIN as short and wide as possible.
7. Place the VCC capacitor as close to VCC and GND as possible.
8. Route SW and BST away from sensitive analog areas, such as FB.
9. Place the feedback resistors close to the chip to ensure the trace that connects to FB is as short as possible.
10. Use multiple vias to connect the power planes to the internal layers.

Note:

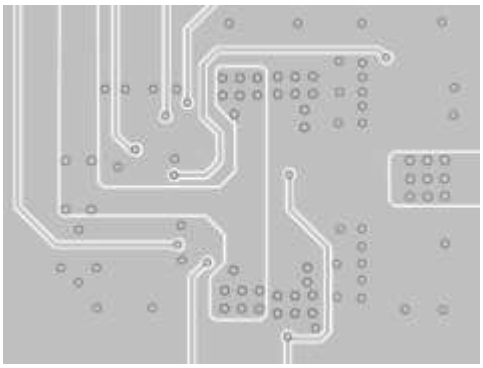
8) The recommended PCB layout is based on Figure 10 on page 35.



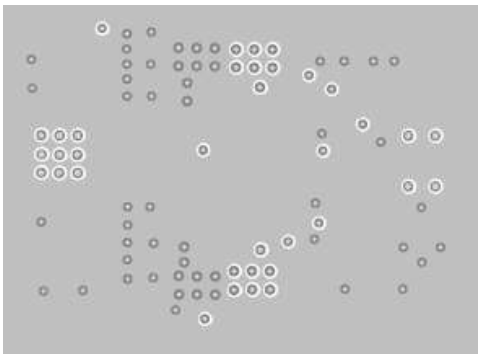
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 9: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

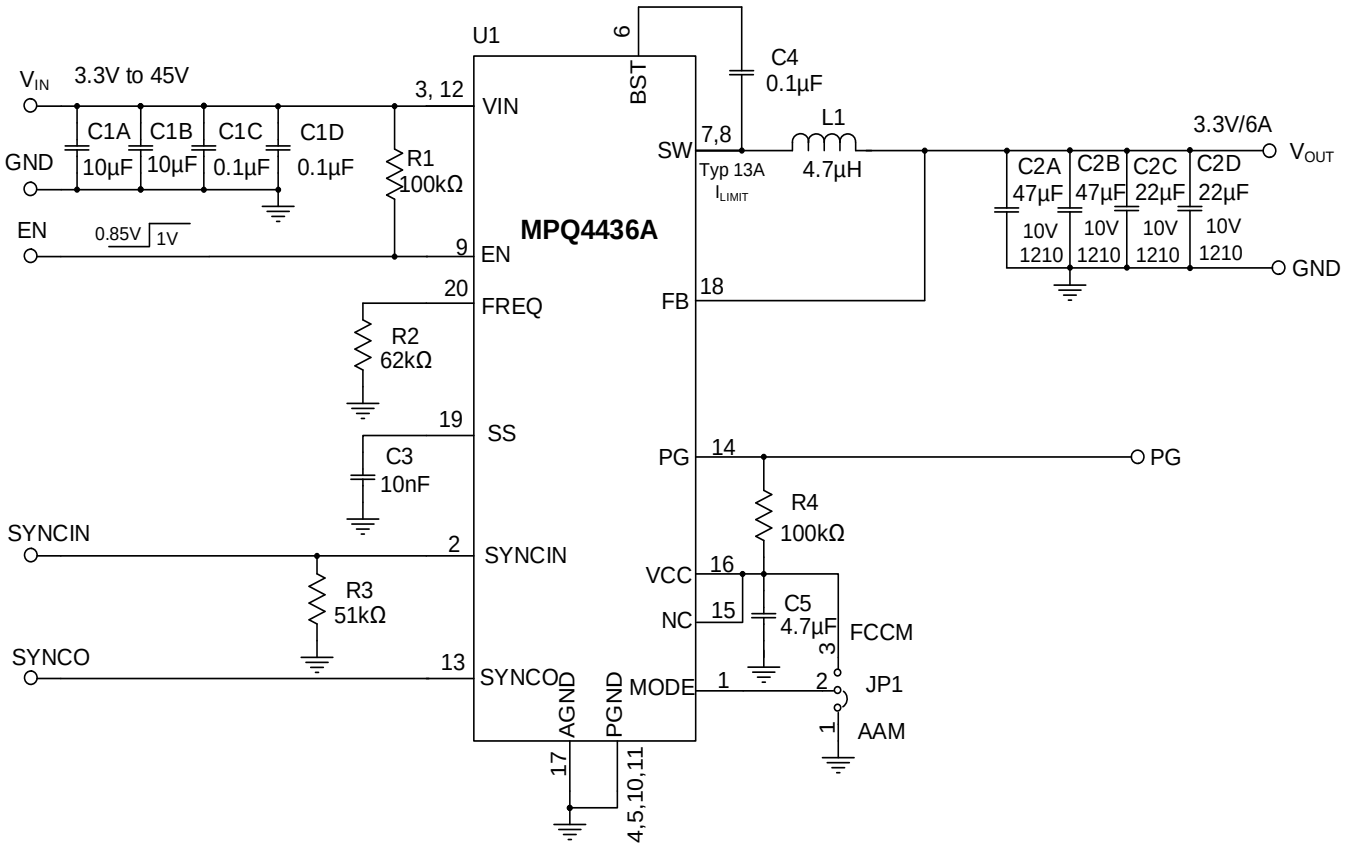


Figure 10: V_{OUT} = 3.3V, f_{SW} = 470kHz

TYPICAL APPLICATION CIRCUITS *(continued)*

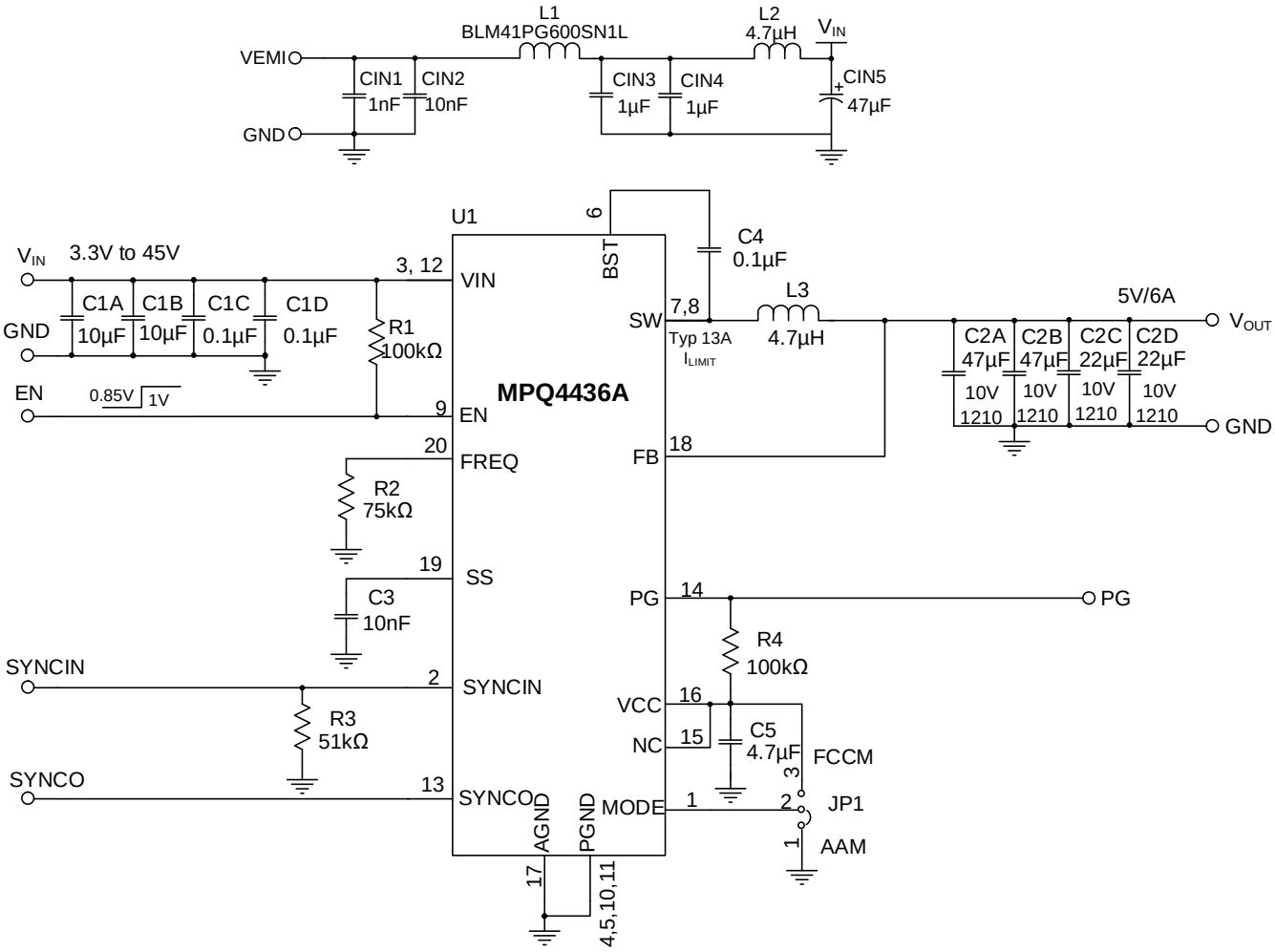
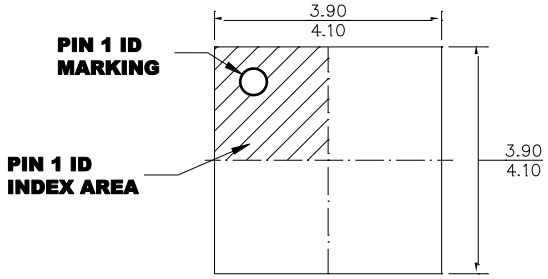


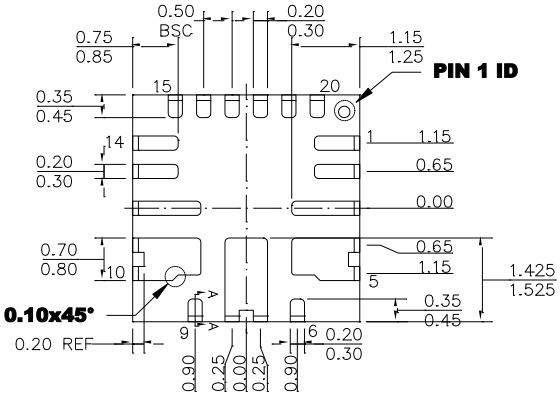
Figure 11: V_{OUT} = 5V, f_{SW} = 410kHz with EMI Filters

PACKAGE INFORMATION

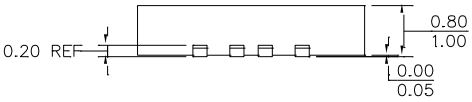
QFN-20 (4mmx4mm)
Wettable Flank



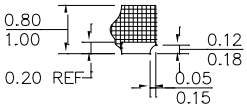
TOP VIEW



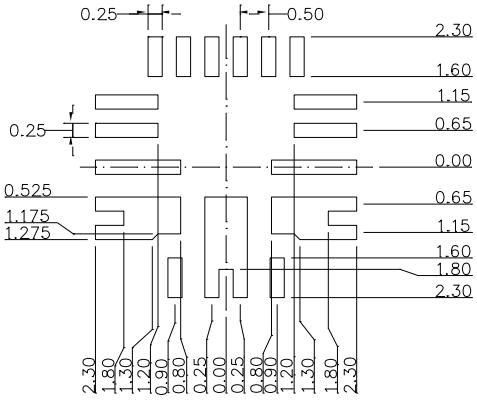
BOTTOM VIEW



SIDE VIEW



SECTION A-A

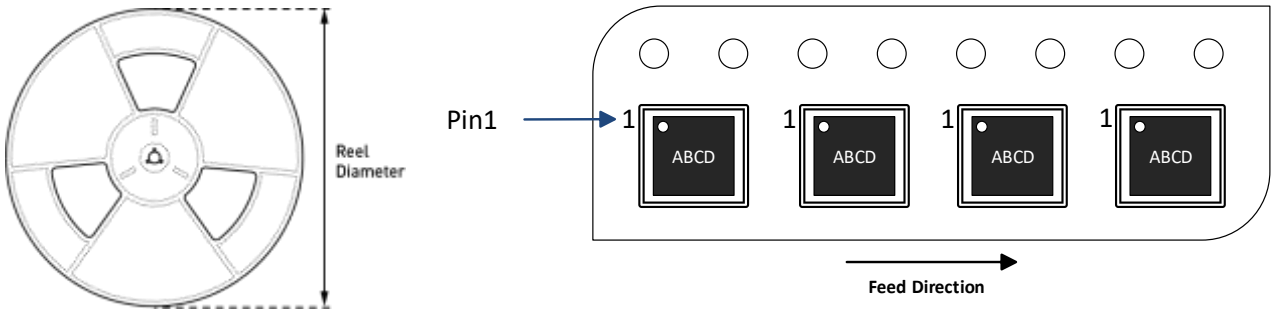


RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantiy/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPQ4436AGRE-33-AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm
MPQ4436AGRE-5-AEC1-Z	QFN-20 (4mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	1/26/2022	Initial Release	-