74HC4514; 74HCT4514

4-to-16 line decoder/demultiplexer with input latches

Rev. 6 — 5 August 2024 Product data sheet

1. General description

The 74HC4514; 74HCT4514 is a 4-to-16 line decoder/demultiplexer having four binary weighted address inputs (A0 to A3), with latches, a latch enable input (LE), an enable input ($\overline{E}$) and 16 outputs (Q0 to Q15). When LE is HIGH, the selected output is determined by the data on An. When LE goes LOW, the last data present at An are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input $\overline{E}$ does not affect the state of the latch. When the device is used as a demultiplexer, $\overline{E}$ is the data input and A0 to A3 are the address inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The 74HCT4514 features reduced input threshold levels to allow interfacing to TTL logic levels.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Input levels:
  - For 74HC4514: CMOS level
  - For 74HCT4514: TTL level
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4514PW 74HCT4514PW	−40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

5. Functional diagram

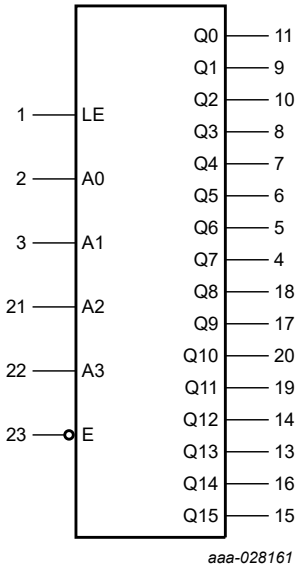


Fig. 1. Logic symbol

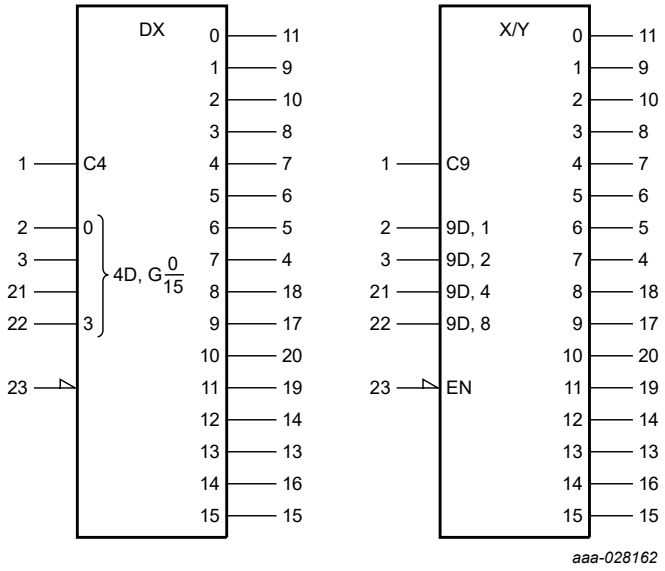


Fig. 2. IEC logic symbol

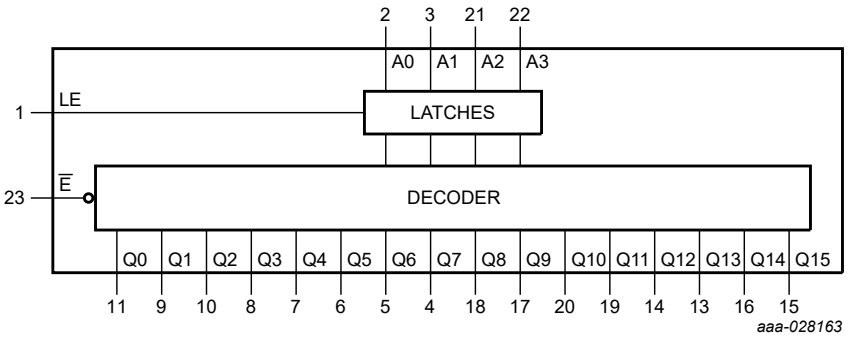


Fig. 3. Functional diagram

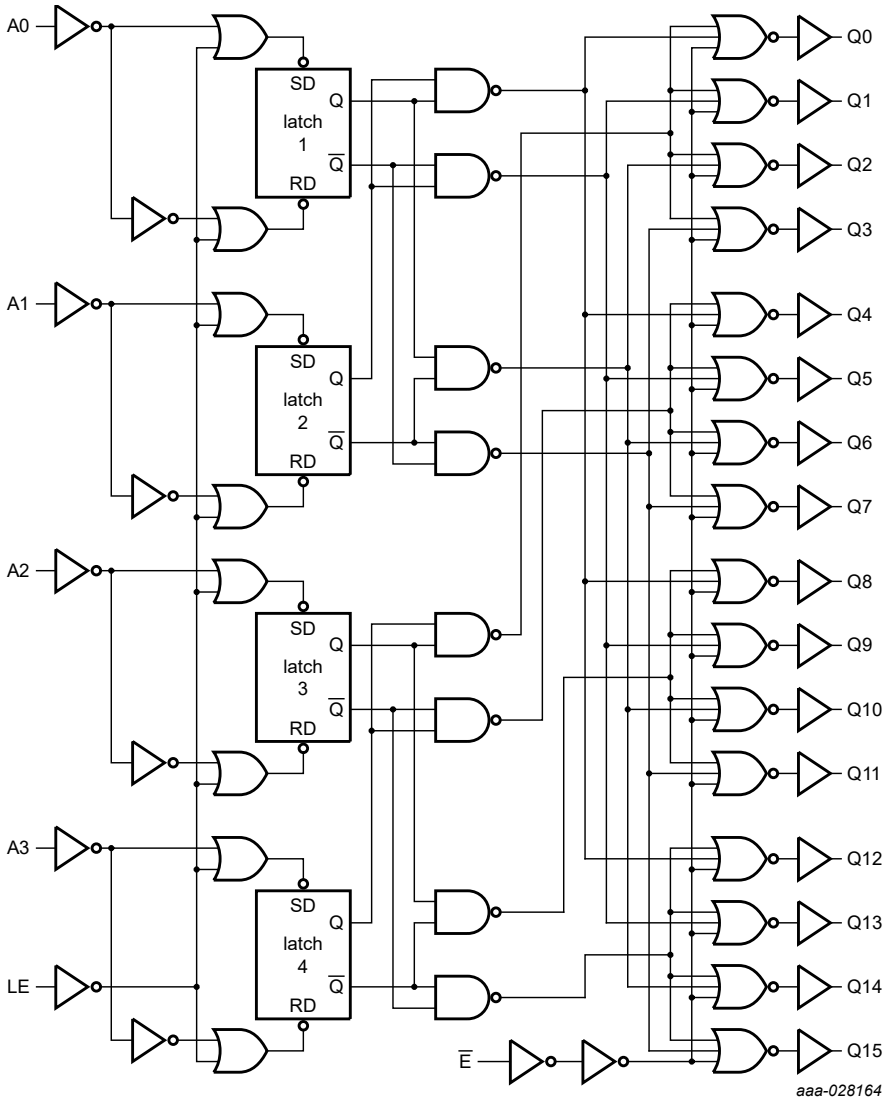
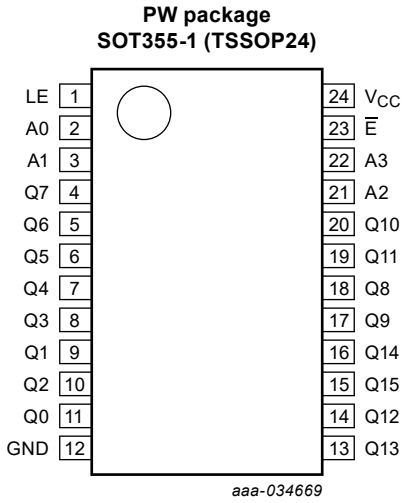


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
LE	1	latch enable input (active HIGH)
$\overline{E}$	23	enable input (active LOW)
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15	11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	multiplexer outputs (active HIGH)
A0, A1, A2, A3	2, 3, 21, 22	address inputs
GND	12	ground (0 V)
V_{CC}	24	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.
Input LE = HIGH.

Inputs					Outputs														
$\overline{E}$	A0	A1	A2	A3	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L
L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[1]	-	500	mW

[1] For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4514			74HCT4514			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	+25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4514										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	+25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4514										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A								
		An	-	65	234	-	292.5	-	318.5	µA
		LE	-	140	504	-	630	-	686	µA
		$\overline{E}$	-	100	360	-	450	-	490	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

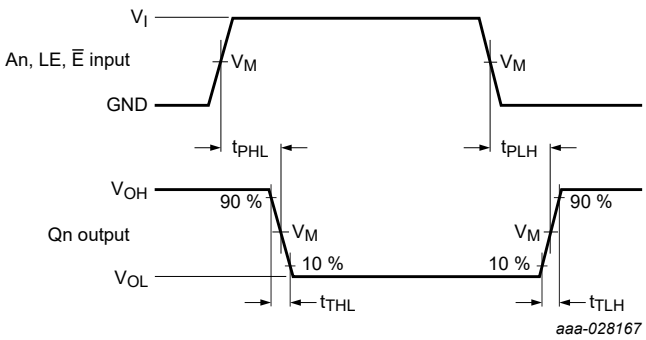
Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	+25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4514										
t_{pd}	propagation delay	An to Qn; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	74	230	-	290	-	345	ns
		V_{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		V_{CC} = 5 V; C_L = 15 pF	-	23	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	22	39	-	49	-	59	ns
		LE to Qn; see Fig. 5								
		V_{CC} = 2.0 V	-	74	230	-	290	-	345	ns
		V_{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		V_{CC} = 6.0 V	-	22	39	-	49	-	59	ns
		$\overline{E}$ to Qn; see Fig. 5								
		V_{CC} = 2.0 V	-	41	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	15	35	-	44	-	53	ns
		V_{CC} = 6.0 V	-	12	30	-	37	-	45	ns
t_t	transition time	Qn; see Fig. 5 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse witdh	LE HIGH; see Fig. 6								
		V_{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t_{su}	set-up time	An to LE; see Fig. 6								
		V_{CC} = 2.0 V	90	25	-	115	-	135	-	ns
		V_{CC} = 4.5 V	18	9	-	23	-	27	-	ns
		V_{CC} = 6.0 V	15	7	-	20	-	23	-	ns
t_h	hold time	An to LE; see Fig. 6								
		V_{CC} = 2.0 V	1	−11	-	1	-	1	-	ns
		V_{CC} = 4.5 V	1	−4	-	1	-	1	-	ns
		V_{CC} = 6.0 V	1	−3	-	1	-	1	-	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	44	-	-	-	-	-	pF

Symbol	Parameter	Conditions	+25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4514										
t_{pd}	propagation delay	An to Qn; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	30	55	-	69	-	83	ns
		V_{CC} = 5 V; C_L = 15 pF	-	26	-	-	-	-	-	ns
		LE to Qn; V_{CC} = 4.5 V; see Fig. 5	-	29	50	-	63	-	75	ns
		$\overline{E}$ to Qn; V_{CC} = 4.5 V; see Fig. 5	-	17	40	-	50	-	60	ns
t_t	transition time	Qn; V_{CC} = 4.5 V; see Fig. 5 [2]	-	7	15	-	19	-	22	ns
t_W	pulse witdh	LE HIGH; V_{CC} = 4.5 V; see Fig. 6	16	4	-	20	-	24	-	ns
t_{su}	set-up time	An to LE; V_{CC} = 4.5 V; see Fig. 6	18	9	-	23	-	27	-	ns
t_h	hold time	An to LE; V_{CC} = 4.5 V; see Fig. 6	3	−3	-	3	-	3	-	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} - 1.5 V [3]	-	45	-	-	-	-	-	pF

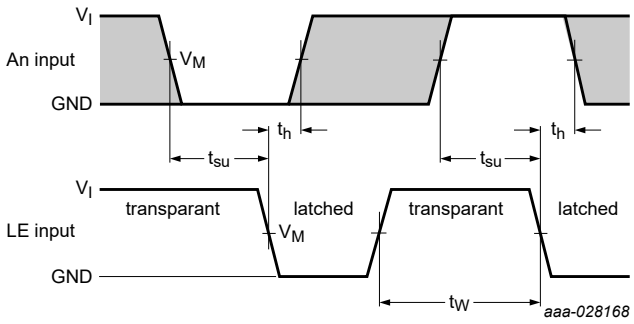
[1] t_{pd} is the same as t_{PLH} and t_{PHL}
[2] t_t is the same as t_{TLH} and t_{THL}
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of load switching outputs;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



Measurement points are given in Table 8.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The inputs (An, LE, $\overline{E}$) to output (Qn) propagation delays and the output transition times



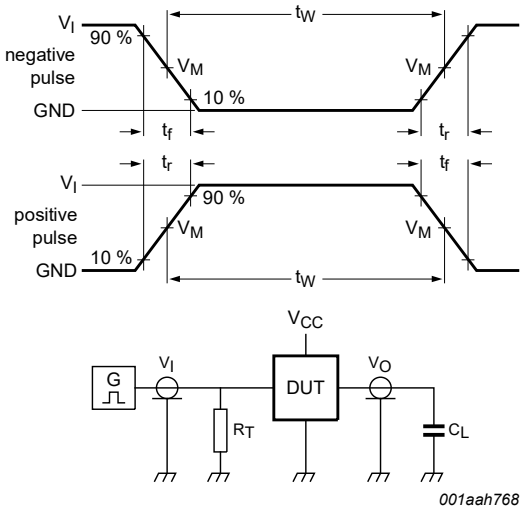
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Data set-up and hold times for An input to LE input and LE input pulse width

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC4514	GND to V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT4514	GND to 3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance; should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load
	V_I	t_r, t_f	C_L
74HC4514	GND to V_{CC}	6 ns	15 pF, 50 pF
74HCT4514	GND to 3 V	6 ns	15 pF, 50 pF

12. Application information

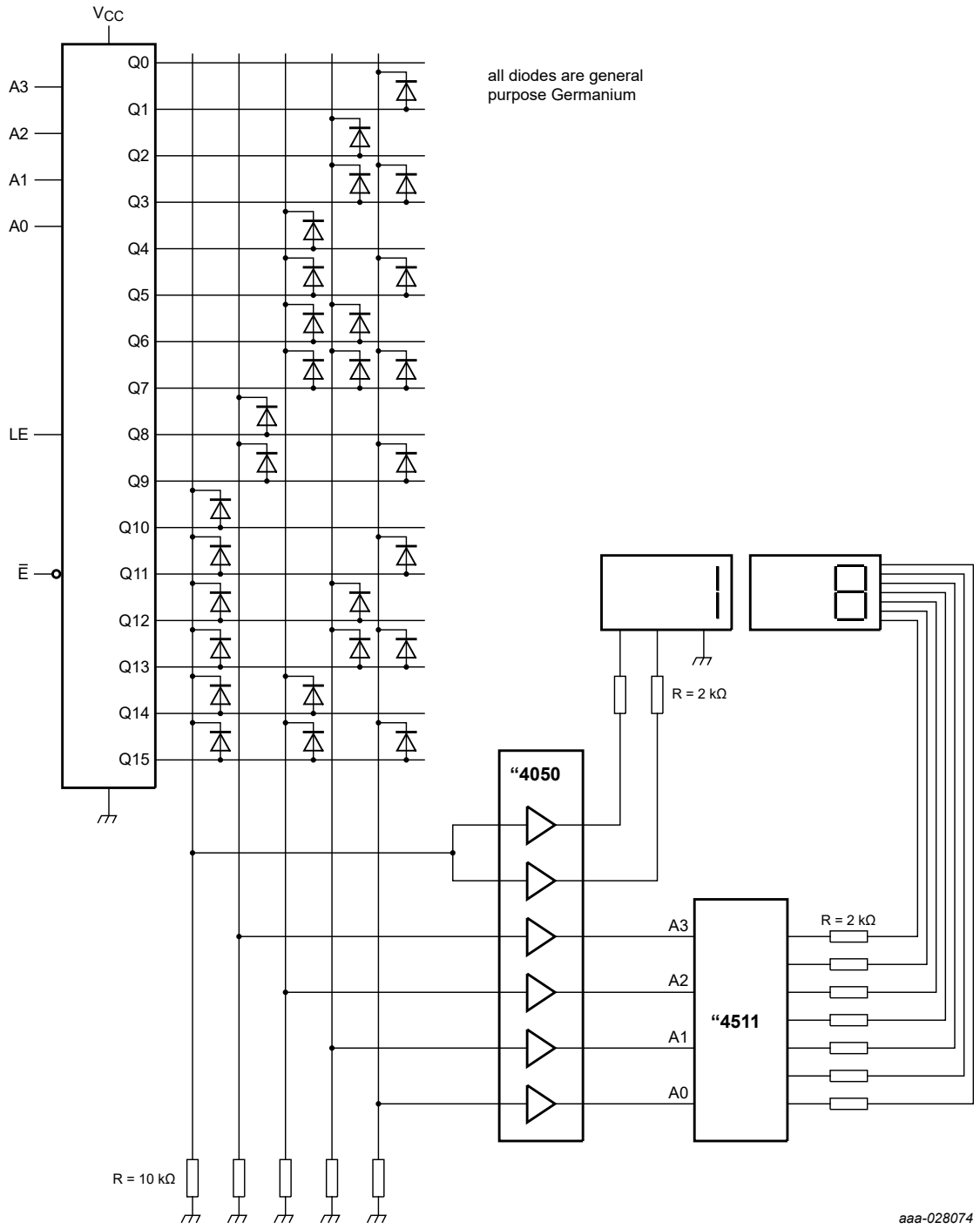
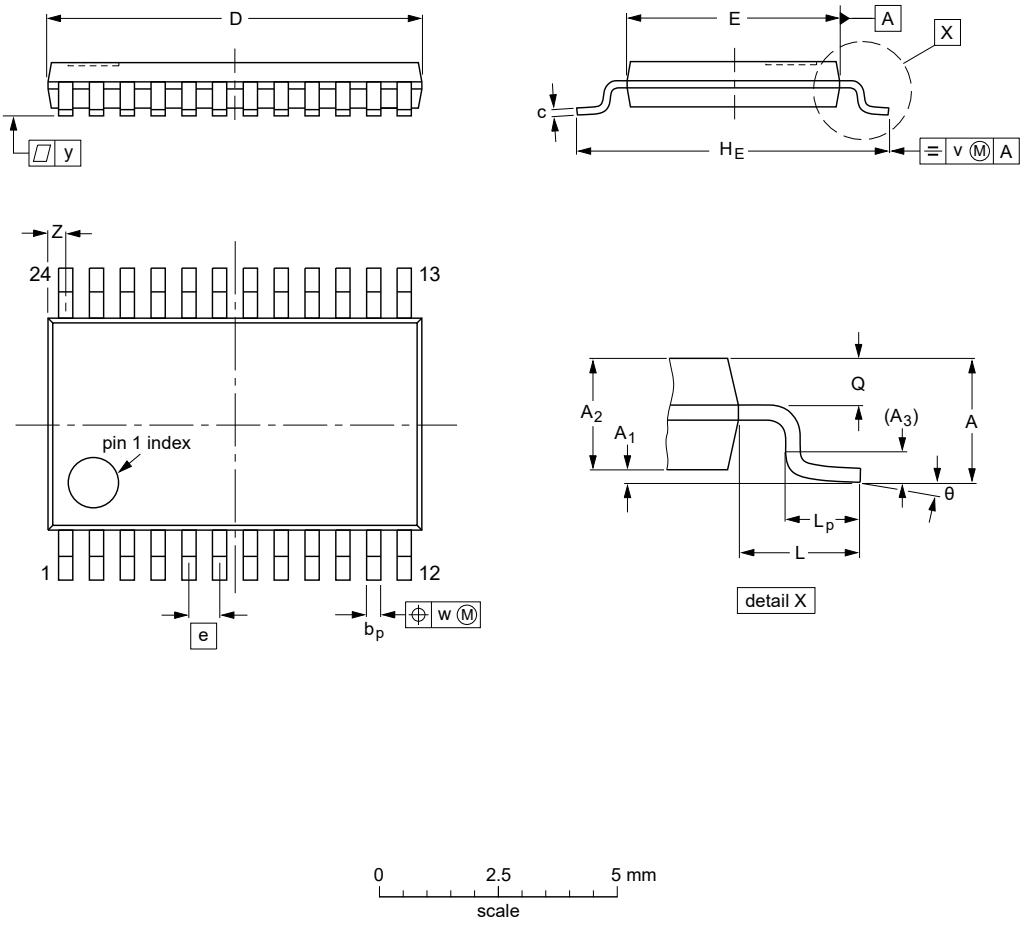


Fig. 8. Code-to-code conversion; hexadecimal to BCD

13. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 9. Package outline SOT355-1 (TSSOP24)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4514 v.6	20240805	Product data sheet	-	74HC_HCT4514 v.5
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT4514 v.5	20240507	Product data sheet	-	74HC_HCT4514 v.4
Modifications:	• Type number 74HCT4514D (SOT137-1/SO24) removed.			
74HC_HCT4514 v.4	20210715	Product data sheet	-	74HC_HCT4514 v.3
Modifications:	• Type number 74HC4514DB (SOT340-1/SSOP24) removed. • Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT4514 v.3	20180220	Product data sheet	-	74HC_HCT4514 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4514 v.2	19930901	Product specification	-	74HC_HCT4514 v.1

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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