UM11812

NXP GUI for FS26 Automotive PMIC Family

Rev. 2 — 22 March 2023

User manual

Document information

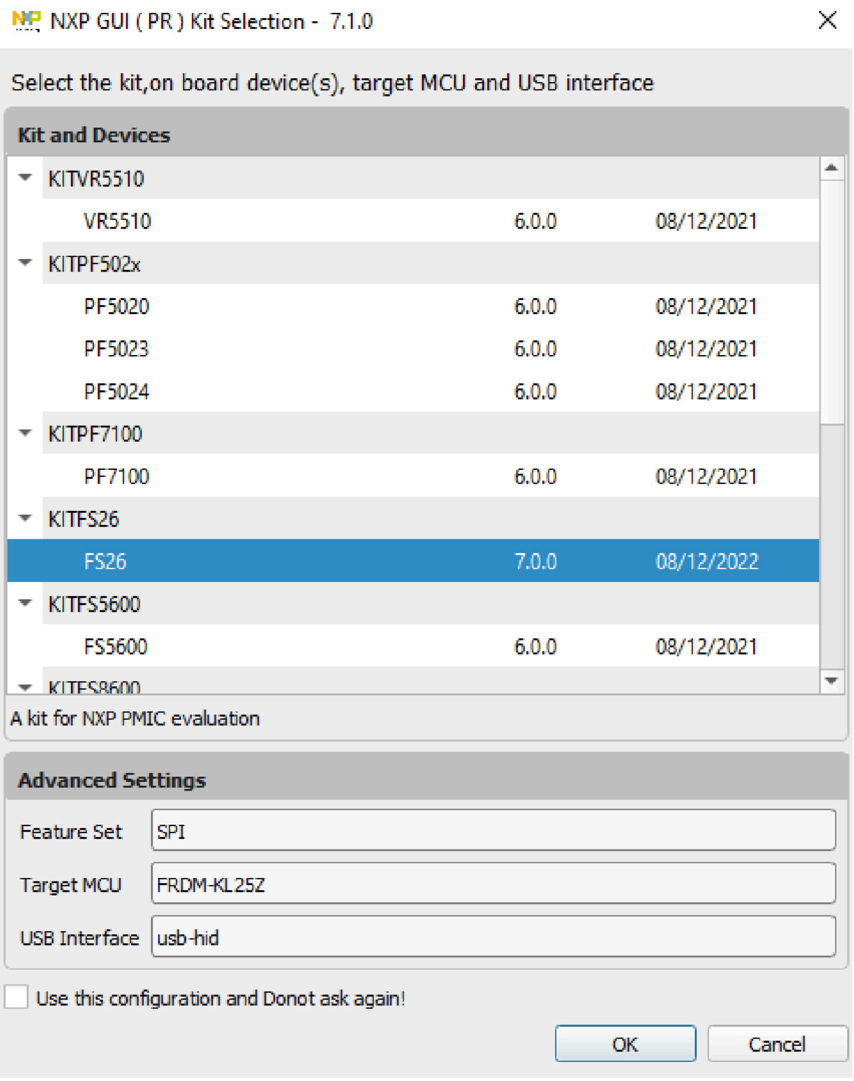
Information	Content
Keywords	NXP GUI automotive SBC families, FS2600 automotive SBC, fail-safe system, low power, ASIL D, SMPS, LDO
Abstract	This user guide describes the use of the NXP GUI for Automotive PMIC family in development using the FS2600 Automotive PMIC family, referred to hereafter as FS26. This document is intended for engineers involved in evaluation, design, implementation, and validation using the FS26 Fail-safe system basis chip with multiple SMPS and LDO.

1 Introduction

This user guide describes the use of the NXP GUI for Automotive PMIC Family in development using the FS2600 Automotive PMIC family, referred to hereafter as FS26. This document is intended for engineers involved in evaluation, design, implementation, and validation using the FS26 Fail-safe system basis chip with multiple SMPS and LDO.

The scope of this document is to provide the user with information to evaluate the FS26 Fail-safe system basis chip with multiple SMPS and LDO. This document covers connecting the hardware, installing the software and tools, configuring the environment, and using the evaluation boards.

The NXP GUI for Automotive PMIC Families enables development on the FS26 family of devices. This GUI allows the user to play with registers, try OTP configurations, and burn the part.



Select the kit,on board device(s), target MCU and USB interface

Kit and Devices

KITVR5510		
VR5510	6.0.0	08/12/2021
KITPF502x		
PF5020	6.0.0	08/12/2021
PF5023	6.0.0	08/12/2021
PF5024	6.0.0	08/12/2021
KITPF7100		
PF7100	6.0.0	08/12/2021
KITFS26		
FS26	7.0.0	08/12/2022
KITFS5600		
FS5600	6.0.0	08/12/2021
KITFS8600		

A kit for NXP PMIC evaluation

Advanced Settings

Feature Set: SPI

Target MCU: FRDM-KL25Z

USB Interface: usb-hid

☐ Use this configuration and Donot ask again!

aaa-050352

Figure 1. NXP GUI for FS26 Automotive PMIC family

2 Finding resources and information on the NXP website

NXP Semiconductors provides online resources for this GUI and its supported devices on http://www.nxp.com.

The information page for NXP GUI for Automotive PMIC Families is at http://www.nxp.com/NXP GUI for Automotive PMIC Families. The information page provides overview information, documentation, downloads, and development tools.

2.1 Collaborate in the NXP community

The NXP community is for sharing ideas and tips, asking and answering technical questions, and receiving input on just about any embedded design topic.

The NXP community is at http://community.nxp.com.

3 FS2600: safety system basis chip with low power for ASIL D / ASIL B

3.1 General description

Devices in the FS26 automotive safety System Basis Chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety, and low-end gateway technology.

This family of devices consists of several versions that are pin to pin and software compatible. These versions support a wide range of applications with automotive safety integrity levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power up sequencing, and integrated system level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs, and communication interfaces. It offers a high-precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionalities for system control and diagnostics, including an analog multiplexer, general-purpose inputs/ outputs (GPIOs), and selectable wake-up events from I/O, long duration timer (LDT), or serial-peripheral interface (SPI) communication.

The FS26 is developed in compliance with the ISO2 6262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.

3.2 Features and benefits

3.2.1 Operating range

- 40 V DC maximum input voltage
- Supports operating voltage range down to battery 3.2 V with VBST
- Supports operating voltage range down to battery 6 V without VBST
- Low Power OFF mode with 30 µA quiescent current
- Low Power Standby mode with 29 µA quiescent current with VPRE active
  - LDO1 or LDO2 activation selectable via OTP configuration
  - GPIO1 or GPIO2 activation selectable via SPI communication

All information provided in this document is subject to legal disclaimers.

3.2.2 Power supplies

- VPRE: synchronous buck converter with integrated FETs
  - Configurable output voltage and switching frequency
  - Output DC current capability up to 1.5 A
  - PFM mode for Low Power Standby mode operation
- VCORE: synchronous buck converter with integrated FETs
  - VCORE is dedicated for microcontroller core supply
  - Output DC current up to 0.8 A or 1.65 A (depending on part number)
  - Output voltage range setting from 0.8 V to 3.35 V
- VBST: asynchronous boost controller with external low-side switch, diode, and current sense resistor
  - VBST is configurable as front-end supply to withstand low-voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability
- VREF: High-precision reference voltage with 0.75 % accuracy for external ADC reference and internal tracking reference
- TRK1and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2, or internal LDO reference. Supports high-voltage protection for ECU off board operation. Each tracker has a current capability up to 150 mA

3.2.3 System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIOs with wake-up capability or HS/LS driver
- Programmable LDT for system shutdown and wake-up control
- Monitoring of system voltages (including battery voltage monitoring) through the analog multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT or SPI activity
- Device control via 32-bit SPI interface with cyclic redundancy checks (CRC)

3.2.4 Compliancy

- Electromagnetic compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control, and manual frequency tuning
- Electromagnetic interference (EMI) robustness supporting various automotive EMI test standards

3.2.5 Functional safety

- Scalable portfolio from ASIL B to D
- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple, or challenger Watchdog function
- Analog built-in self-test (ABIST) and logical built-in self-test (LBIST) at startup
- Analog built-in self-test (ABIST) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

3.2.6 Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via one time programmable (OTP) fuse memory
- OTP emulation mode for hardware development and evaluation
- Debug mode for software development, MCU programming, and debugging

4 Getting ready

Working with the FS26 requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

4.1 Development board and accessories

The development boards (with accessories) are available on the NXP website. Three different boards are available:

- Programming socket board: KITFS26SKTEVM
  - Available on https://www.nxp.com/KITFS26SKTEVM
- Automotive evaluation board: KITFS26AEEVM
  - Available on https://www.nxp.com/KITFS26AEEVM

4.2 Additional hardware

In addition to the development board, the following hardware is necessary or beneficial when working with this kit.

- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A.

4.3 Windows PC workstation

The software requires a Windows PC workstation. Meeting these minimum specifications produces great results when working with this evaluation board.

- USB-enabled computer with Windows 7 or Windows 10

4.4 Software

The software must be installed before working with the NXP GUI and the evaluation boards. All listed software is available on the NXP GUI information page at http://www.nxp.com/NXP GUI for Automotive PMIC Families or from our 'Secure Files' portal at https://www.nxp.com/mynxp/secure-files.

4.5 Configuring the hardware for startup

The development board setup must be completed before using the NXP GUI. This setup is described in the “Configuring the hardware for startup” section in the dedicated user manual available for each board kit:

- Programming socket board: KITFS26SKTEVM
  - Available on https://www.nxp.com/KITFS26SKTEVM
- Automotive evaluation board: KITFS26AEEVM
  - Available on https://www.nxp.com/KITFS26AEEVM

5 Installing and configuring software and tools

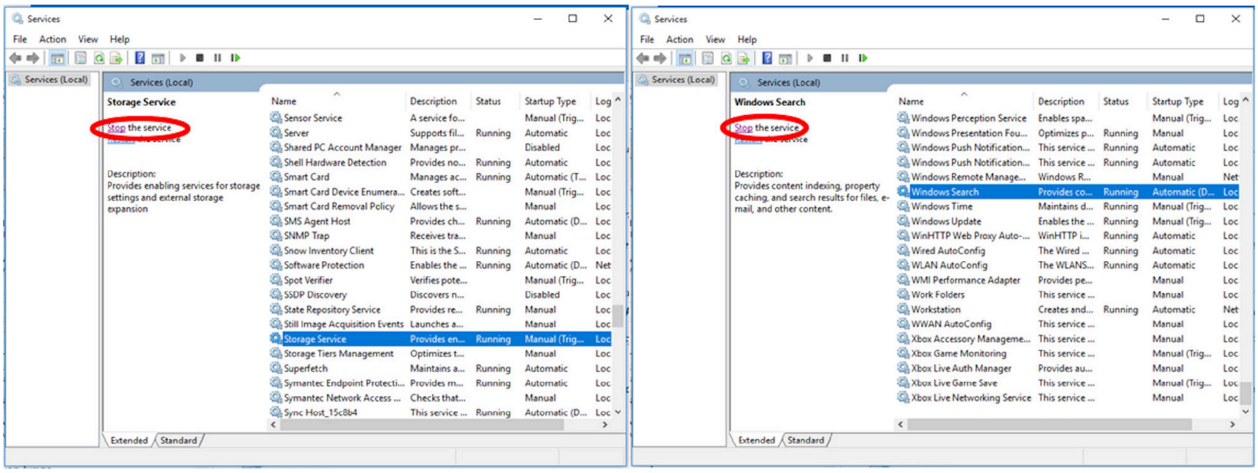
The programming/evaluation boards are always delivered with the GUI firmware already flashed. If the MCU firmware is already flashed, this section can be ignored. If it is specified that the firmware must be updated, or if it is malfunctioning, follow these instructions.

5.1 Flashing or updating the GUI firmware

5.1.1 Flashing the Freedom board firmware on Windows 7/10

If BOOTLOADER is already loaded in the FRDM Board, steps 1 and 2 are not required. Start from step 3.

1. Disable the Storage Service and Windows Search: Run Services, double-click, and stop them as shown in Figure 2.



Storage Service

Stop the service

Description:
Provides enabling services for storage settings and external storage expansion

Name	Description	Status	Startup Type	Log
Sensor Service	A service fo...		Manual (Trig...	Loc
Server	Supports fil...	Running	Automatic	Loc
Shared PC Account Manager	Manages pr...		Disabled	Loc
Shell Hardware Detection	Provides no...	Running	Automatic	Loc
Smart Card	Manages ac...	Running	Automatic (T...	Loc
Smart Card Device Enumera...	Creates soft...		Manual (Trig...	Loc
Smart Card Removal Policy	Allows the s...		Manual	Loc
SMS Agent Host	Provides ch...	Running	Automatic (D...	Loc
SNMP Trap	Receives tra...		Manual	Loc
Snow Inventory Client	This is the S...	Running	Automatic	Loc
Software Protection	Enables the ...	Running	Automatic (D...	Net
Spot Verifier	Verifies pote...		Manual (Trig...	Loc
SSDP Discovery	Discovers n...		Disabled	Loc
State Repository Service	Provides re...	Running	Manual	Loc
Still Image Acquisition Events	Launches a...		Manual	Loc
Storage Service	Provides en...	Running	Manual (Trig...	Loc
Storage Tiers Management	Optimizes t...		Manual	Loc
Superfetch	Maintains a...	Running	Automatic	Loc
Symantec Endpoint Protecti...	Provides m...	Running	Automatic	Loc
Symantec Network Access ...	Checks that...		Manual	Loc
Sync Host_15c8b4	This service ...	Running	Automatic (D...	Loc

Windows Search

Stop the service

Description:
Provides content indexing, property caching, and search results for files, e-mail, and other content.

Name	Description	Status	Startup Type	Log
Windows Perception Service	Enables spa...		Manual (Trig...	Loc
Windows Presentation Fou...	Optimizes p...	Running	Manual	Loc
Windows Push Notification...	This service ...	Running	Automatic	Loc
Windows Push Notification...	This service ...	Running	Automatic	Loc
Windows Remote Manage...	Windows R...		Manual	Net
Windows Search	Provides co...	Running	Automatic (D...	Loc
Windows Time	Maintains d...	Running	Manual (Trig...	Loc
Windows Update	Enables the ...	Running	Manual (Trig...	Loc
WinHTTP Web Proxy Auto-...	WinHTTP i...	Running	Automatic	Loc
Wired AutoConfig	The Wired ...	Running	Automatic	Loc
WLAN AutoConfig	The WLANS...	Running	Automatic	Loc
WMI Performance Adapter	Provides pe...		Manual	Loc
Work Folders	This service ...		Manual	Loc
Workstation	Creates and...	Running	Automatic	Net
WWAN AutoConfig	This service ...		Manual	Loc
Xbox Accessory Manageme...	This service ...		Manual	Loc
Xbox Game Monitoring	This service ...		Manual (Trig...	Loc
Xbox Live Auth Manager	Provides au...		Manual	Loc
Xbox Live Game Save	This service ...		Manual (Trig...	Loc
Xbox Live Networking Service	This service ...		Manual	Loc

aaa-044226

Figure 2. Services configuration

2. Press the RST button and connect the USB cable to the SDA port on the Freedom Board.
   - A new BOOTLOADER device appears on the left pane of the File Explorer.
3. Drag and drop the file “MSD-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA” to the BOOTLOADER drive. Ensure there is enough time for the firmware to be saved in the BOOTLOADER.
4. Disconnect the USB cable, then reconnect it to the SDA port.
   - This time WITHOUT pressing the RST button, the FRDM_KL25Z device appears on the left pane of the File Explorer as pictured in Figure 3.

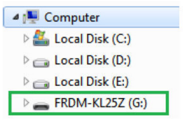


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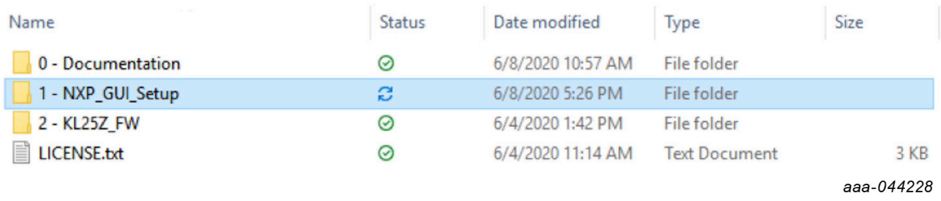
Figure 3. FRDM-KL25Z in left pane

5. Locate the file “nxp-gui-fw-frdmkl25z-usb_hid-device_version.bin” from the package. Drag and drop this file into the FRDM_KL25Z device.
   Ensure that there is enough time for the firmware to be saved.
6. The Freedom board firmware is successfully loaded. Disconnect the USB-cable and reconnect it to the KL25Z USB port.

5.2 Installing the NXP GUI software package

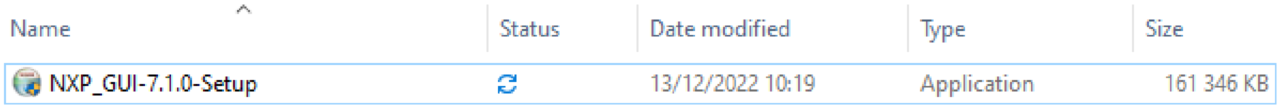
To install the FS2600 NXP GUI, download or obtain the NXP GUI package, unzip an open 1-NXP_GUI_Setup folder:



Name	Status	Date modified	Type	Size
0 - Documentation	✓	6/8/2020 10:57 AM	File folder	
1 - NXP_GUI_Setup	⟳	6/8/2020 5:26 PM	File folder	
2 - KL25Z_FW	✓	6/4/2020 1:42 PM	File folder	
LICENSE.txt	✓	6/4/2020 11:14 AM	Text Document	3 KB

Figure 4. NXP_GUI_Setup folder

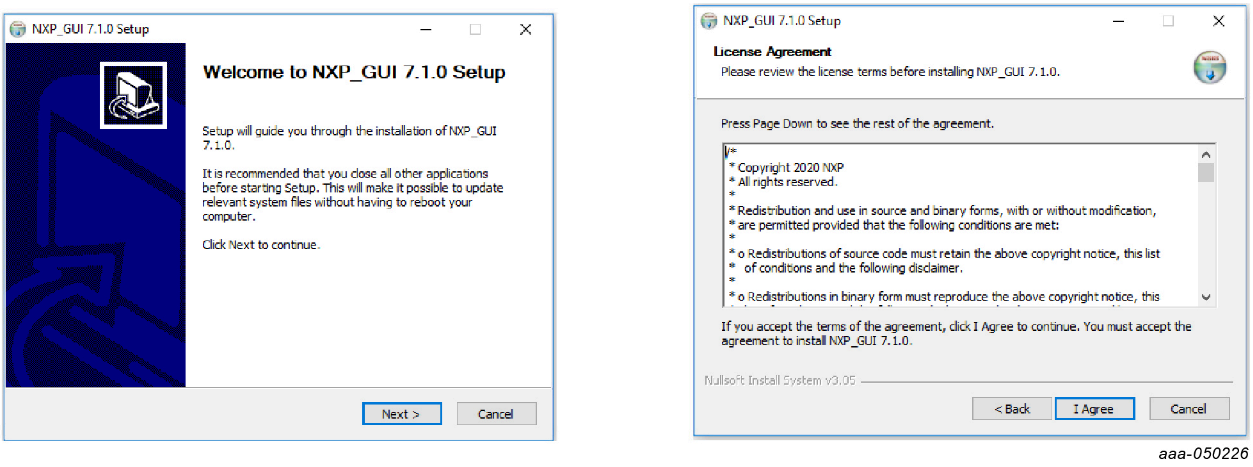
Then double-click on the NXP_GUI_version-Setup.exe and follow the instructions.



Name	Status	Date modified	Type	Size
NXP_GUI-7.1.0-Setup	⟳	13/12/2022 10:19	Application	161 346 KB

Figure 5. NXP_GUI_version_Setup.exe

To install the application on a Windows PC, proceed with the following pop-up windows:



NXP_GUI 7.1.0 Setup

Welcome to NXP_GUI 7.1.0 Setup

Setup will guide you through the installation of NXP_GUI 7.1.0.

It is recommended that you close all other applications before starting Setup. This will make it possible to update relevant system files without having to reboot your computer.

Click Next to continue.

NXP_GUI 7.1.0 Setup

License Agreement

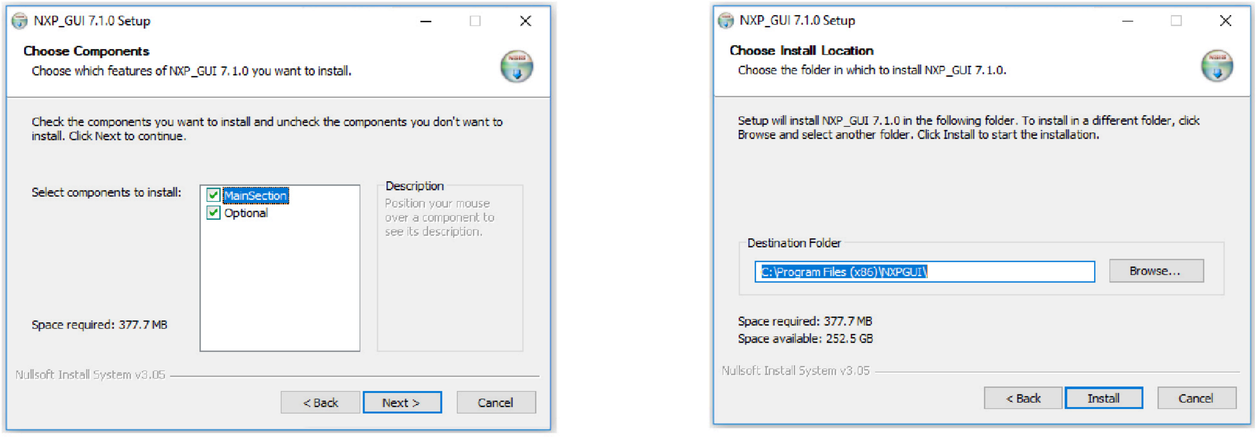
Please review the license terms before installing NXP_GUI 7.1.0.

Press Page Down to see the rest of the agreement.

```
/*
 * Copyright 2020 NXP
 * All rights reserved.
 *
 * Redistribution and use in source and binary forms, with or without modification,
 * are permitted provided that the following conditions are met:
 *
 * o Redistributions of source code must retain the above copyright notice, this list
 *   of conditions and the following disclaimer.
 *
 * o Redistributions in binary form must reproduce the above copyright notice, this
```

If you accept the terms of the agreement, click I Agree to continue. You must accept the agreement to install NXP_GUI 7.1.0.

Figure 6. NXP GUI setup



NXP_GUI 7.1.0 Setup

Choose Components

Choose which features of NXP_GUI 7.1.0 you want to install.

Check the components you want to install and uncheck the components you don't want to install. Click Next to continue.

Select components to install:

☑ MainSection

☑ Optional

Description

Position your mouse over a component to see its description.

Space required: 377.7 MB

Nullsoft Install System v3.05

NXP_GUI 7.1.0 Setup

Choose Install Location

Choose the folder in which to install NXP_GUI 7.1.0.

Setup will install NXP_GUI 7.1.0 in the following folder. To install in a different folder, click Browse and select another folder. Click Install to start the installation.

Destination Folder

C:\Program Files (x86)\NXPGUI\

Space required: 377.7 MB

Space available: 252.5 GB

Nullsoft Install System v3.05

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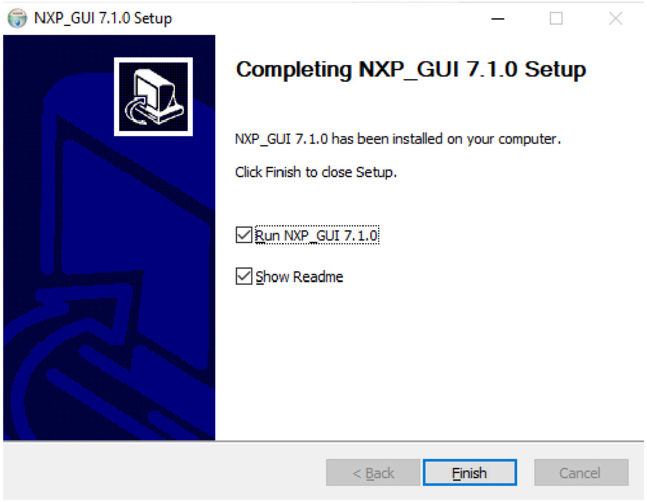
Figure 7. NXP GUI setup configuration

Select the following options before completing the installation of the setup:

- Run NXP_GUI
- Show Readme



NXP_GUI 7.1.0 Setup

Completing NXP_GUI 7.1.0 Setup

NXP_GUI 7.1.0 has been installed on your computer.

Click Finish to close Setup.

☑ Run NXP_GUI 7.1.0

☑ Show Readme

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Figure 8. NXP GUI setup completion

Select **Finish** to complete the installation.

When the installation is finished, find the application by searching for *NXPGUI* in the Windows search bar. Click to launch.

6 Configuring the hardware

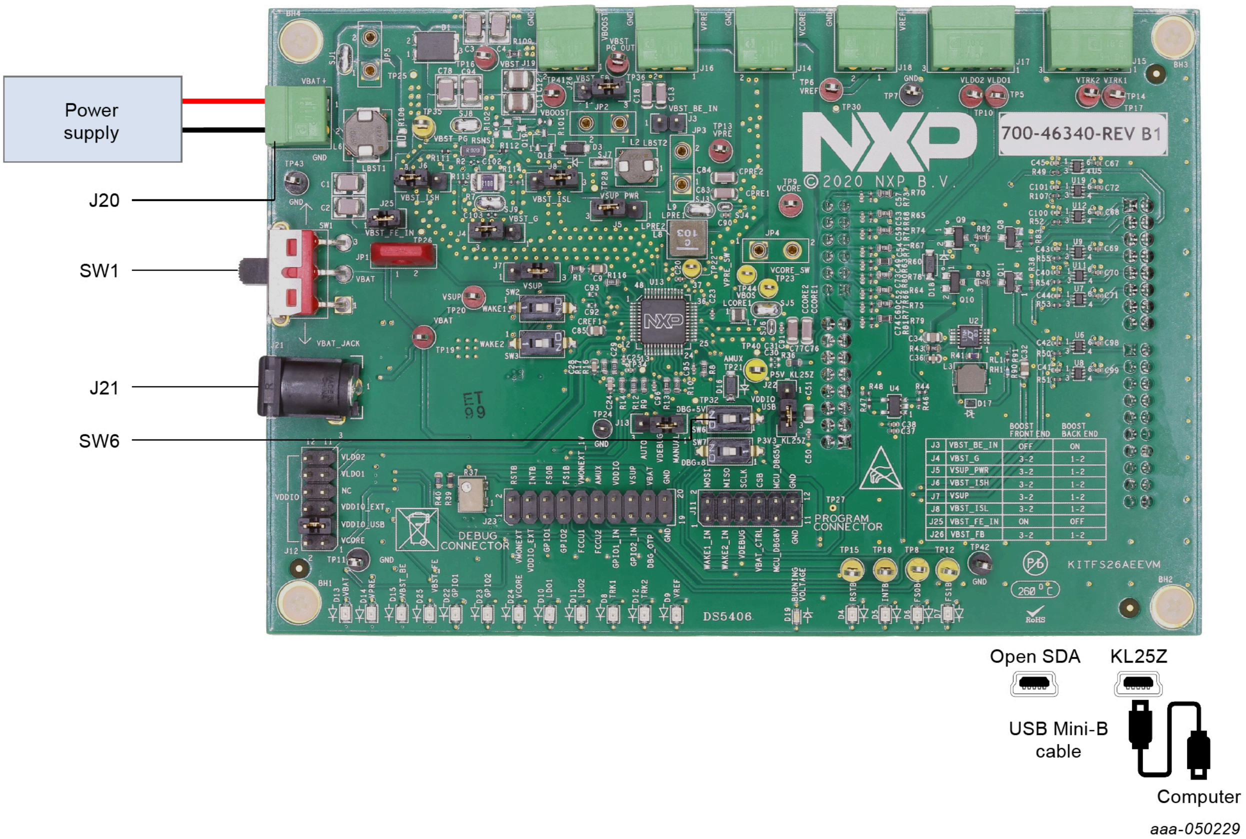


Figure 9. Device programming

To configure the hardware and workstation, complete the following procedure:

1. With SW1 in the middle position, set the DC power supply to 12 V and the current limit to 1.0 A. Attach the DC power supply positive and negative outputs to KITFS26AEEVM VBAT Phoenix connector (J20), or connect the 12 V power supply to VBAT Jack (J2).

Table 1. VBAT Phoenix connector (J20)

Schematic label	Signal name	Description
J20-1	VBAT	Battery voltage supply input
J20-2	GND	Ground

Table 2. VBAT three position connector (SW1)

Schematic label	Signal name	Description
SW1pin 2-3	VBAT Phoenix	Board supplied by Phoenix connector
SW1pin 2 (middle position)	VBAT	Board not supplied
SW1pin 2-1	VBAT jack	Board supplied by jack connector

2. Connect the Windows PC USB port to the KL25Z USB side of the Freedom board included in the kit, using the provided USB 2.0 cable.

3. Turn on SW6 to apply V_{DBG} to the DEBUG pin or SW7 to apply V_{OTP}.
4. Turn on the power supply.
5. Close SW1.

Note: *At this step, the product is either in Debug mode, and all regulators are turned OFF, or in OTP emulation mode. In the latter, the user can then power up with a preloaded OTP configuration or manually configure the mirror registers before powering up (the power up is effective as soon as SW7 is turned off).*

7 Using the FS2600 NXP GUI

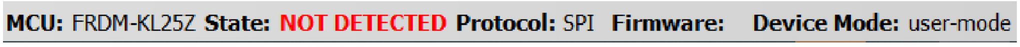
To follow the steps in this section, ensure the board is connected using the appropriate hardware configuration (see the board user information in UM11503 and UM11504).

Always use the latest version of the NXP GUI.

7.1 Establishing the connection between the NXP GUI and the hardware

The device manager allows the connection of the FS26 development board with the NXP GUI.

Before plugging the KL25Z USB port USB to the computer, the MCU is in a “NOT DETECTED” state.

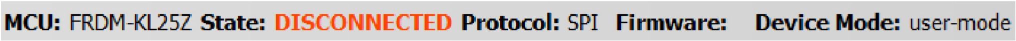


MCU: FRDM-KL25Z **State:** NOT DETECTED **Protocol:** SPI **Firmware:** **Device Mode:** user-mode

aaa-050262

Figure 10. MCU state is NOT DETECTED

After plugging in the USB, the MCU state changes to “DISCONNECTED”. **If the state does not change, press the RST button on the Freedom board.**

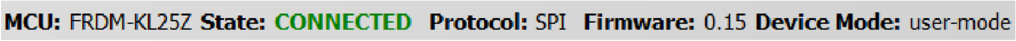


MCU: FRDM-KL25Z **State:** DISCONNECTED **Protocol:** SPI **Firmware:** **Device Mode:** user-mode

aaa-050263

Figure 11. MCU state is DISCONNECTED

In this state, the communication with the MCU can be started.



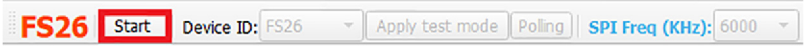
MCU: FRDM-KL25Z **State:** CONNECTED **Protocol:** SPI **Firmware:** 0.15 **Device Mode:** user-mode

aaa-050264

Figure 12. MCU state is CONNECTED

The MCU state changes to “CONNECTED” and the firmware version is displayed.

To start the communication with the FS2600, click the **Start** button.



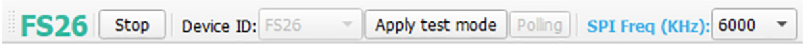
Device ID: FS26

SPI Freq (KHz): 6000

aaa-046877

Figure 13. Click Start button

When the communication has started successfully, the FS2600 switches to Green.



Device ID: FS26

SPI Freq (KHz): 6000

aaa-046878

Figure 14. FS26 is now green

When the device starts with the DEBUG pin voltage at V_{OTP} (on the EVBs: SW7 ON, DBG jumper populated, OTP mode led ON), the state machine stops at the M/FS_STATES: 4-Debug entry state.

The current mode can be read at the bottom of the GUI window and is automatically refreshed when transitioning to another state. Also, it is possible to manually refresh when clicking the current status button.

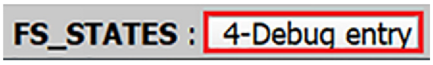


Figure 15. Current mode

The user can click **Apply test mode** to send Main and Fail-safe test mode entry keys. If test mode is entered correctly, button changes to **Exit test mode**.

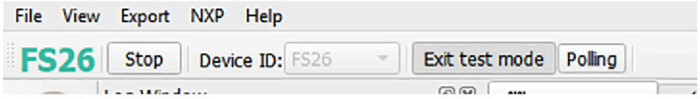


Figure 16. Button changes to Exit test mode

When test mode is entered, options requiring test mode are enabled, such as Mirrors and device programming.

Click **Polling** to do a continuous check of test mode entry.

If the device versioning bits are already programmed with an existing part number, the NXP GUI decodes and displays the assigned Device ID. The following example displays FS2633D.

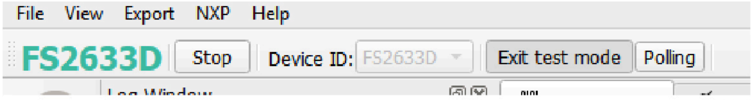
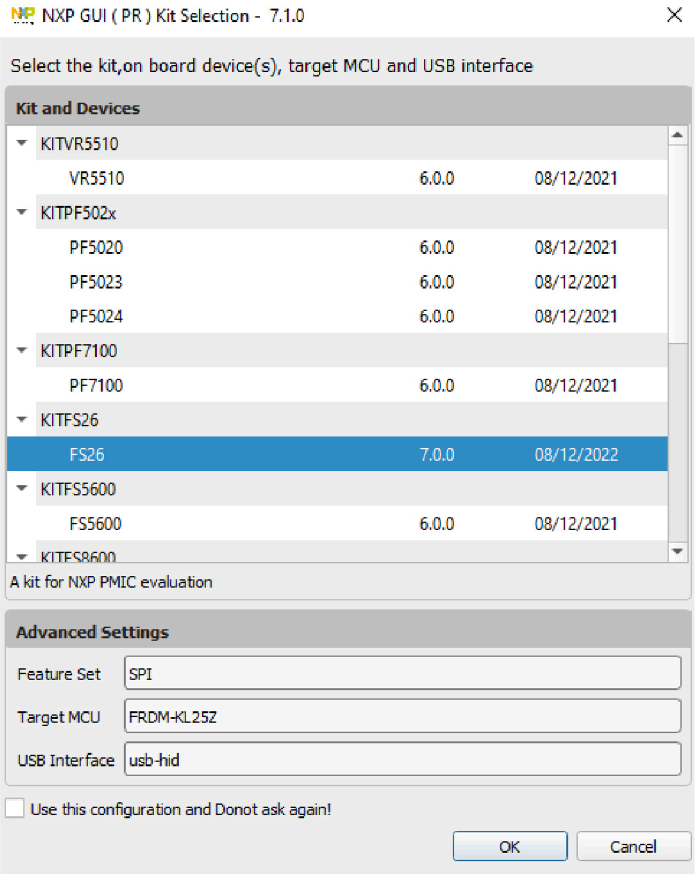


Figure 17. Device ID display

7.2 Starting the FS2600 NXP GUI

When the kit is ready and the NXP GUI is installed, click to launch the kit from the Windows search bar.



NXP GUI (PR) Kit Selection - 7.1.0

Select the kit,on board device(s), target MCU and USB interface

Kit and Devices

KITVR5510		
VR5510	6.0.0	08/12/2021
KITPF502x		
PF5020	6.0.0	08/12/2021
PF5023	6.0.0	08/12/2021
PF5024	6.0.0	08/12/2021
KITPF7100		
PF7100	6.0.0	08/12/2021
KITFS26		
FS26	7.0.0	08/12/2022
KITFS5600		
FS5600	6.0.0	08/12/2021
KITFS8600		

A kit for NXP PMIC evaluation

Advanced Settings

Feature Set: SPI

Target MCU: FRDM-KL25Z

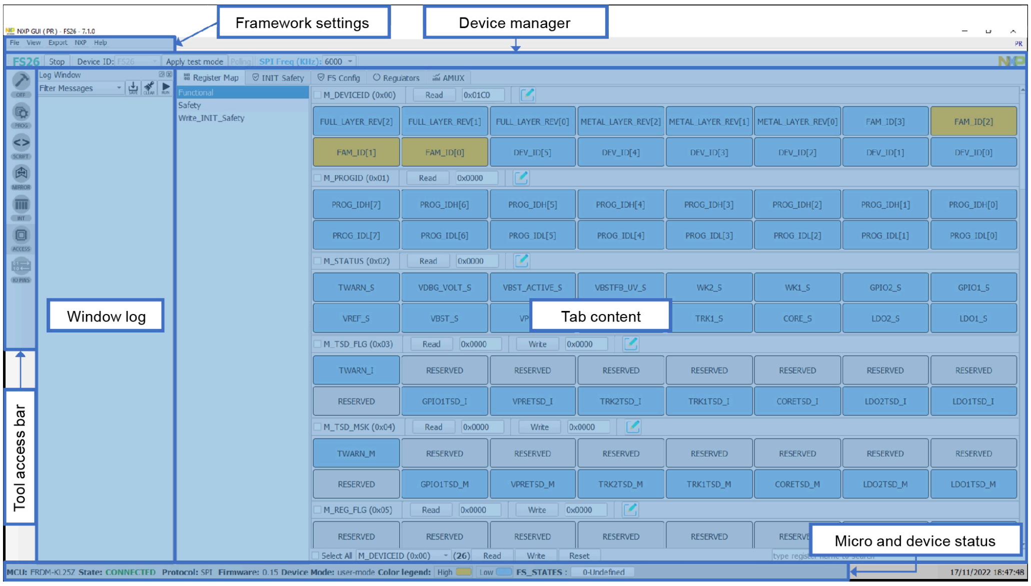
USB Interface: usb-hid

☐ Use this configuration and Donot ask again!

aaa-050230

Figure 18. KIT selection window

To avoid the kit selection window on every launch, check the “Use this configuration and do not ask again” box. The window shown in Figure 19 opens.



MCU: FRDM-KL25Z State: CONNECTED Protocol: SPI Firmware: 0.15 Device Mode: user-mode Color legend: High Low FS_STATES : 0-Undefined 17/11/2022 18:47:48

aaa-050231

Figure 19. NXP GUI framework

The FS2600 GUI interface is now in use. It can be divided in several parts:

- **Settings:** Import or export files; configure framework
- **Device Manager:** Start communication with device; enter or exit test mode; SPI communication settings
- **Tool Access Bar:** Quick access to the FS2600 evaluation tools and features
- **Window Log:** Microcontroller and device communication events
- **Tab Content:** Content of each tool or tab – there can be more tabs, boxes, or windows
- **Micro and Device Status:** Displays whether USB or device is connected or disconnected; displays Firmware and GUI version; displays the current state of the FS state machine – click **Display** button to refresh

Note: *The tool access bar shows the GUI tools in the sequence they must be used. The first step is to verify device POWER dissipation and then configure the OTP. When the power is verified and OTP is done, the device can be programmed or emulated with a SCRIPT. MIRROR registers can be read/modified to a configuration validation. To verify states and configure safety reactions, the Access tab allows manipulation of the registers.*

7.2.1 Framework settings

The NXP GUI main menu has five GUI elements: File, View, Export, NXP, and Help.

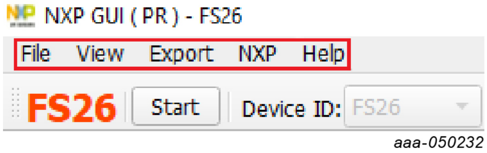


Figure 20. Framework settings

7.2.1.1 File

Load or save a configuration or exit the application. Load and save are only enabled when OTP tool tab is active.

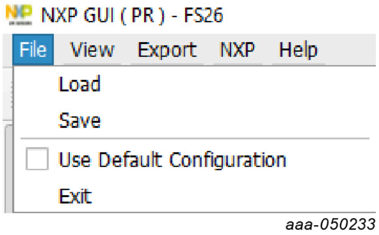


Figure 21. File options

- **Load**: Loads an existing configuration file previously exported from OTP tool, to continue to modify it on the OTP tool. This file has a .cfg extension. It is identified as: FS26_ProgIDASILlevel_CONFIG.cfg. Example: FS26_A0D_CONFIG.cfg.
- **Save**: Saves the current configuration of the OTP tool as a .cfg file.
- **Use default configuration**: Loads default values into the OTP tool.
- **Exit**: Exits NXP GUI application.

7.2.1.2 View

This main menu has options related to the GUI display.

- Display
- Show
- Naming Conventions

Display: It consists of the Connection Tool Bar (enabled by default) option. To show or hide, go to **View** → **Display** and then select **Connection Tool Bar**.

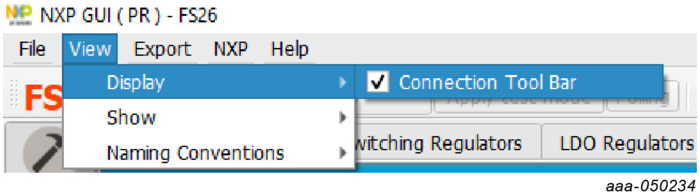


Figure 22. Display options

Show: This option can be used to access various sections of the GUI.

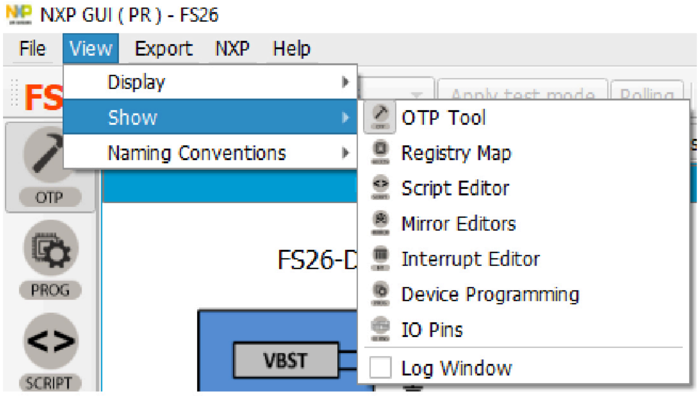


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Figure 23. Show options

Naming Conventions: Select Friendly or Register name display for the OTP tool. This option is enabled only when the OTP tool is active.

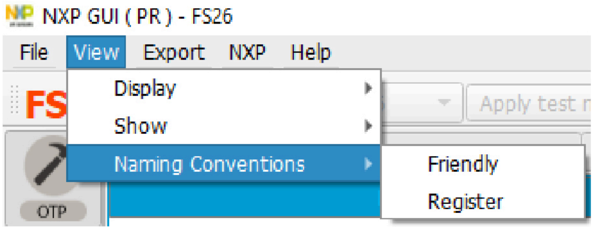

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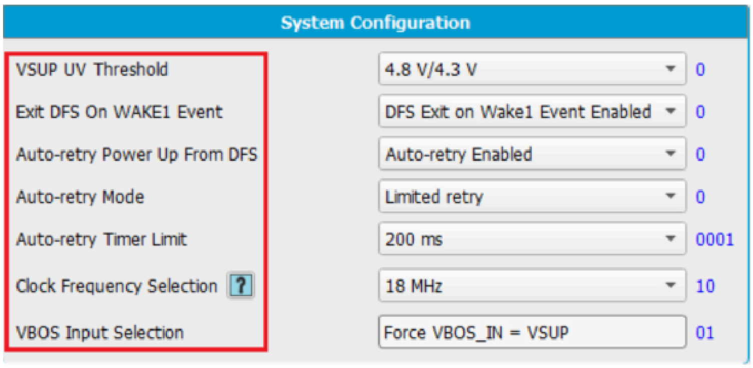
Figure 24. Naming conventions options

Friendly: Go to View → Naming Conventions → Friendly. This mode helps to view the the registers names as user-friendly names throughout the OTP tool.



System Configuration

VSUP UV Threshold	4.8 V/4.3 V	0
Exit DFS On WAKE1 Event	DFS Exit on Wake1 Event Enabled	0
Auto-retry Power Up From DFS	Auto-retry Enabled	0
Auto-retry Mode	Limited retry	0
Auto-retry Timer Limit	200 ms	0001
Clock Frequency Selection ?	18 MHz	10
VBOS Input Selection	Force VBOS_IN = VSUP	01

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Figure 25. Friendly mode

Register: Go to View → Naming Conventions → Register. This mode helps to view the register names as the registers' technical names throughout the OTP Tool.

Example: VSUP UV threshold → VSUP_UVTH_OTP

7.2.1.3 Export

This option allows the user to export the current OTP from the OTP tool into different script formats.

- **OTP**: Exports OTP configuration into OTP script file for programming
- **TBB**: Exports OTP configuration into a TBB script file for emulation
- **I-HEX**: Exports to Intel Hex script file
- **S-HEX**: Exports to Simple Hex script file.

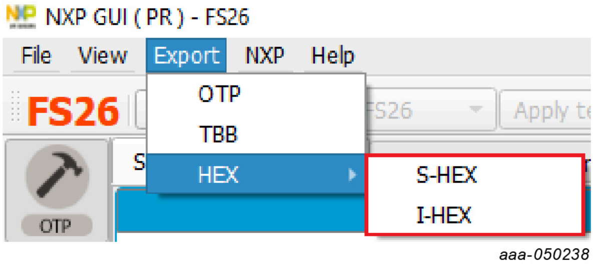


Figure 26. KIT selection window

This option is enabled only in the OTP Tool, and remains disabled in other sections of the GUI.

7.3 OTP tab

The OTP tool allows the configuration of OTP registers and generates scripts for OTP emulation or OTP programming. These scripts program parameters that the main state machine and the fail-safe state machine control.

The OTP tool includes four tabs:

- System Configuration
- Switching and LDO Regulators
- Voltage Monitoring
- System Safety Configuration
- OTP ID

These five tabs are used to define the entire FS26 OTP configuration.

When the OTP configuration is defined, TBB/OTP scripts can be generated using the *Export* menu. Generate a TBB file for emulation and an OTP file for OTP programming.

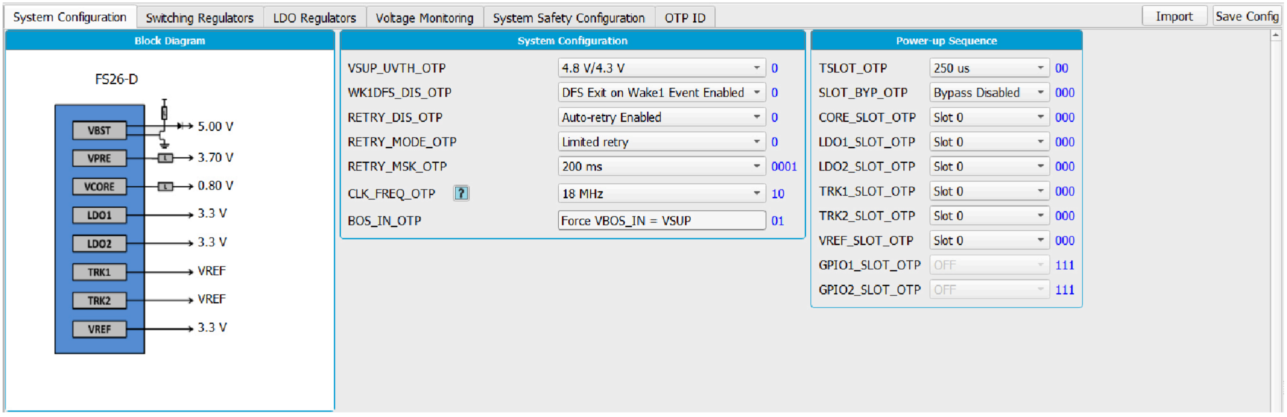
It is possible to save a configuration to use or to modify it later. To export the OTP configuration, click **Save Config**. To import a configuration initially saved from the OTP tool or the Mirrors tab, click the **Import** button.

7.3.1 System Configuration tab

The system configuration tab has several sections:

- **Block Diagram**: This graphic shows the output voltage set for each supply rail (VBST, VPRE, VCORE ...).
- **System Configuration**: Clock frequency, VSUP undervoltage threshold, auto retry ...
- **Power-up Sequence**: This box is used to define the power sequence of the device – if the configuration is modified, the Sequence Diagram is updated automatically.
- **I/O Configuration**: This last box is used to configure the four I/Os available on the FS2600 (GPIO1, GPIO2, WAKE1, and WAKE2).
- **Sequence Diagram**: This diagram reflects the power-up sequence of the FS2600 depending on the OTP configuration – the power-up sequence timing may not be 100 % accurate.

Figure 27 shows an OTP configuration example.



System Configuration

VSUP_UVTH_OTP	4.8 V/4.3 V	0
WK1DFS_DIS_OTP	DFS Exit on Wake1 Event Enabled	0
RETRY_DIS_OTP	Auto-retry Enabled	0
RETRY_MODE_OTP	Limited retry	0
RETRY_MSK_OTP	200 ms	0001
CLK_FREQ_OTP ?	18 MHz	10
BOS_IN_OTP	Force VBOS_IN = VSUP	01

Power-up Sequence

TSLOT_OTP	250 us	00
SLOT_BYP_OTP	Bypass Disabled	000
CORE_SLOT_OTP	Slot 0	000
LDO1_SLOT_OTP	Slot 0	000
LDO2_SLOT_OTP	Slot 0	000
TRK1_SLOT_OTP	Slot 0	000
TRK2_SLOT_OTP	Slot 0	000
VREF_SLOT_OTP	Slot 0	000
GPIO1_SLOT_OTP	OFF	111
GPIO2_SLOT_OTP	OFF	111

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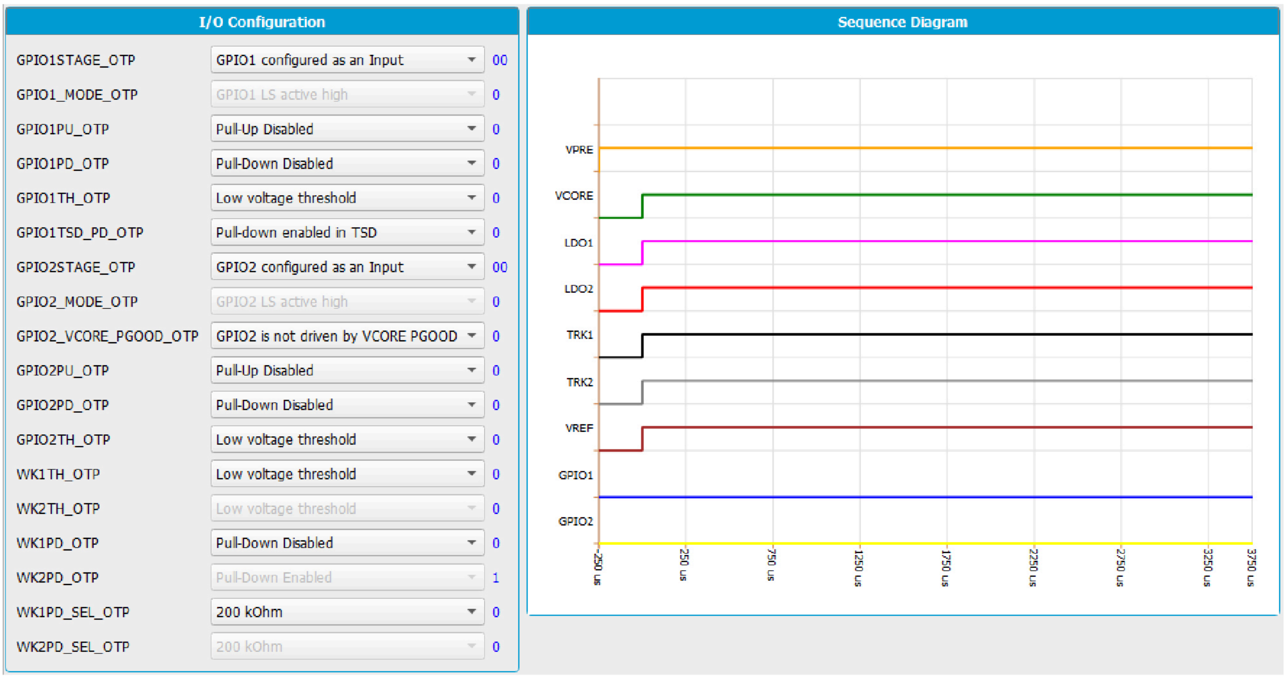
Figure 27. OTP System Configuration Tab, part 1 of 2: Block Diagram, System, and Power-up Sequence configurations

Figure 28 shows a voltage monitoring recap connection and the resulting power-up sequence diagram.



I/O Configuration

GPIO1STAGE_OTP	GPIO1 configured as an Input	00
GPIO1_MODE_OTP	GPIO1 LS active high	0
GPIO1PU_OTP	Pull-Up Disabled	0
GPIO1PD_OTP	Pull-Down Disabled	0
GPIO1TH_OTP	Low voltage threshold	0
GPIO1TSD_PD_OTP	Pull-down enabled in TSD	0
GPIO2STAGE_OTP	GPIO2 configured as an Input	00
GPIO2_MODE_OTP	GPIO2 LS active high	0
GPIO2_VCORE_PGOOD_OTP	GPIO2 is not driven by VCORE PGOOD	0
GPIO2PU_OTP	Pull-Up Disabled	0
GPIO2PD_OTP	Pull-Down Disabled	0
GPIO2TH_OTP	Low voltage threshold	0
WK1TH_OTP	Low voltage threshold	0
WK2TH_OTP	Low voltage threshold	0
WK1PD_OTP	Pull-Down Disabled	0
WK2PD_OTP	Pull-Down Enabled	1
WK1PD_SEL_OTP	200 kOhm	0
WK2PD_SEL_OTP	200 kOhm	0

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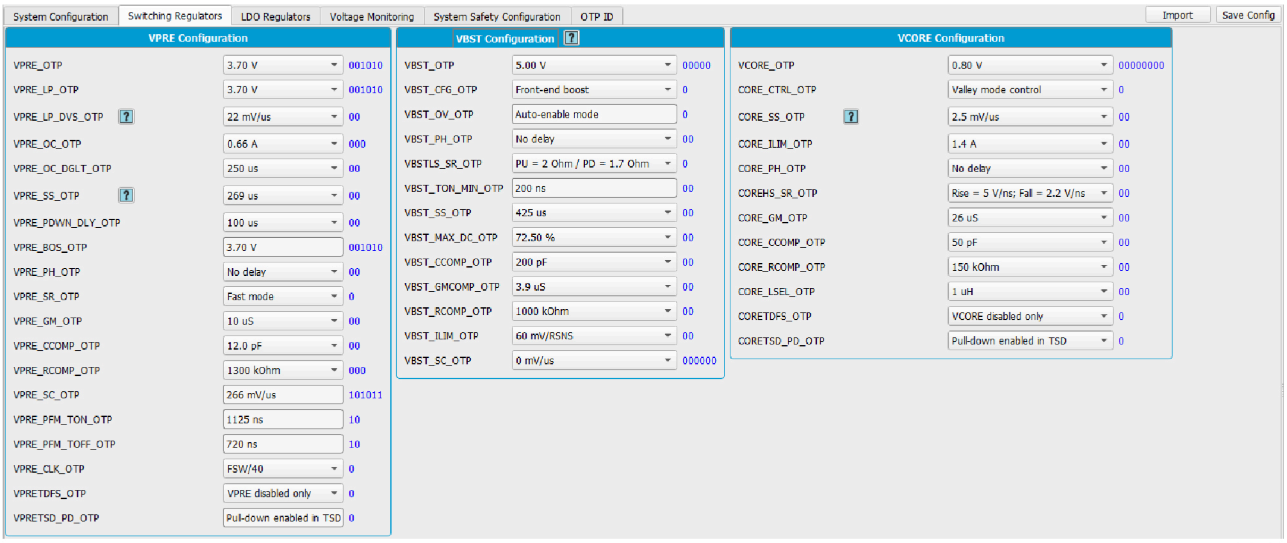
Figure 28. OTP System Configuration tab, part 2 of 2: I/Os Configuration and Power-up sequence diagram

7.3.2 Switching Regulators tab

The Switching Regulators tab shown in Figure 29 has three sections:

- **VPRE Configuration**: Minimum ON and OFF time in PFM mode and the slope compensation are set and cannot be modified. Also, VPRE transition voltage when going to Standby mode (VPRE_BOS_OTP) is linked to VPRE output voltage in Standby mode (VPRE_LP_OTP).Other parameters can be chosen.
- **VBST Configuration**: VBST minimum ontime is already set. Other parameters can be chosen.
- **VCORE Configuration**: VCORE conduction mode is already set. Other parameters can be chosen.



VPRE Configuration

VPRE_OTP	3.70 V	001010
VPRE_LP_OTP	3.70 V	001010
VPRE_LP_DVS_OTP	22 mV/us	00
VPRE_OC_OTP	0.66 A	000
VPRE_OC_DGLT_OTP	250 us	00
VPRE_SS_OTP	269 us	00
VPRE_PDWN_DLY_OTP	100 us	00
VPRE_BOS_OTP	3.70 V	001010
VPRE_PH_OTP	No delay	00
VPRE_SR_OTP	Fast mode	0
VPRE_GM_OTP	10 uS	00
VPRE_CCOMP_OTP	12.0 pF	00
VPRE_RCOMP_OTP	1300 kOhm	000
VPRE_SC_OTP	266 mV/us	101011
VPRE_PFM_TON_OTP	1125 ns	10
VPRE_PFM_TOFF_OTP	720 ns	10
VPRE_CLK_OTP	FSW/40	0
VPRETDFS_OTP	VPRE disabled only	0
VPRETSD_PD_OTP	Pull-down enabled in TSD	0

VBST Configuration

VBST_OTP	5.00 V	00000
VBST_CFG_OTP	Front-end boost	0
VBST_OV_OTP	Auto-enable mode	0
VBST_PH_OTP	No delay	00
VBSTLS_SR_OTP	PU = 2 Ohm / PD = 1.7 Ohm	0
VBST_TON_MIN_OTP	200 ns	00
VBST_SS_OTP	425 us	00
VBST_MAX_DC_OTP	72.50 %	00
VBST_CCOMP_OTP	200 pF	00
VBST_GMCOMP_OTP	3.9 uS	00
VBST_RCOMP_OTP	1000 kOhm	00
VBST_ILIM_OTP	60 mV/RSNS	00
VBST_SC_OTP	0 mV/us	000000

VCORE Configuration

VCORE_OTP	0.80 V	00000000
CORE_CTRL_OTP	Valley mode control	0
CORE_SS_OTP	2.5 mV/us	00
CORE_ILIM_OTP	1.4 A	00
CORE_PH_OTP	No delay	00
COREHS_SR_OTP	Rise = 5 V/ns; Fall = 2.2 V/ns	00
CORE_GM_OTP	26 uS	00
CORE_CCOMP_OTP	50 pF	00
CORE_RCOMP_OTP	150 kOhm	00
CORE_LSEL_OTP	1 uH	00
CORETDFS_OTP	VCORE disabled only	0
CORETSD_PD_OTP	Pull-down enabled in TSD	0

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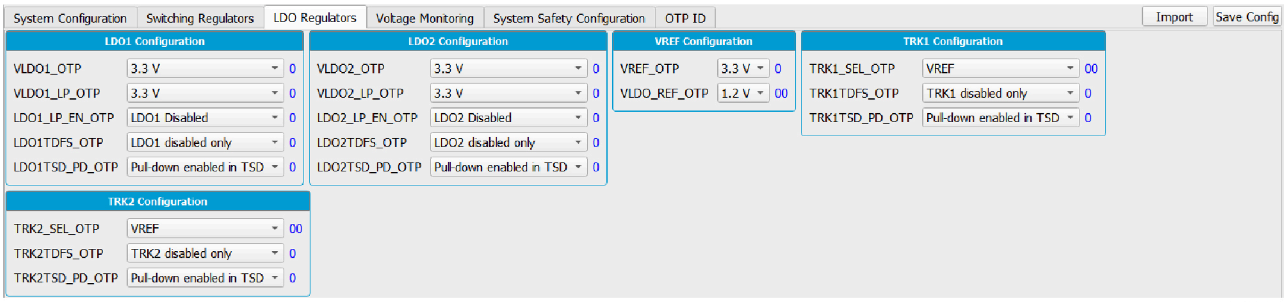
Figure 29. OTP SMPS regulators Configuration tab

7.3.3 LDO Regulators tab

The LDO Regulators tab shown in Figure 30 has five sections:

- **LDO1/LDO2 Configuration**: Linear dropout regulators configuration
- **VREF Configuration**: High-precision voltage linear dropout regulator configuration
- **TRK1/TRK2 Configuration**: Voltage tracking regulators configuration



LDO1 Configuration

VLDO1_OTP	3.3 V	0
VLDO1_LP_OTP	3.3 V	0
LDO1_LP_EN_OTP	LDO1 Disabled	0
LDO1TDFS_OTP	LDO1 disabled only	0
LDO1TSD_PD_OTP	Pull-down enabled in TSD	0

LDO2 Configuration

VLDO2_OTP	3.3 V	0
VLDO2_LP_OTP	3.3 V	0
LDO2_LP_EN_OTP	LDO2 Disabled	0
LDO2TDFS_OTP	LDO2 disabled only	0
LDO2TSD_PD_OTP	Pull-down enabled in TSD	0

VREF Configuration

VREF_OTP	3.3 V	0
VLDO_REF_OTP	1.2 V	00

TRK1 Configuration

TRK1_SEL_OTP	VREF	00
TRK1TDFS_OTP	TRK1 disabled only	0
TRK1TSD_PD_OTP	Pull-down enabled in TSD	0

TRK2 Configuration

TRK2_SEL_OTP	VREF	00
TRK2TDFS_OTP	TRK2 disabled only	0
TRK2TSD_PD_OTP	Pull-down enabled in TSD	0

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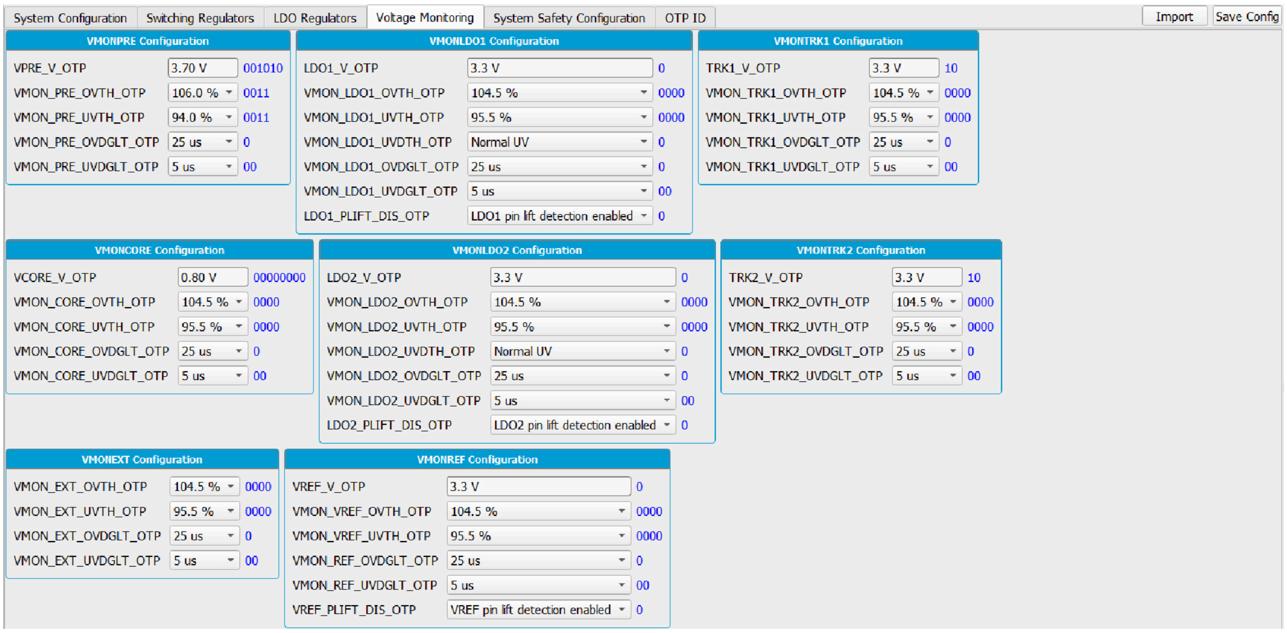
Figure 30. OTP LDO Regulators Configuration tab

7.3.4 Voltage Monitoring tab

The Voltage Monitoring tab shown in Figure 31 has eight sections:

- **VMONPRE/VMONCORE/VMONTRK1/VMONTRK2/VMONEXT Configuration**: Defines OV/UV thresholds and deglitch timings for VPRE, VCORE, TRK1 and TRK2 regulators. The monitoring voltages are bound to the respective regulator voltage set in the Switching/LDO Regulators tab (except for VMONEXT).
- **VMONLDO1/VMONLDO2/VMONREF Configuration**: Defines OV/UV thresholds, normal or degraded UV (except for VREF), pin lift detection enablement and deglitch timings for LDO1, LDO2 and VREF regulators.



VMONPRE Configuration

VPRE_V_OTP	3.70 V	001010
VMON_PRE_OVTH_OTP	106.0 %	0011
VMON_PRE_UVTH_OTP	94.0 %	0011
VMON_PRE_OVDGLT_OTP	25 us	0
VMON_PRE_UVDGLT_OTP	5 us	00

VMONLDO1 Configuration

LDO1_V_OTP	3.3 V	0
VMON_LDO1_OVTH_OTP	104.5 %	0000
VMON_LDO1_UVTH_OTP	95.5 %	0000
VMON_LDO1_UVDTH_OTP	Normal UV	0
VMON_LDO1_OVDGLT_OTP	25 us	0
VMON_LDO1_UVDGLT_OTP	5 us	00
LDO1_PLIFT_DIS_OTP	LDO1 pin lift detection enabled	0

VMONTRK1 Configuration

TRK1_V_OTP	3.3 V	10
VMON_TRK1_OVTH_OTP	104.5 %	0000
VMON_TRK1_UVTH_OTP	95.5 %	0000
VMON_TRK1_OVDGLT_OTP	25 us	0
VMON_TRK1_UVDGLT_OTP	5 us	00

VMONCORE Configuration

VCORE_V_OTP	0.80 V	00000000
VMON_CORE_OVTH_OTP	104.5 %	0000
VMON_CORE_UVTH_OTP	95.5 %	0000
VMON_CORE_OVDGLT_OTP	25 us	0
VMON_CORE_UVDGLT_OTP	5 us	00

VMONLDO2 Configuration

LDO2_V_OTP	3.3 V	0
VMON_LDO2_OVTH_OTP	104.5 %	0000
VMON_LDO2_UVTH_OTP	95.5 %	0000
VMON_LDO2_UVDTH_OTP	Normal UV	0
VMON_LDO2_OVDGLT_OTP	25 us	0
VMON_LDO2_UVDGLT_OTP	5 us	00
LDO2_PLIFT_DIS_OTP	LDO2 pin lift detection enabled	0

VMONTRK2 Configuration

TRK2_V_OTP	3.3 V	10
VMON_TRK2_OVTH_OTP	104.5 %	0000
VMON_TRK2_UVTH_OTP	95.5 %	0000
VMON_TRK2_OVDGLT_OTP	25 us	0
VMON_TRK2_UVDGLT_OTP	5 us	00

VMONEXT Configuration

VMON_EXT_OVTH_OTP	104.5 %	0000
VMON_EXT_UVTH_OTP	95.5 %	0000
VMON_EXT_OVDGLT_OTP	25 us	0
VMON_EXT_UVDGLT_OTP	5 us	00

VMONREF Configuration

VREF_V_OTP	3.3 V	0
VMON_VREF_OVTH_OTP	104.5 %	0000
VMON_VREF_UVTH_OTP	95.5 %	0000
VMON_REF_OVDGLT_OTP	25 us	0
VMON_REF_UVDGLT_OTP	5 us	00
VREF_PLIFT_DIS_OTP	VREF pin lift detection enabled	0

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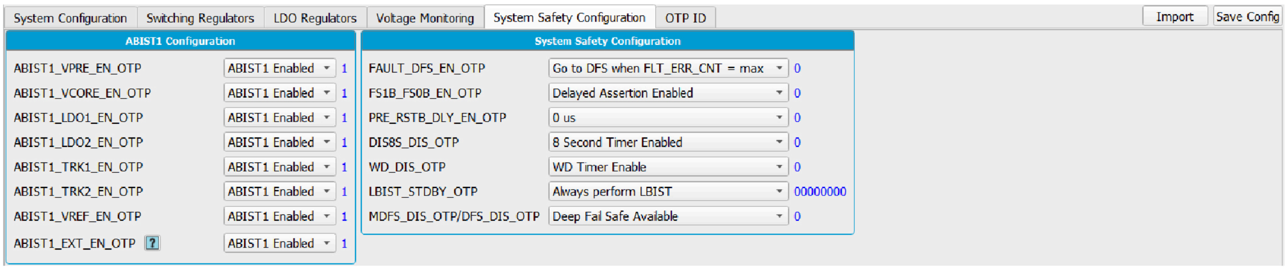
Figure 31. OTP Voltage Monitoring Configuration tab

7.3.5 System Safety Configuration tab

The System Safety Configuration tab shown in Figure 32 has two sections:

- **ABIST1 Configuration**: Allows the user to enable or disable ABIST1 execution for each available kind of monitoring
- **System Safety Configuration**: DFS, FS1B behavior, Watchdog, LBIST, RSTB, ...



ABIST1 Configuration

ABIST1_VPRE_EN_OTP	ABIST1 Enabled	1
ABIST1_VCORE_EN_OTP	ABIST1 Enabled	1
ABIST1_LDO1_EN_OTP	ABIST1 Enabled	1
ABIST1_LDO2_EN_OTP	ABIST1 Enabled	1
ABIST1_TRK1_EN_OTP	ABIST1 Enabled	1
ABIST1_TRK2_EN_OTP	ABIST1 Enabled	1
ABIST1_VREF_EN_OTP	ABIST1 Enabled	1
ABIST1_EXT_EN_OTP	ABIST1 Enabled	1

System Safety Configuration

FAULT_DFS_EN_OTP	Go to DFS when FLT_ERR_CNT = max	0
FS1B_FS0B_EN_OTP	Delayed Assertion Enabled	0
PRE_RSTB_DLY_EN_OTP	0 us	0
DIS8S_DIS_OTP	8 Second Timer Enabled	0
WD_DIS_OTP	WD Timer Enable	0
LBIST_STDBY_OTP	Always perform LBIST	00000000
MDFS_DIS_OTP/DFS_DIS_OTP	Deep Fail Safe Available	0

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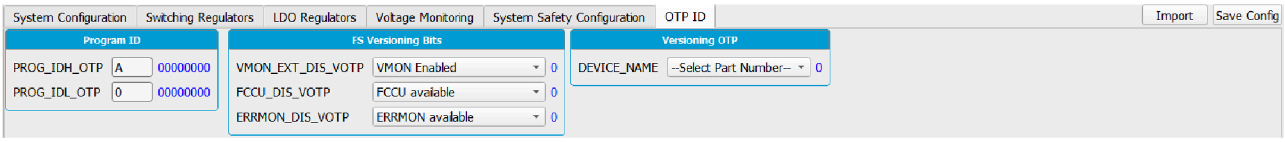
Figure 32. OTP System Safety Configuration tab

7.3.6 OTP ID tab

The OTP ID tab shown in Figure 33 has three sections:

- **Program ID**: Shows the OTP ID code
- **FS Versioning Bits**: DFS, FS1B behavior, Watchdog, LBIST, RSTB…

- **Versioning Bits**: Allows the user to choose one of the generic part numbers from the dropdown list – this automatically updates the related OTP and VOTP configuration bits to match the selected part number (VCORE current capability, LDT, TRK2, FS1B, ABIST2, Watchdog, Fault recovery, FCCU, and LBIST)



Program ID

PROG_IDH_OTP A 00000000

PROG_IDL_OTP 0 00000000

FS Versioning Bits

VMON_EXT_DIS_VOTP VMON Enabled 0

FCCU_DIS_VOTP FCCU available 0

ERRMON_DIS_VOTP ERRMON available 0

Versioning OTP

DEVICE_NAME --Select Part Number-- 0

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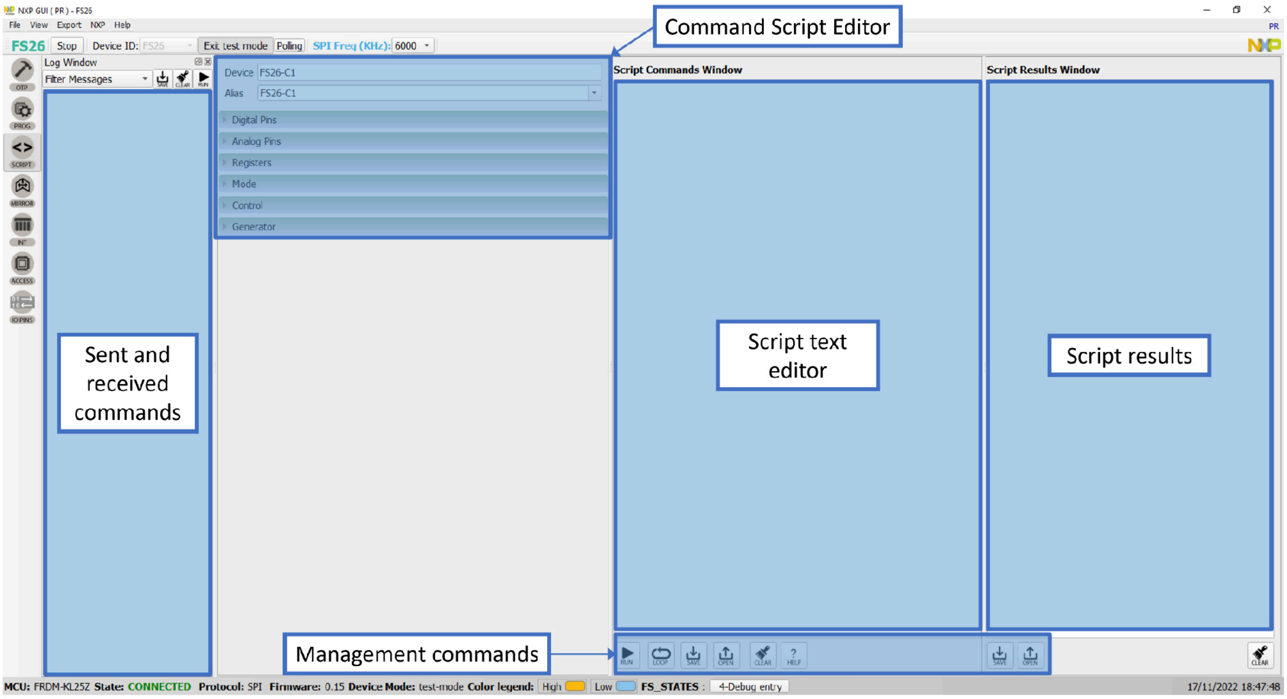
Figure 33. OTP ID tab

7.4 Device programming

The Device Programming tab shown in Figure 34 allows the user to burn the FS2600 OTP using a script initially generated by the OTP tool. In order to enable this window, the device must be in test mode.



Device FS26-C1

Alias FS26-C1

MCU: FRDM-KL25Z State: CONNECTED Protocol: SPI Firmware: 0.15 Device Mode: test-mode Color legend: High 🟨 Low 🟦 FS_STATES : 4-Debug entry 17/11/2022 18:47:48

aaa-050246

Figure 34. Device programming

To program an OTP configuration, the V_{OTP} voltage must be applied to the DEBUG pin. To do so, the user must turn on SW7 to apply 8.0 V to the FS26 DEBUG pin.

Click **Browse** to select an OTP script file, then click the **Program** button to run the script. If the DEBUG pin voltage is not set to V_{OTP}, a pop up appears to ask the user to turn on SW7, or it turns on automatically if jumper J13 is on Automatic mode J13 3-2.

If the required conditions are met (sectors are available), the programming process starts. Otherwise, the execution is canceled. To verify that the sectors are available, click **Read** from the Fuse Box Status window.

OTP is programmed into SECTBE2 of Main and Fail-safe. SECTBE1 and SECTBE0 are reserved for NXP users only.

Blue or ‘0’: Available

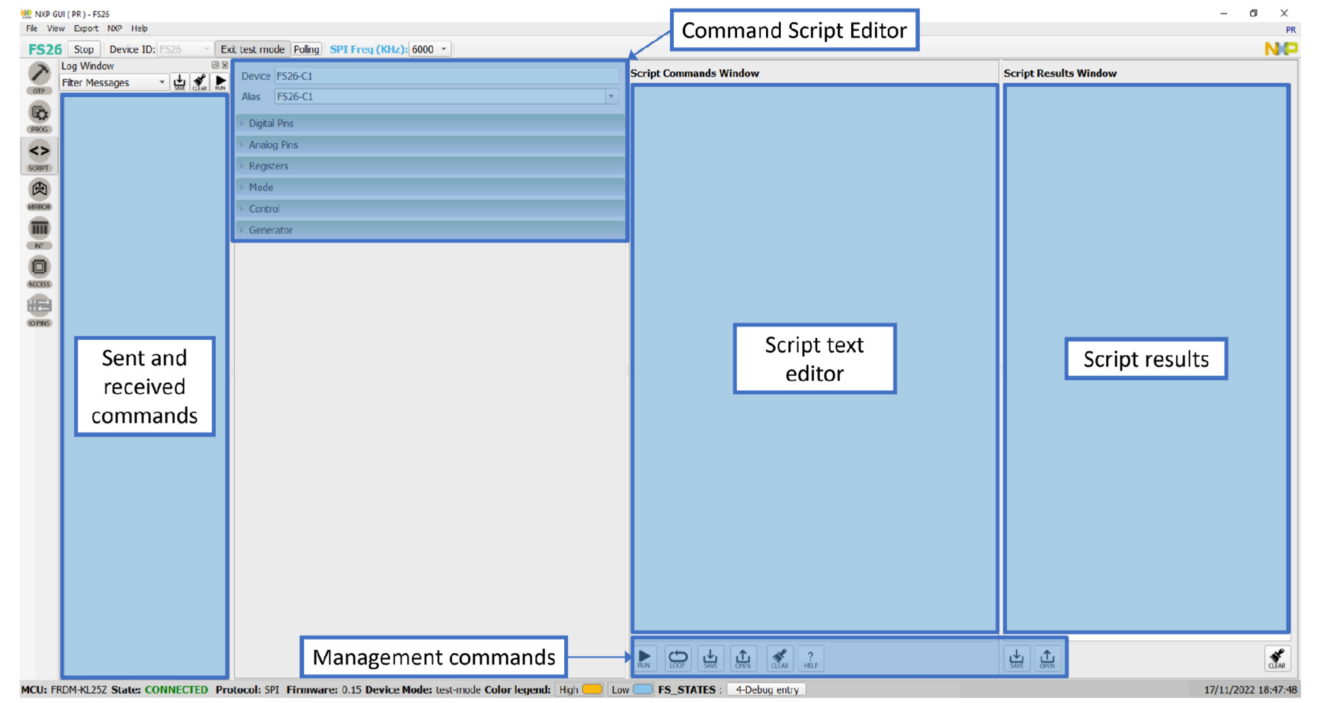
Yellow or ‘1’: Not available

When programming is complete, a pop up appears to ask the user to turn off SW7 and SW6 (set DEBUG pin voltage to 0 V).

If the device was programmed correctly, the power-up sequence starts. Fuse box status can be read to check whether sectors are burned. In some conditions, a power up could be required.

7.5 Script tab

The registers and OTP emulation can be configured with the Script editor shown in Figure 35. The Script editor is useful for trying various OTP configurations in OTP Emulation mode.



MCU: FRDM-KL25Z State: CONNECTED Protocol: SPI Firmware: 0.15 Device Mode: test-mode Color legend: High Low FS_STATES : 4-Debug entry 17/11/2022 18:47:48

aaa-050246

Figure 35. Script editor

The main subareas of this panel are:

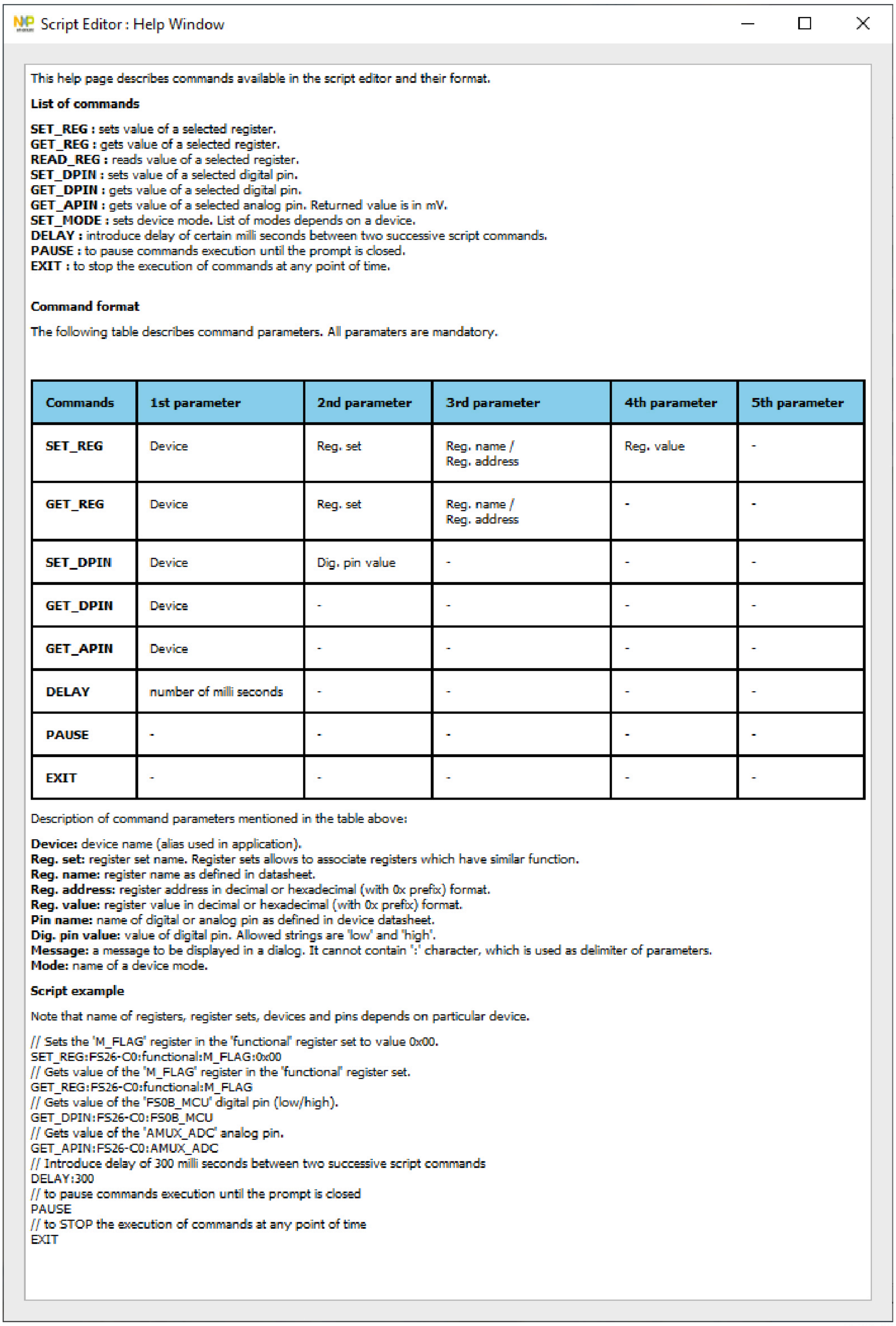
- **Command Script Editor**: Builds commands to be sent to the device.
- **Script Text Editor**: Sends a sequence of register configurations from a text file or from a command edited directly in this area.
- **Script Results**: Displays result status of each command sent to the device.
- **Sent and Received Commands**: Displays a summary of commands sent and received from the device.
- **Management Commands**: These commands are used for scripts.

7.5.1 Command script editor

Using the script editor, the user can execute any command either directly or from a file. It is also possible to save and modify a script. Using the brush symbol, it is possible to clean windows if necessary.

All commands must follow a specific syntax. The Help menu describes the commands available in the script editor and the syntax to be used.

Figure 36 shows an example of building a command from the panel.



This help page describes commands available in the script editor and their format.

List of commands

SET_REG : sets value of a selected register.
GET_REG : gets value of a selected register.
READ_REG : reads value of a selected register.
SET_DPIN : sets value of a selected digital pin.
GET_DPIN : gets value of a selected digital pin.
GET_APIN : gets value of a selected analog pin. Returned value is in mV.
SET_MODE : sets device mode. List of modes depends on a device.
DELAY : introduce delay of certain milli seconds between two successive script commands.
PAUSE : to pause commands execution until the prompt is closed.
EXIT : to stop the execution of commands at any point of time.

Command format

The following table describes command parameters. All paramaters are mandatory.

Commands	1st parameter	2nd parameter	3rd parameter	4th parameter	5th parameter
SET_REG	Device	Reg. set	Reg. name / Reg. address	Reg. value	-
GET_REG	Device	Reg. set	Reg. name / Reg. address	-	-
SET_DPIN	Device	Dig. pin value	-	-	-
GET_DPIN	Device	-	-	-	-
GET_APIN	Device	-	-	-	-
DELAY	number of milli seconds	-	-	-	-
PAUSE	-	-	-	-	-
EXIT	-	-	-	-	-

Description of command parameters mentioned in the table above:

Device: device name (alias used in application).
Reg. set: register set name. Register sets allows to associate registers which have similar function.
Reg. name: register name as defined in datasheet.
Reg. address: register address in decimal or hexadecimal (with 0x prefix) format.
Reg. value: register value in decimal or hexadecimal (with 0x prefix) format.
Pin name: name of digital or analog pin as defined in device datasheet.
Dig. pin value: value of digital pin. Allowed strings are 'low' and 'high'.
Message: a message to be displayed in a dialog. It cannot contain ':' character, which is used as delimiter of parameters.
Mode: name of a device mode.

Script example

Note that name of registers, register sets, devices and pins depends on particular device.

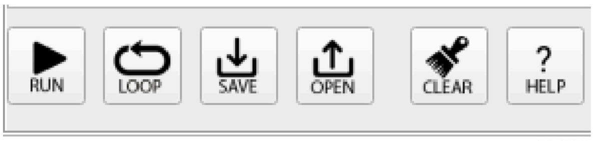
```
// Sets the 'M_FLAG' register in the 'functional' register set to value 0x00.
SET_REG:FS26-C0:functional:M_FLAG:0x00
// Gets value of the 'M_FLAG' register in the 'functional' register set.
GET_REG:FS26-C0:functional:M_FLAG
// Gets value of the 'FS0B_MCU' digital pin (low/high).
GET_DPIN:FS26-C0:FS0B_MCU
// Gets value of the 'AMUX_ADC' analog pin.
GET_APIN:FS26-C0:AMUX_ADC
// Introduce delay of 300 milli seconds between two successive script commands
DELAY:300
// to pause commands execution until the prompt is closed
PAUSE
// to STOP the execution of commands at any point of time
EXIT
```

aaa-046932

Figure 36. Script Editor: Help window

7.5.2 Management commands

Some commands are used for formatting the scripts. Figure 37 shows the description of each button.



aaa-046933

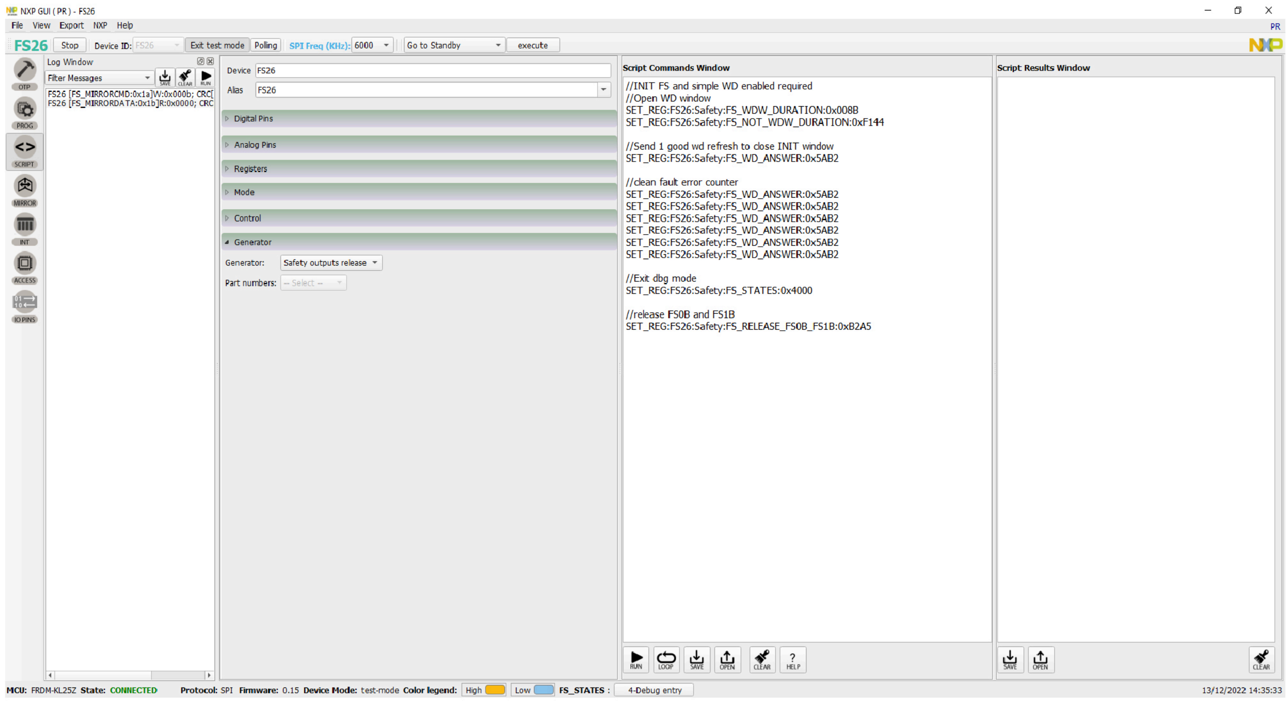
Figure 37. Script editor commands

- **Run**: Runs the script once.
- **Loop**: Runs the script continuously in a loop.
- **Save**: Save the script that is present in the script command window in text file.
- **Open**: Open a saved script from the desired location.
- **Clear**: Clears the script command window.
- **Script Editor Help Window**: Describes the commands available in the script editor and their formats.

7.5.3 Script editor

The script editor allows the user to create or send existing sequences to the device. The user can read/write individually to a register, to an I/O, or to an analog pin. The user can emulate an OTP configuration as well with this tab.

This tab can be accessed from Toolbar → SCRIPT or View → Show → Script Editor.



Device ID: FS26

SPI Freq (KHz): 6000

Go to Standby

Filter Messages

```
FS26 [FS_MIRRORCMD:0x1a]W:0x000b; CRC[
FS26 [FS_MIRRORDATA:0x1b]R:0x0000; CRC
```

Device: FS26

Alias: FS26

Generator: Safety outputs release

Part numbers: -- Select --

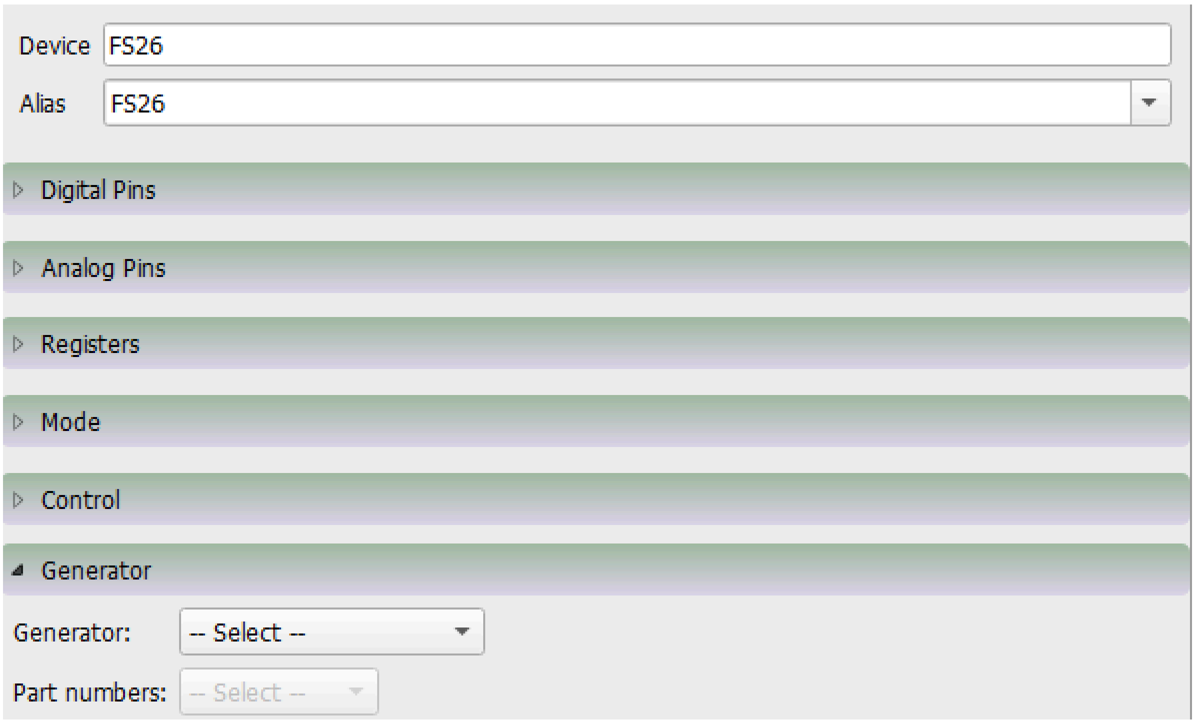
```
//INIT FS and simple WD enabled required
//Open WD window
SET_REG:FS26:Safety:FS_WDW_DURATION:0x008B
SET_REG:FS26:Safety:FS_NOT_WDW_DURATION:0xF144

//Send 1 good wd refresh to close INIT window
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2

//clean fault error counter
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2

//Exit dbg mode
SET_REG:FS26:Safety:FS_STATES:0x4000

//release FS0B and FS1B
SET_REG:FS26:Safety:FS_RELEASE_FS0B_FS1B:0xB2A5
```

MCU: FRDM-KL25Z State: CONNECTED Protocol: SPI Firmware: 0.15 Device Mode: test-mode Color legend: High 🟧 Low 🟦 FS_STATES : 4-Debug entry 13/12/2022 14:35:33

aaa-050247

Figure 38. Script Editor

The script can be written by selecting and configuring the pins and registers that are available in the script commands section or by loading a previously exported .txt file.



Device: FS26

Alias: FS26

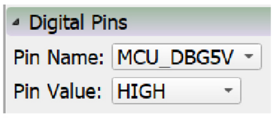
Generator: -- Select --

Part numbers: -- Select --

Figure 39. Use script editor to access more commands

Click one type of command to access more options, until the command to build the sequence is found.

- Digital pins: Select the pin name, then pin value (HIGH or LOW). The command is automatically added to the script.



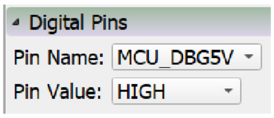
Pin Name: MCU_DBG5V

Pin Value: HIGH

aaa-046936

Figure 40. Digital Pins

- Analog pins: Select the pin name and then write the pin value. If the pin is read only, the pin value is not enabled and it gets added to script editor automatically.



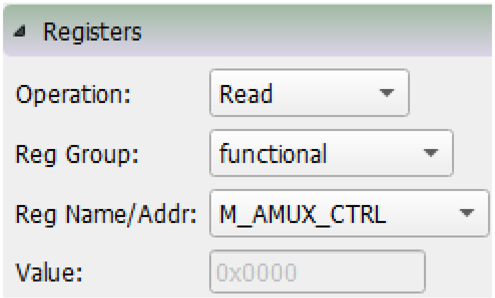
Pin Name: MCU_DBG5V

Pin Value: HIGH

aaa-046936

Figure 41. Digital Pins

- Registers: Select the Operation (Read/Write).
  – Read: Select the register group, then the register name. The register is added to script editor automatically.



◢ Registers

Operation: Read

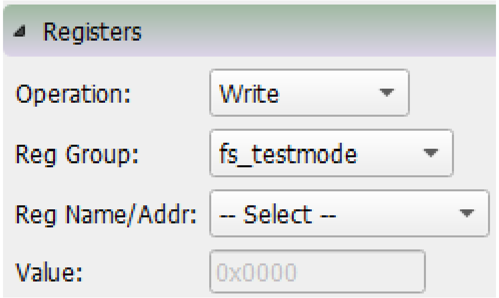
Reg Group: functional

Reg Name/Addr: M_AMUX_CTRL

Value: 0x0000

Figure 42. Registers: Read

- Write: Select the register group, then the register name. Write the value and click the enter key. The value must be written in HEX. Press the Enter key to add to the editor.



◢ Registers

Operation: Write

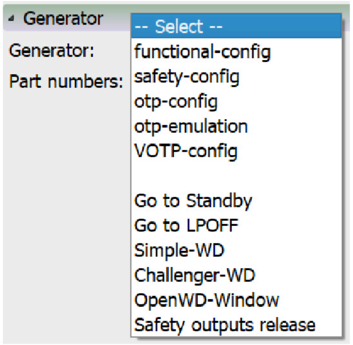
Reg Group: fs_testmode

Reg Name/Addr: -- Select --

Value: 0x0000

Figure 43. Registers: Write

- Mode: Write command to exit or enter different device modes.
  - Test mode: Send main and Fail-safe test mode entry keys.
  - User mode: Exit test mode if device is in test mode.
- Generator: Select an existing script to add to the script editor. Some options may require to be in a specific mode or state.



◢ Generator

Generator:

Part numbers:

Figure 44. Generator

The script operations can be found at the bottom of the script editor window. This section is responsible for:

- Execution of script
- Script management: Create, Open, Save, Run
- Logging feature: Load, Save, Clear

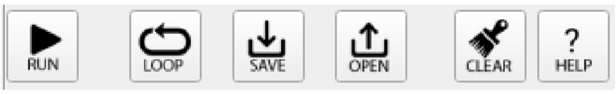


Figure 45. Script editor controls

Run: Runs the script once

Loop: Runs the script continuously in a loop

Save: Saves the script that is present in the script command window in a text file

Open: Opens a saved script from the desired location

ATE: Saves the script in ATE format

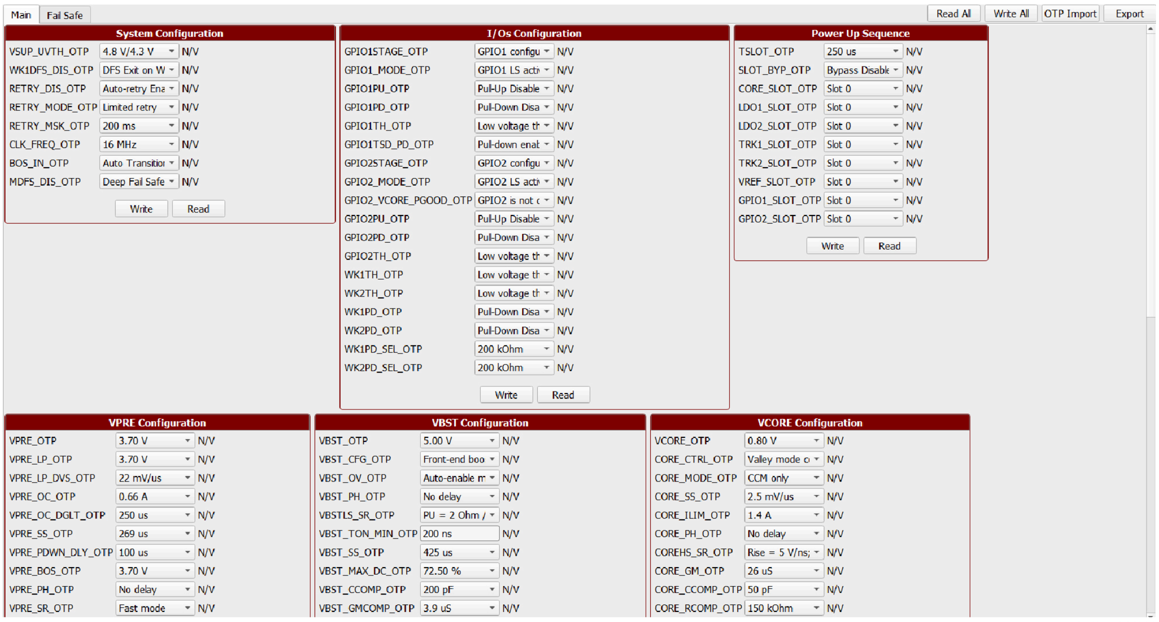
Clear: Clears the script command window

Script Editor Help Window: This section describes the commands available in Script editor, and their formats. This option can be accessed from Menu → SCRIPT → Help or View → Show → Script Editor → Help.

7.6 Mirrors tab

Test mode must be applied to enable the Mirrors tab. This tab is divided into main and fail-safe mirrors registers, shown in Figure 46 and Figure 47, respectively.

The **Read/Write All** buttons can be used to read/write the entire set of mirrors registers. The Mirrors configuration can be exported and imported in the OTP tool as an OTP configuration to generate TBB/OTP scripts files.



System Configuration		
VSUP_UVTH_OTP	4.8 V/4.3 V	N/V
WK1DFS_DIS_OTP	DFS Exit on W	N/V
RETRY_DIS_OTP	Auto-retry Ena	N/V
RETRY_MODE_OTP	Limited retry	N/V
RETRY_MSK_OTP	200 ms	N/V
CLK_FREQ_OTP	16 MHz	N/V
BOS_IN_OTP	Auto Transitio	N/V
MDFS_DIS_OTP	Deep Fail Safe	N/V

I/Os Configuration		
GPIO1STAGE_OTP	GPIO1 configu	N/V
GPIO1_MODE_OTP	GPIO1 LS acti	N/V
GPIO1PU_OTP	Pull-Up Disable	N/V
GPIO1PD_OTP	Pull-Down Disa	N/V
GPIO1TH_OTP	Low voltage th	N/V
GPIO1TSD_PD_OTP	Pull-down enal	N/V
GPIO2STAGE_OTP	GPIO2 configu	N/V
GPIO2_MODE_OTP	GPIO2 LS acti	N/V
GPIO2_VCORE_PGOOD_OTP	GPIO2 is not c	N/V
GPIO2PU_OTP	Pull-Up Disable	N/V
GPIO2PD_OTP	Pull-Down Disa	N/V
GPIO2TH_OTP	Low voltage th	N/V
WK1TH_OTP	Low voltage th	N/V
WK2TH_OTP	Low voltage th	N/V
WK1PD_OTP	Pull-Down Disa	N/V
WK2PD_OTP	Pull-Down Disa	N/V
WK1PD_SEL_OTP	200 kOhm	N/V
WK2PD_SEL_OTP	200 kOhm	N/V

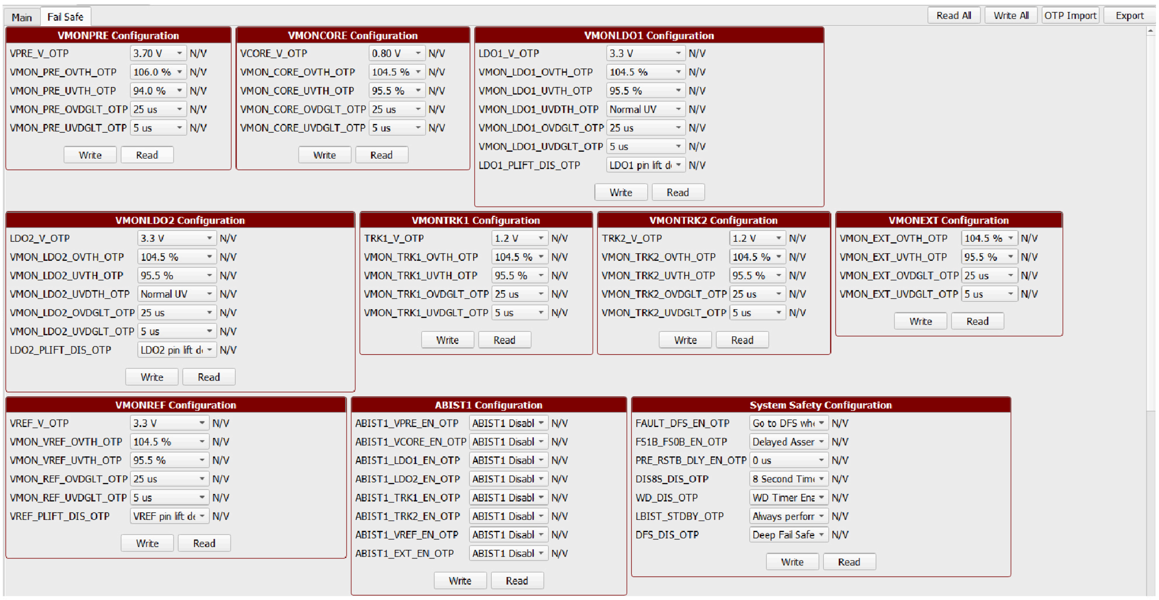
Power Up Sequence		
TSLOT_OTP	250 us	N/V
SLOT_BYP_OTP	Bypass Disable	N/V
CORE_SLOT_OTP	Slot 0	N/V
LDO1_SLOT_OTP	Slot 0	N/V
LDO2_SLOT_OTP	Slot 0	N/V
TRK1_SLOT_OTP	Slot 0	N/V
TRK2_SLOT_OTP	Slot 0	N/V
VREF_SLOT_OTP	Slot 0	N/V
GPIO1_SLOT_OTP	Slot 0	N/V
GPIO2_SLOT_OTP	Slot 0	N/V

VPRE Configuration		
VPRE_OTP	3.70 V	N/V
VPRE_LP_OTP	3.70 V	N/V
VPRE_LP_DVS_OTP	22 mV/us	N/V
VPRE_OC_OTP	0.66 A	N/V
VPRE_OC_DGLT_OTP	250 us	N/V
VPRE_SS_OTP	269 us	N/V
VPRE_PDWN_DLY_OTP	100 us	N/V
VPRE_BOS_OTP	3.70 V	N/V
VPRE_PH_OTP	No delay	N/V
VPRE_SR_OTP	Fast mode	N/V

VBST Configuration		
VBST_OTP	5.00 V	N/V
VBST_CFG_OTP	Front-end boo	N/V
VBST_OV_OTP	Auto-enable m	N/V
VBST_PH_OTP	No delay	N/V
VBSTLS_SR_OTP	PU = 2 Ohm /	N/V
VBST_TON_MIN_OTP	200 ns	N/V
VBST_SS_OTP	425 us	N/V
VBST_MAX_DC_OTP	72.50 %	N/V
VBST_CCOMP_OTP	200 pF	N/V
VBST_GMCOMP_OTP	3.9 uS	N/V

VCORE Configuration		
VCORE_OTP	0.80 V	N/V
CORE_CTRL_OTP	Valley mode c	N/V
CORE_MODE_OTP	CCM only	N/V
CORE_SS_OTP	2.5 mV/us	N/V
CORE_ILIM_OTP	1.4 A	N/V
CORE_PH_OTP	No delay	N/V
COREHS_SR_OTP	Rise = 5 V/ns;	N/V
CORE_GM_OTP	26 uS	N/V
CORE_CCOMP_OTP	50 pF	N/V
CORE_RCOMP_OTP	150 kOhm	N/V

Figure 46. Main mirrors tab



VMONPRE Configuration		
VPRE_V_OTP	3.70 V	N/V
VMON_PRE_OVTH_OTP	106.0 %	N/V
VMON_PRE_UVTH_OTP	94.0 %	N/V
VMON_PRE_OVDGLT_OTP	25 us	N/V
VMON_PRE_UVDGLT_OTP	5 us	N/V

VMONCORE Configuration		
VCORE_V_OTP	0.80 V	N/V
VMON_CORE_OVTH_OTP	104.5 %	N/V
VMON_CORE_UVTH_OTP	95.5 %	N/V
VMON_CORE_OVDGLT_OTP	25 us	N/V
VMON_CORE_UVDGLT_OTP	5 us	N/V

VMONLDO1 Configuration		
LDO1_V_OTP	3.3 V	N/V
VMON_LDO1_OVTH_OTP	104.5 %	N/V
VMON_LDO1_UVTH_OTP	95.5 %	N/V
VMON_LDO1_UVDTH_OTP	Normal UV	N/V
VMON_LDO1_OVDGLT_OTP	25 us	N/V
VMON_LDO1_UVDGLT_OTP	5 us	N/V
LDO1_PLIFT_DIS_OTP	LDO1 pin lift d	N/V

VMONLDO2 Configuration		
LDO2_V_OTP	3.3 V	N/V
VMON_LDO2_OVTH_OTP	104.5 %	N/V
VMON_LDO2_UVTH_OTP	95.5 %	N/V
VMON_LDO2_UVDTH_OTP	Normal UV	N/V
VMON_LDO2_OVDGLT_OTP	25 us	N/V
VMON_LDO2_UVDGLT_OTP	5 us	N/V
LDO2_PLIFT_DIS_OTP	LDO2 pin lift d	N/V

VMONTRK1 Configuration		
TRK1_V_OTP	1.2 V	N/V
VMON_TRK1_OVTH_OTP	104.5 %	N/V
VMON_TRK1_UVTH_OTP	95.5 %	N/V
VMON_TRK1_OVDGLT_OTP	25 us	N/V
VMON_TRK1_UVDGLT_OTP	5 us	N/V

VMONTRK2 Configuration		
TRK2_V_OTP	1.2 V	N/V
VMON_TRK2_OVTH_OTP	104.5 %	N/V
VMON_TRK2_UVTH_OTP	95.5 %	N/V
VMON_TRK2_OVDGLT_OTP	25 us	N/V
VMON_TRK2_UVDGLT_OTP	5 us	N/V

VMONEXT Configuration		
VMON_EXT_OVTH_OTP	104.5 %	N/V
VMON_EXT_UVTH_OTP	95.5 %	N/V
VMON_EXT_OVDGLT_OTP	25 us	N/V
VMON_EXT_UVDGLT_OTP	5 us	N/V

VMONREF Configuration		
VREF_V_OTP	3.3 V	N/V
VMON_VREF_OVTH_OTP	104.5 %	N/V
VMON_VREF_UVTH_OTP	95.5 %	N/V
VMON_REF_OVDGLT_OTP	25 us	N/V
VMON_REF_UVDGLT_OTP	5 us	N/V
VREF_PLIFT_DIS_OTP	VREF pin lift de	N/V

ABIST1 Configuration		
ABIST1_VPRE_EN_OTP	ABIST1 Disabl	N/V
ABIST1_VCORE_EN_OTP	ABIST1 Disabl	N/V
ABIST1_LDO1_EN_OTP	ABIST1 Disabl	N/V
ABIST1_LDO2_EN_OTP	ABIST1 Disabl	N/V
ABIST1_TRK1_EN_OTP	ABIST1 Disabl	N/V
ABIST1_TRK2_EN_OTP	ABIST1 Disabl	N/V
ABIST1_VREF_EN_OTP	ABIST1 Disabl	N/V
ABIST1_EXT_EN_OTP	ABIST1 Disabl	N/V

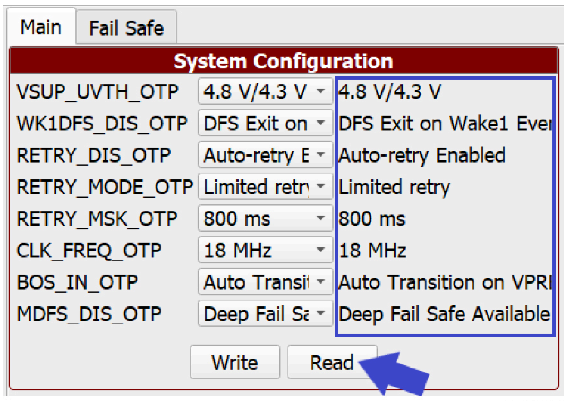
System Safety Configuration		
FAULT_DFS_EN_OTP	Go to DFS whe	N/V
FS1B_FS0B_EN_OTP	Delayed Asser	N/V
PRE_RSTB_DLY_EN_OTP	0 us	N/V
DIS8S_DIS_OTP	8 Second Time	N/V
WD_DIS_OTP	WD Timer Ena	N/V
LBIST_STDBY_OTP	Always perforr	N/V
DFS_DIS_OTP	Deep Fail Safe	N/V

aaa-050249

Figure 47. Fail-safe mirrors tab

7.6.1 Read/write operation

To read a bit group, click **Read** from a box. Read values are displayed to the right of each register.

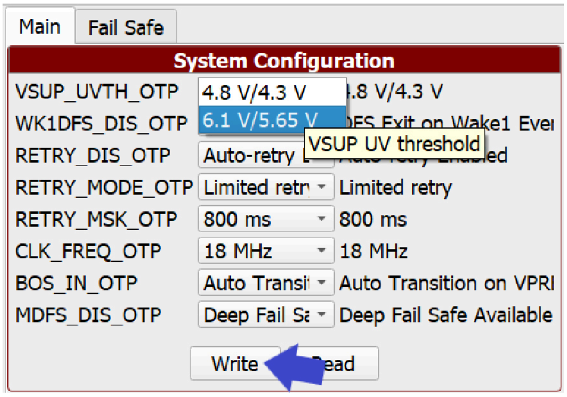


System Configuration		
VSUP_UVTH_OTP	4.8 V/4.3 V	4.8 V/4.3 V
WK1DFS_DIS_OTP	DFS Exit on	DFS Exit on Wake1 Eve
RETRY_DIS_OTP	Auto-retry E	Auto-retry Enabled
RETRY_MODE_OTP	Limited retr	Limited retry
RETRY_MSK_OTP	800 ms	800 ms
CLK_FREQ_OTP	18 MHz	18 MHz
BOS_IN_OTP	Auto Transi	Auto Transition on VPRI
MDFS_DIS_OTP	Deep Fail Sa	Deep Fail Safe Available

aaa-046943

Figure 48. Read bit group

To write to a bit group, modify the controls of each register, then click **Write**.



VSUP_UVTH_OTP	4.8 V/4.3 V	.8 V/4.3 V
WK1DFS_DIS_OTP		DFS Exit on Wake1 Eve
RETRY_DIS_OTP	Auto-retry	ed
RETRY_MODE_OTP	Limited retr	Limited retry
RETRY_MSK_OTP	800 ms	800 ms
CLK_FREQ_OTP	18 MHz	18 MHz
BOS_IN_OTP	Auto Transi	Auto Transition on VPRI
MDFS_DIS_OTP	Deep Fail Sa	Deep Fail Safe Available

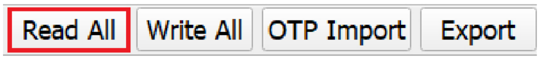
aaa-046944

Figure 49. Write bit group

7.6.2 Read/write all and write all operation

Read All reads the bits of each block from all mirror registers.

Read values also appear at the right of each register in the window log.



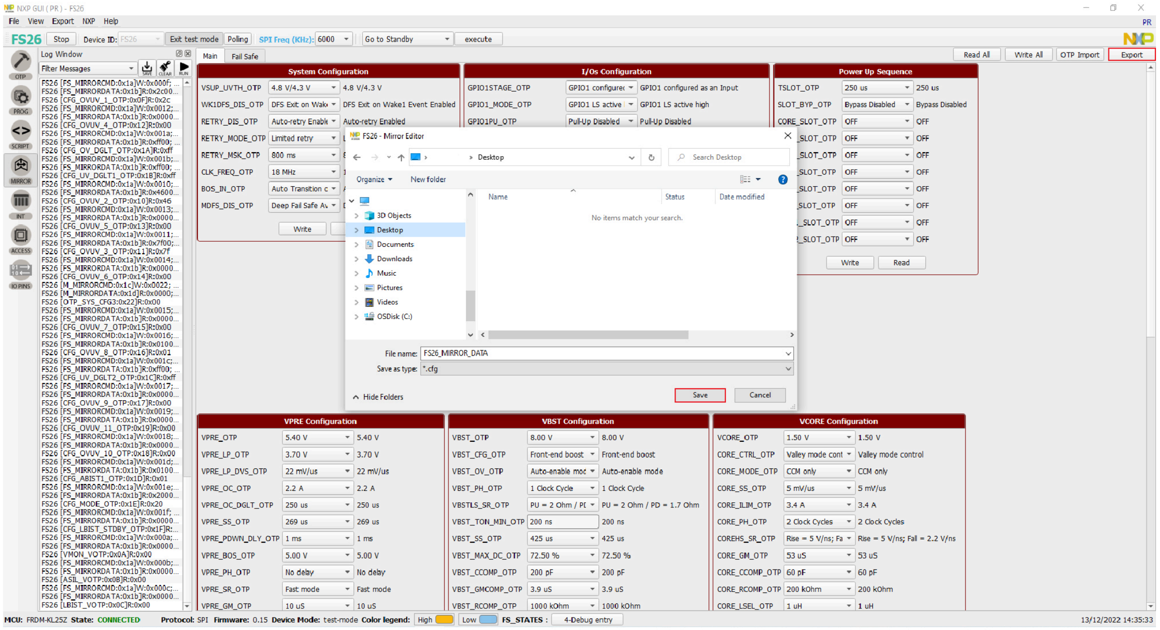
aaa-046945

Figure 50. Read all

To write all OTP bit groups configuration, click **Write All**.

7.6.3 Mirror registers export option

This operation generates a configuration file, which is saved as a text file in the local device. The configuration file can be imported into this tab later. Figure 51 shows the generated .txt configuration file.



Device ID: FS26

SPI Freq (KHz): 6000

```
FS26 [FS_MIRRORCMD:0x1a]W:0x000f; ...
FS26 [FS_MIRRORDATA:0x1b]R:0x2c00...
FS26 [CFG_OVUV_1_OTP:0x0F]R:0x2c
FS26 [FS_MIRRORCMD:0x1a]W:0x0012;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_4_OTP:0x12]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x001a;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_OV_DGLT_OTP:0x1A]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x001b;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_UV_DGLT1_OTP:0x1B]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x0010;...
FS26 [FS_MIRRORDATA:0x1b]R:0x4600...
FS26 [CFG_OVUV_2_OTP:0x10]R:0x46
FS26 [FS_MIRRORCMD:0x1a]W:0x0013;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_5_OTP:0x13]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0011;...
FS26 [FS_MIRRORDATA:0x1b]R:0x7f00;...
FS26 [CFG_OVUV_3_OTP:0x11]R:0x7f
FS26 [FS_MIRRORCMD:0x1a]W:0x0014;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_6_OTP:0x14]R:0x00
FS26 [M_MIRRORCMD:0x1c]W:0x0022; ...
FS26 [M_MIRRORDATA:0x1d]R:0x0000;...
FS26 [OTP_SYS_CFG3:0x22]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0015;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_7_OTP:0x15]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0016;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0100...
FS26 [CFG_OVUV_8_OTP:0x16]R:0x01
FS26 [FS_MIRRORCMD:0x1a]W:0x001c;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_UV_DGLT2_OTP:0x1C]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x0017;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_9_OTP:0x17]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0019;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_11_OTP:0x19]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0018;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_10_OTP:0x18]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x001d;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0100...
FS26 [CFG_ABIST1_OTP:0x1D]R:0x01
FS26 [FS_MIRRORCMD:0x1a]W:0x001e;...
FS26 [FS_MIRRORDATA:0x1b]R:0x2000...
FS26 [CFG_MODE_OTP:0x1E]R:0x20
FS26 [FS_MIRRORCMD:0x1a]W:0x001f; ...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_LBIST_STDBY_OTP:0x1F]R:...
FS26 [FS_MIRRORCMD:0x1a]W:0x000a;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [VMON_VOTP:0x0A]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x000b;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [ASIL_VOTP:0x0B]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x000c;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [LBIST_VOTP:0x0C]R:0x00
```

System Configuration		
VSUP_UVTH_OTP	4.8 V/4.3 V	4.8 V/4.3 V
WK1DFS_DIS_OTP	DFS Exit on Wak	DFS Exit on Wake1 Event Enabled
RETRY_DIS_OTP	Auto-retry Enable	Auto-retry Enabled
RETRY_MODE_OTP	Limited retry	L
RETRY_MSK_OTP	800 ms	8
CLK_FREQ_OTP	18 MHz	1
BOS_IN_OTP	Auto Transition c	A
MDFS_DIS_OTP	Deep Fail Safe Av	D

I/Os Configuration		
GPIO1STAGE_OTP	GPIO1 configure	GPIO1 configured as an Input
GPIO1_MODE_OTP	GPIO1 LS active	GPIO1 LS active high
GPIO1PU_OTP	Pull-Up Disabled	Pull-Up Disabled

Power Up Sequence		
TSLOT_OTP	250 us	250 us
SLOT_BYP_OTP	Bypass Disabled	Bypass Disabled
CORE_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF
_SLOT_OTP	OFF	OFF

FS26 - Mirror Editor

Desktop

Search Desktop

Organize

New folder

3D Objects
Desktop
Documents
Downloads
Music
Pictures
Videos
OSDisk (C:)

Name	Status	Date modified

No items match your search.

File name: FS26_MIRROR_DATA

Save as type: *.cfg

Hide Folders

Save

Cancel

VPRE Configuration		
VPRE_OTP	5.40 V	5.40 V
VPRE_LP_OTP	3.70 V	3.70 V
VPRE_LP_DVS_OTP	22 mV/us	22 mV/us
VPRE_OC_OTP	2.2 A	2.2 A
VPRE_OC_DGLT_OTP	250 us	250 us
VPRE_SS_OTP	269 us	269 us
VPRE_PDWN_DLY_OTP	1 ms	1 ms
VPRE_BOS_OTP	5.00 V	5.00 V
VPRE_PH_OTP	No delay	No delay
VPRE_SR_OTP	Fast mode	Fast mode
VPRE_GM_OTP	10 uS	10 uS

VBST Configuration		
VBST_OTP	8.00 V	8.00 V
VBST_CFG_OTP	Front-end boost	Front-end boost
VBST_OV_OTP	Auto-enable moc	Auto-enable mode
VBST_PH_OTP	1 Clock Cycle	1 Clock Cycle
VBSTLS_SR_OTP	PU = 2 Ohm / PI	PU = 2 Ohm / PD = 1.7 Ohm
VBST_TON_MIN_OTP	200 ns	200 ns
VBST_SS_OTP	425 us	425 us
VBST_MAX_DC_OTP	72.50 %	72.50 %
VBST_CCOMP_OTP	200 pF	200 pF
VBST_GMCOMP_OTP	3.9 uS	3.9 uS
VBST_RCOMP_OTP	1000 kOhm	1000 kOhm

VCORE Configuration		
VCORE_OTP	1.50 V	1.50 V
CORE_CTRL_OTP	Valley mode cont	Valley mode control
CORE_MODE_OTP	CCM only	CCM only
CORE_SS_OTP	5 mV/us	5 mV/us
CORE_ILIM_OTP	3.4 A	3.4 A
CORE_PH_OTP	2 Clock Cycles	2 Clock Cycles
COREHS_SR_OTP	Rise = 5 V/ns; Fa	Rise = 5 V/ns; Fall = 2.2 V/ns
CORE_GM_OTP	53 uS	53 uS
CORE_CCOMP_OTP	60 pF	60 pF
CORE_RCOMP_OTP	200 kOhm	200 kOhm
CORE_LSEL_OTP	1 uH	1 uH

MCU: FRDM-KL25Z State: CONNECTED Protocol: SPI Firmware: 0.15 Device Mode: test-mode Color legend: High 🟧 Low 🟦 FS_STATES : 4-Debug entry 13/12/2022 14:35:33

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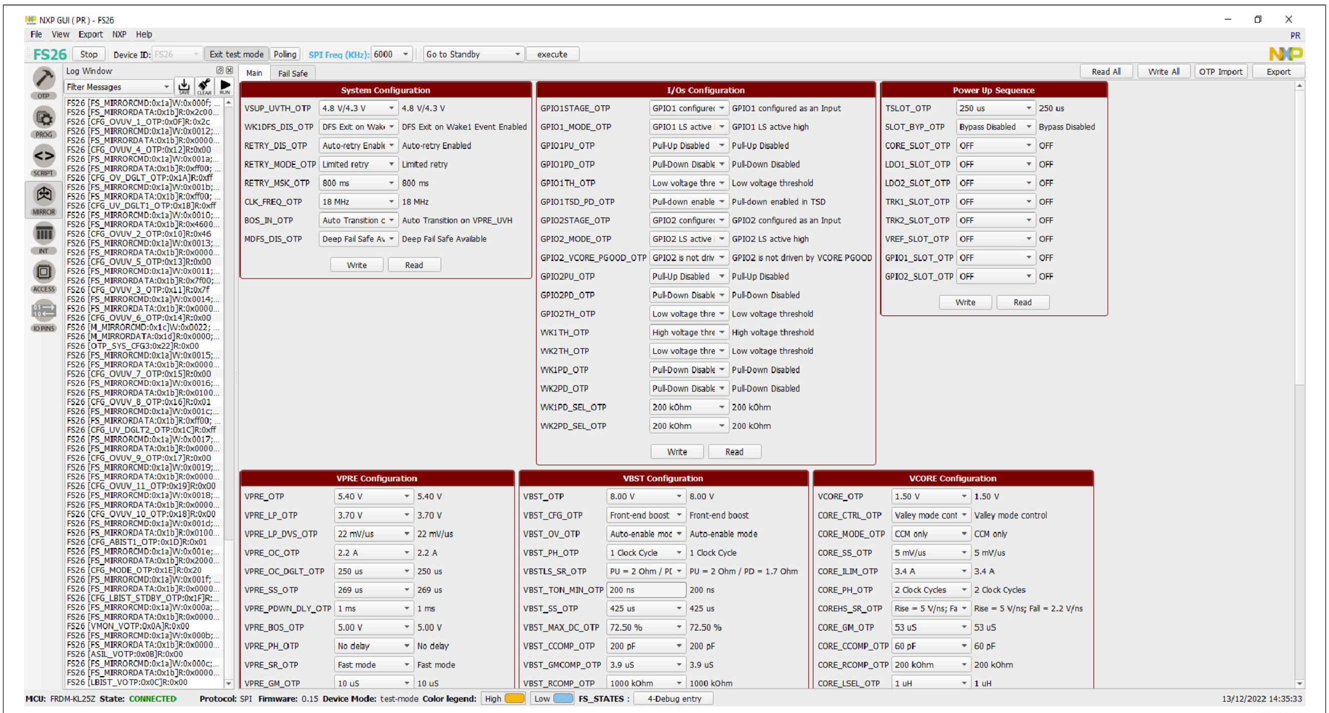
Figure 51. Export option for reference

7.6.4 OTP import to mirror registers

This option is used to import the configuration file previously saved. Click **OTP Import** and select the .txt configuration file previously saved from this tab.



```
FS26 [FS_MIRRORCMD:0x1a]W:0x000f; ...
FS26 [FS_MIRRORDATA:0x1b]R:0x2c00...
FS26 [CFG_OVUV_1_OTP:0x0F]R:0x2c
FS26 [FS_MIRRORCMD:0x1a]W:0x0012;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_4_OTP:0x12]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x001a;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_OV_DGLT_OTP:0x1A]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x001b;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_UV_DGLT1_OTP:0x1B]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x0010;...
FS26 [FS_MIRRORDATA:0x1b]R:0x4600...
FS26 [CFG_OVUV_2_OTP:0x10]R:0x46
FS26 [FS_MIRRORCMD:0x1a]W:0x0013;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_5_OTP:0x13]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0011;...
FS26 [FS_MIRRORDATA:0x1b]R:0x7f00;...
FS26 [CFG_OVUV_3_OTP:0x11]R:0x7f
FS26 [FS_MIRRORCMD:0x1a]W:0x0014;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_6_OTP:0x14]R:0x00
FS26 [M_MIRRORCMD:0x1c]W:0x0022; ...
FS26 [M_MIRRORDATA:0x1d]R:0x0000;...
FS26 [OTP_SYS_CFG3:0x22]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0015;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_7_OTP:0x15]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0016;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0100...
FS26 [CFG_OVUV_8_OTP:0x16]R:0x01
FS26 [FS_MIRRORCMD:0x1a]W:0x001c;...
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; ...
FS26 [CFG_UV_DGLT2_OTP:0x1C]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x0017;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_9_OTP:0x17]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0019;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_11_OTP:0x19]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0018;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_OVUV_10_OTP:0x18]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x001d;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0100...
FS26 [CFG_ABIST1_OTP:0x1D]R:0x01
FS26 [FS_MIRRORCMD:0x1a]W:0x001e;...
FS26 [FS_MIRRORDATA:0x1b]R:0x2000...
FS26 [CFG_MODE_OTP:0x1E]R:0x20
FS26 [FS_MIRRORCMD:0x1a]W:0x001f; ...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [CFG_LBIST_STDBY_OTP:0x1F]R:...
FS26 [FS_MIRRORCMD:0x1a]W:0x000a;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [VMON_VOTP:0x0A]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x000b;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [ASIL_VOTP:0x0B]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x000c;...
FS26 [FS_MIRRORDATA:0x1b]R:0x0000...
FS26 [LBIST_VOTP:0x0C]R:0x00
```

System Configuration

VSUP_UVTH_OTP	4.8 V/4.3 V	4.8 V/4.3 V
WK1DFS_DIS_OTP	DFS Exit on Wak	DFS Exit on Wake1 Event Enabled
RETRY_DIS_OTP	Auto-retry Enabl	Auto-retry Enabled
RETRY_MODE_OTP	Limited retry	Limited retry
RETRY_MSK_OTP	800 ms	800 ms
CLK_FREQ_OTP	18 MHz	18 MHz
BOS_IN_OTP	Auto Transition c	Auto Transition on VPRE_UVH
MDFS_DIS_OTP	Deep Fail Safe Av	Deep Fail Safe Available

I/Os Configuration

GPIO1STAGE_OTP	GPIO1 configure	GPIO1 configured as an Input
GPIO1_MODE_OTP	GPIO1 LS active	GPIO1 LS active high
GPIO1PU_OTP	Pull-Up Disabled	Pull-Up Disabled
GPIO1PD_OTP	Pull-Down Disable	Pull-Down Disabled
GPIO1TH_OTP	Low voltage thre	Low voltage threshold
GPIO1TSD_PD_OTP	Pull-down enable	Pull-down enabled in TSD
GPIO2STAGE_OTP	GPIO2 configure	GPIO2 configured as an Input
GPIO2_MODE_OTP	GPIO2 LS active	GPIO2 LS active high
GPIO2_VCORE_PGOOD_OTP	GPIO2 is not driv	GPIO2 is not driven by VCORE PGOOD
GPIO2PU_OTP	Pull-Up Disabled	Pull-Up Disabled
GPIO2PD_OTP	Pull-Down Disable	Pull-Down Disabled
GPIO2TH_OTP	Low voltage thre	Low voltage threshold
WK1TH_OTP	High voltage thre	High voltage threshold
WK2TH_OTP	Low voltage thre	Low voltage threshold
WK1PD_OTP	Pull-Down Disable	Pull-Down Disabled
WK2PD_OTP	Pull-Down Disable	Pull-Down Disabled
WK1PD_SEL_OTP	200 kOhm	200 kOhm
WK2PD_SEL_OTP	200 kOhm	200 kOhm

Power Up Sequence

TSLOT_OTP	250 us	250 us
SLOT_BYP_OTP	Bypass Disabled	Bypass Disabled
CORE_SLOT_OTP	OFF	OFF
LDO1_SLOT_OTP	OFF	OFF
LDO2_SLOT_OTP	OFF	OFF
TRK1_SLOT_OTP	OFF	OFF
TRK2_SLOT_OTP	OFF	OFF
VREF_SLOT_OTP	OFF	OFF
GPIO1_SLOT_OTP	OFF	OFF
GPIO2_SLOT_OTP	OFF	OFF

VPRE Configuration

VPRE_OTP	5.40 V	5.40 V
VPRE_LP_OTP	3.70 V	3.70 V
VPRE_LP_DVS_OTP	22 mV/us	22 mV/us
VPRE_OC_OTP	2.2 A	2.2 A
VPRE_OC_DGLT_OTP	250 us	250 us
VPRE_SS_OTP	269 us	269 us
VPRE_PDWN_DLY_OTP	1 ms	1 ms
VPRE_BOS_OTP	5.00 V	5.00 V
VPRE_PH_OTP	No delay	No delay
VPRE_SR_OTP	Fast mode	Fast mode
VPRE_GM_OTP	10 uS	10 uS

VBST Configuration

VBST_OTP	8.00 V	8.00 V
VBST_CFG_OTP	Front-end boost	Front-end boost
VBST_OV_OTP	Auto-enable moc	Auto-enable mode
VBST_PH_OTP	1 Clock Cycle	1 Clock Cycle
VBSTLS_SR_OTP	PU = 2 Ohm / PI	PU = 2 Ohm / PD = 1.7 Ohm
VBST_TON_MIN_OTP	200 ns	200 ns
VBST_SS_OTP	425 us	425 us
VBST_MAX_DC_OTP	72.50 %	72.50 %
VBST_CCOMP_OTP	200 pF	200 pF
VBST_GMCOMP_OTP	3.9 uS	3.9 uS
VBST_RCOMP_OTP	1000 kOhm	1000 kOhm

VCORE Configuration

VCORE_OTP	1.50 V	1.50 V
CORE_CTRL_OTP	Valley mode cont	Valley mode control
CORE_MODE_OTP	CCM only	CCM only
CORE_SS_OTP	5 mV/us	5 mV/us
CORE_ILIM_OTP	3.4 A	3.4 A
CORE_PH_OTP	2 Clock Cycles	2 Clock Cycles
COREHS_SR_OTP	Rise = 5 V/ns; Fa	Rise = 5 V/ns; Fall = 2.2 V/ns
CORE_GM_OTP	53 uS	53 uS
CORE_CCOMP_OTP	60 pF	60 pF
CORE_RCOMP_OTP	200 kOhm	200 kOhm
CORE_LSEL_OTP	1 uH	1 uH

MCU: FRDM-KL25Z **State:** CONNECTED **Protocol:** SPI **Firmware:** 0.15 **Device Mode:** test-mode **Color legend:** High 🟨 Low 🟦 **FS_STATES :** 4-Debug entry 13/12/2022 14:35:33

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Figure 52. OTP Import for reference

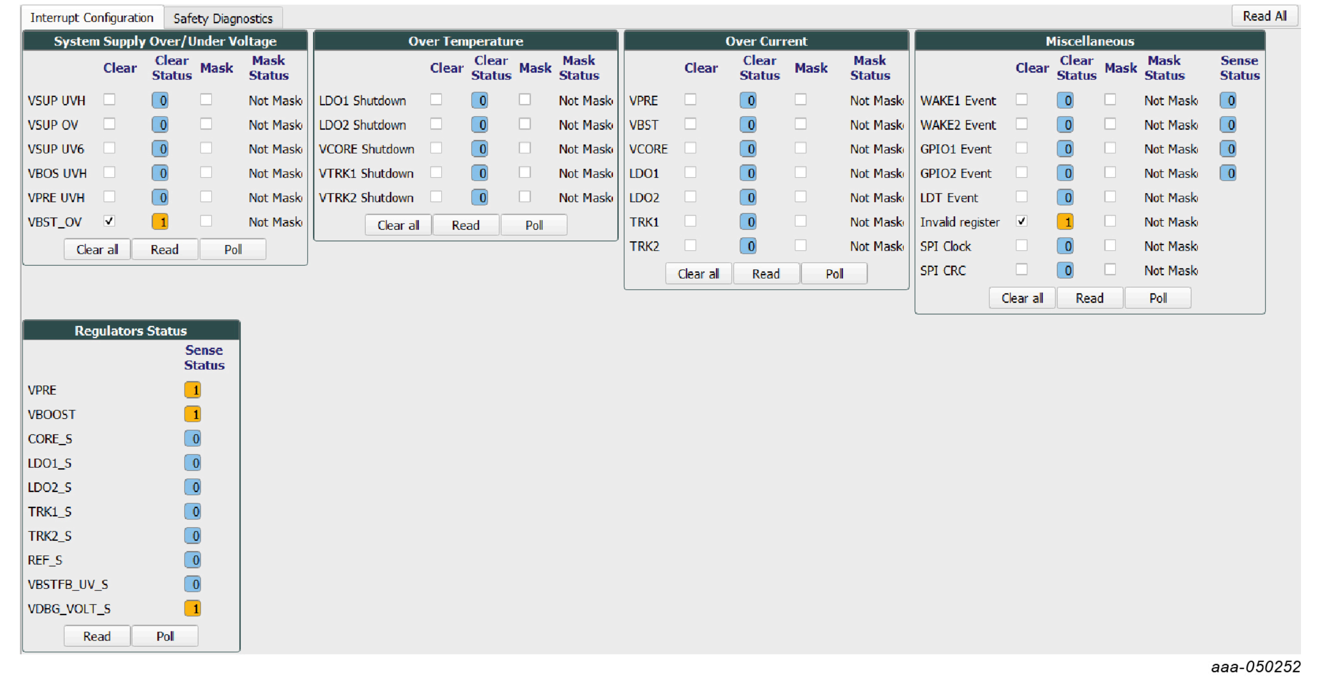
7.7 INT tab

To access the Interrupt Editor window, click Menu → INT or View → Show → Interrupt Editor.

The Interrupt Editor window has two tabs: the Interrupt Configuration tab and the Safety Diagnostic tab.

7.7.1 Interrupt Configuration tab

The Interrupt Configuration tab shown in Figure 53 allows the monitoring of the regulators, the wake inputs, the I/Os, and the communication events or status. It also allows the reading, writing and polling of overvoltage/ undervoltage, overtemperature, and overcurrent.



System Supply Over/Under Voltage

	Clear	Clear Status	Mask	Mask Status
VSUP UVH	□	0	□	Not Mask
VSUP OV	□	0	□	Not Mask
VSUP UV6	□	0	□	Not Mask
VBOS UVH	□	0	□	Not Mask
VPRE UVH	□	0	□	Not Mask
VBST_OV	☑	1	□	Not Mask

Over Temperature

	Clear	Clear Status	Mask	Mask Status
LDO1 Shutdown	□	0	□	Not Mask
LDO2 Shutdown	□	0	□	Not Mask
VCORE Shutdown	□	0	□	Not Mask
VTRK1 Shutdown	□	0	□	Not Mask
VTRK2 Shutdown	□	0	□	Not Mask

Over Current

	Clear	Clear Status	Mask	Mask Status
VPRE	□	0	□	Not Mask
VBST	□	0	□	Not Mask
VCORE	□	0	□	Not Mask
LDO1	□	0	□	Not Mask
LDO2	□	0	□	Not Mask
TRK1	□	0	□	Not Mask
TRK2	□	0	□	Not Mask

Miscellaneous

	Clear	Clear Status	Mask	Mask Status	Sense Status
WAKE1 Event	□	0	□	Not Mask	0
WAKE2 Event	□	0	□	Not Mask	0
GPIO1 Event	□	0	□	Not Mask	0
GPIO2 Event	□	0	□	Not Mask	0
LDT Event	□	0	□	Not Mask	
Invalid register	☑	1	□	Not Mask	
SPI Clock	□	0	□	Not Mask	
SPI CRC	□	0	□	Not Mask	

Regulators Status

	Sense Status
VPRE	1
VBOOST	1
CORE_S	0
LDO1_S	0
LDO2_S	0
TRK1_S	0
TRK2_S	0
REF_S	0
VBSTFB_UV_S	0
VDBG_VOLT_S	1

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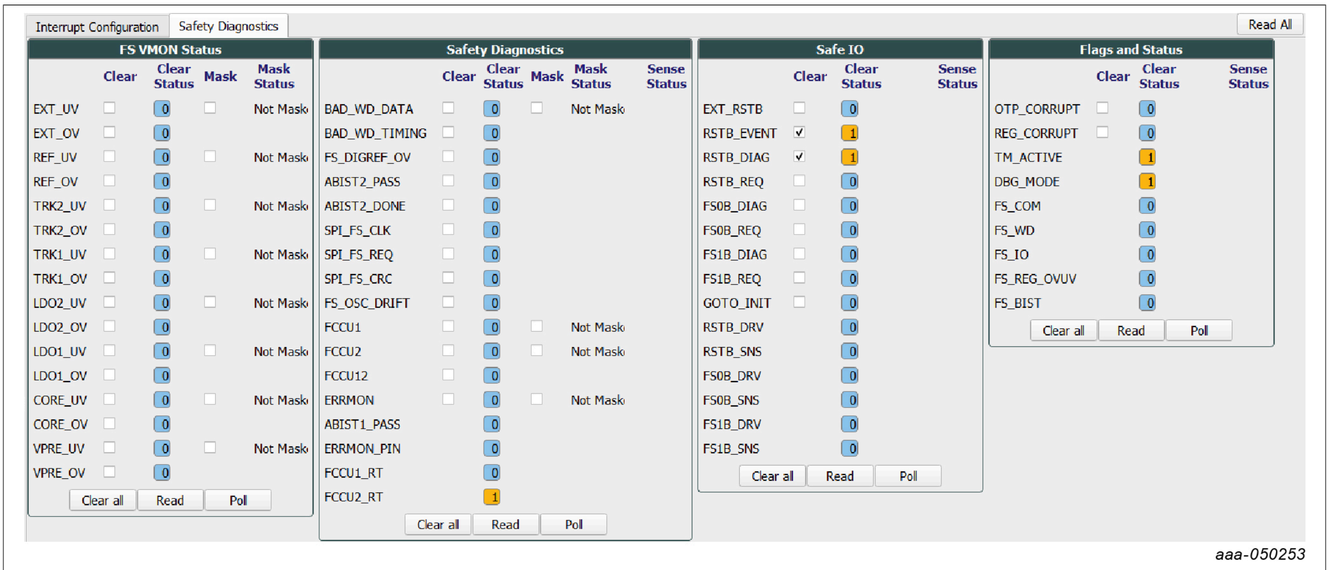
Figure 53. Interrupt Configuration tab

These commands can be used to manage the interrupts:

- **Clear all**: All interrupts in the box are cleared. The user can also click the individual check boxes from the **Clear** column.
- **Read**: Gives the status of all interrupts in the box.
- **Poll**: Reads interrupts' values in a loop.
  A few tips are given below to help the user:
- **Blue** means Low or not activated.
- **Yellow** means High or activated.
- To **mask** a specific interrupt, the user can check the interrupt's box from the **Mask** column.
- Click **Read** on each box to read the current status or **Read All** to update the whole tab.

7.7.2 Safety Diagnostics tab

The Safety Diagnostics tab allows the monitoring of safety events such as VMON status, bad WD, SPI communication errors, FCCU pins, safety outputs, ABIST1 and ABIST2 status.



Interrupt Configuration | Safety Diagnostics | Read All

FS VMON Status

	Clear	Clear Status	Mask	Mask Status
EXT_UV	□	0	□	Not Mask
EXT_OV	□	0		
REF_UV	□	0	□	Not Mask
REF_OV	□	0		
TRK2_UV	□	0	□	Not Mask
TRK2_OV	□	0		
TRK1_UV	□	0	□	Not Mask
TRK1_OV	□	0		
LDO2_UV	□	0	□	Not Mask
LDO2_OV	□	0		
LDO1_UV	□	0	□	Not Mask
LDO1_OV	□	0		
CORE_UV	□	0	□	Not Mask
CORE_OV	□	0		
VPRE_UV	□	0	□	Not Mask
VPRE_OV	□	0		

Clear all | Read | Poll

Safety Diagnostics

	Clear	Clear Status	Mask	Mask Status	Sense Status
BAD_WD_DATA	□	0	□	Not Mask	
BAD_WD_TIMING	□	0			
FS_DIGREF_OV	□	0			
ABIST2_PASS	□	0			
ABIST2_DONE	□	0			
SPI_FS_CLK	□	0			
SPI_FS_REQ	□	0			
SPI_FS_CRC	□	0			
FS_OSC_DRIFT	□	0			
FCCU1	□	0	□	Not Mask	
FCCU2	□	0	□	Not Mask	
FCCU12	□	0			
ERRMON	□	0	□	Not Mask	
ABIST1_PASS		0			
ERRMON_PIN		0			
FCCU1_RT		0			
FCCU2_RT		1			

Clear all | Read | Poll

Safe IO

	Clear	Clear Status	Sense Status
EXT_RSTB	□	0	
RSTB_EVENT	☑	1	
RSTB_DIAG	☑	1	
RSTB_REQ	□	0	
FS0B_DIAG	□	0	
FS0B_REQ	□	0	
FS1B_DIAG	□	0	
FS1B_REQ	□	0	
GOTO_INIT	□	0	
RSTB_DRV		0	
RSTB_SNS		0	
FS0B_DRV		0	
FS0B_SNS		0	
FS1B_DRV		0	
FS1B_SNS		0	

Clear all | Read | Poll

Flags and Status

	Clear	Clear Status	Sense Status
OTP_CORRUPT	□	0	
REG_CORRUPT	□	0	
TM_ACTIVE		1	
DBG_MODE		1	
FS_COM		0	
FS_WD		0	
FS_IO		0	
FS_REG_OVUV		0	
FS_BIST		0	

Clear all | Read | Poll

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Figure 54. Safety Diagnostics tab

ABIST1_PASS yellow means the ABIST1 is done and its status is PASS, since the user can read ‘1’ from its register. '0' or blue after execution means fail.

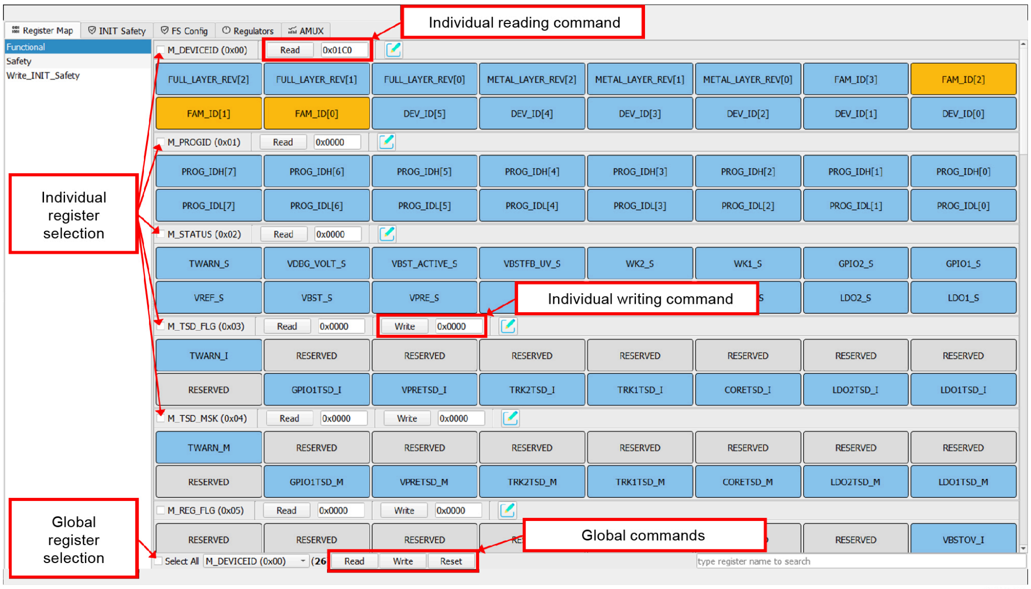
Sense status can only be read (RSTB_DRV, RSTB_SNS, FS0B_DRV, ...).

7.8 Access tab

7.8.1 Register map

All FS2600 SPI registers can be accessed in write and read mode using this tab shown in Figure 55. These registers are divided into three sections:

- **Functional**: Main functional SPI registers (diagnostics, configuration, and controls)
- **Safety**: Safety SPI registers (diagnostics and configuration)
- **Write INIT safety**: Safety registers that can be configured during INIT FS state (for example, WD configuration and WD window)


Register Map
INIT Safety
FS Config
Regulators
AMUX
Functional
Safety
Write_INIT_Safety
Individual reading command
Individual register selection
Individual writing command
Global register selection
Global commands
Select All
Read
Write
Reset
type register name to search

□ M_DEVICEID (0x00)	Read	0x01C0					
FULL_LAYER_REV[2]	FULL_LAYER_REV[1]	FULL_LAYER_REV[0]	METAL_LAYER_REV[2]	METAL_LAYER_REV[1]	METAL_LAYER_REV[0]	FAM_ID[3]	FAM_ID[2]
FAM_ID[1]	FAM_ID[0]	DEV_ID[5]	DEV_ID[4]	DEV_ID[3]	DEV_ID[2]	DEV_ID[1]	DEV_ID[0]
□ M_PROGID (0x01)	Read	0x0000					
PROG_IDH[7]	PROG_IDH[6]	PROG_IDH[5]	PROG_IDH[4]	PROG_IDH[3]	PROG_IDH[2]	PROG_IDH[1]	PROG_IDH[0]
PROG_IDL[7]	PROG_IDL[6]	PROG_IDL[5]	PROG_IDL[4]	PROG_IDL[3]	PROG_IDL[2]	PROG_IDL[1]	PROG_IDL[0]
□ M_STATUS (0x02)	Read	0x0000					
TWARN_S	VDBG_VOLT_S	VBST_ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	GPIO2_S	GPIO1_S
VREF_S	VBST_S	VPRE_S			S	LDO2_S	LDO1_S
□ M_TSD_FLG (0x03)	Read	0x0000	Write	0x0000			
TWARN_I	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
RESERVED	GPIO1TSD_I	VPRETSD_I	TRK2TSD_I	TRK1TSD_I	CORETSD_I	LDO2TSD_I	LDO1TSD_I
□ M_TSD_MSK (0x04)	Read	0x0000	Write	0x0000			
TWARN_M	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
RESERVED	GPIO1TSD_M	VPRETSD_M	TRK2TSD_M	TRK1TSD_M	CORETSD_M	LDO2TSD_M	LDO1TSD_M
□ M_REG_FLG (0x05)	Read	0x0000	Write	0x0000			
RESERVED	RESERVED	RESERVED	RE			RESERVED	VBSTOV_I
□ Select All	M_DEVICEID (0x00)	(26	Read	Write	Reset		

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Figure 55. Register map access

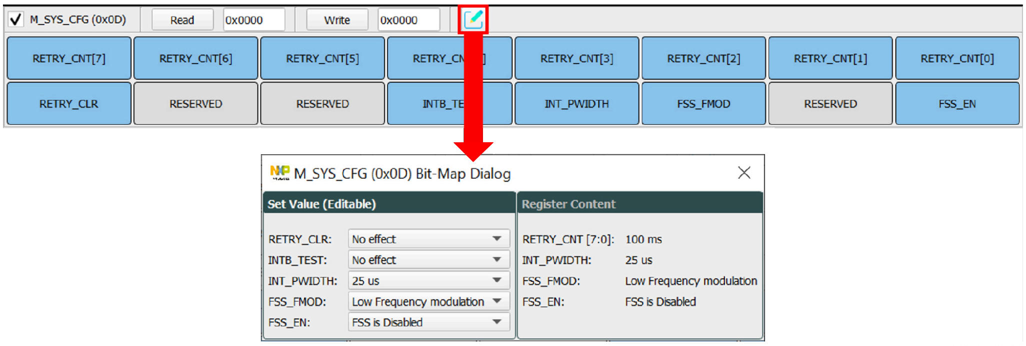
To read the values of a register, click the **READ** button. The value is read from the device and is displayed on a label near the **READ** button. It is also displayed in the log window.

To write the bit values individually, click the desired bit. The corresponding bit button color changes. The value is updated in the log window. Click the **WRITE** button to write to the register. To write the values through a text box near the **WRITE** button, enter the appropriate write value. Then click the **WRITE** button to write to the register.

When registers have been selected, global commands can also be used:

- **WRITE**: Writes data to all the selected register at once.
- **READ**: Reads data back from the selected register at once.
- **RESET**: Resets all the input text boxes to 0x00. Write bits are set to '0'. Change register bit buttons are set to the default setting.

The value can also be written by selecting the Edit option near the **WRITE** button. Bits and corresponding values are displayed in a pop window as shown in Figure 56. Select the options of all write bits, close the input dialog box, and click the **WRITE** button. Selected input combinations are written to the register.



Set Value (Editable)		Register Content	
RETRY_CLR:	No effect	RETRY_CNT [7:0]:	100 ms
INTB_TEST:	No effect	INT_PWIDTH:	25 us
INT_PWIDTH:	25 us	FSS_FMOD:	Low Frequency modulation
FSS_FMOD:	Low Frequency modulation	FSS_EN:	FSS is Disabled
FSS_EN:	FSS is Disabled		

aaa-046952

Figure 56. Bit map dialog

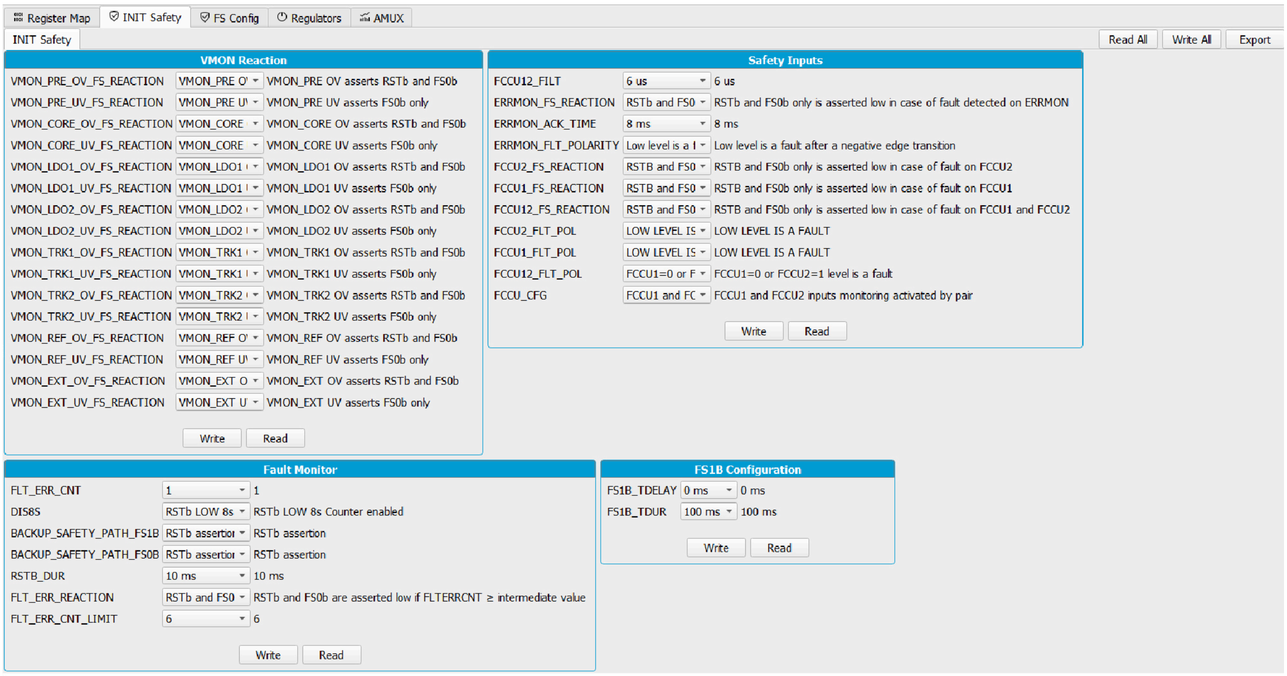
Writing an INIT safety register automatically updates the corresponding NOT register.

7.8.2 INIT safety tab

This tab allows the configuration of a safety output reaction in case of fault for voltage monitoring, FCCU, ERRMON Watchdog monitoring, as shown in Figure 57. See the FS2600 data sheet for a complete description of these registers.

It is required to be in **INIT_FS** state to configure these registers.

Click the combo box controls to select the desired configuration, then click **Write**.



VMON Reaction		
VMON_PRE_OV_FS_REACTION	VMON_PRE O'	VMON_PRE OV asserts RSTb and FS0b
VMON_PRE_UV_FS_REACTION	VMON_PRE U\	VMON_PRE UV asserts FS0b only
VMON_CORE_OV_FS_REACTION	VMON_CORE	VMON_CORE OV asserts RSTb and FS0b
VMON_CORE_UV_FS_REACTION	VMON_CORE	VMON_CORE UV asserts FS0b only
VMON_LDO1_OV_FS_REACTION	VMON_LDO1	VMON_LDO1 OV asserts RSTb and FS0b
VMON_LDO1_UV_FS_REACTION	VMON_LDO1	VMON_LDO1 UV asserts FS0b only
VMON_LDO2_OV_FS_REACTION	VMON_LDO2	VMON_LDO2 OV asserts RSTb and FS0b
VMON_LDO2_UV_FS_REACTION	VMON_LDO2	VMON_LDO2 UV asserts FS0b only
VMON_TRK1_OV_FS_REACTION	VMON_TRK1	VMON_TRK1 OV asserts RSTb and FS0b
VMON_TRK1_UV_FS_REACTION	VMON_TRK1	VMON_TRK1 UV asserts FS0b only
VMON_TRK2_OV_FS_REACTION	VMON_TRK2	VMON_TRK2 OV asserts RSTb and FS0b
VMON_TRK2_UV_FS_REACTION	VMON_TRK2	VMON_TRK2 UV asserts FS0b only
VMON_REF_OV_FS_REACTION	VMON_REF O'	VMON_REF OV asserts RSTb and FS0b
VMON_REF_UV_FS_REACTION	VMON_REF U\	VMON_REF UV asserts FS0b only
VMON_EXT_OV_FS_REACTION	VMON_EXT O	VMON_EXT OV asserts RSTb and FS0b
VMON_EXT_UV_FS_REACTION	VMON_EXT U'	VMON_EXT UV asserts FS0b only

Safety Inputs		
FCCU12_FILT	6 us	6 us
ERRMON_FS_REACTION	RSTb and FS0	RSTb and FS0b only is asserted low in case of fault detected on ERRMON
ERRMON_ACK_TIME	8 ms	8 ms
ERRMON_FLT_POLARITY	Low level is a f	Low level is a fault after a negative edge transition
FCCU2_FS_REACTION	RSTB and FS0	RSTB and FS0b only is asserted low in case of fault on FCCU2
FCCU1_FS_REACTION	RSTB and FS0	RSTB and FS0b only is asserted low in case of fault on FCCU1
FCCU12_FS_REACTION	RSTB and FS0	RSTB and FS0b only is asserted low in case of fault on FCCU1 and FCCU2
FCCU2_FLT_POL	LOW LEVEL IS	LOW LEVEL IS A FAULT
FCCU1_FLT_POL	LOW LEVEL IS	LOW LEVEL IS A FAULT
FCCU12_FLT_POL	FCCU1=0 or F	FCCU1=0 or FCCU2=1 level is a fault
FCCU_CFG	FCCU1 and FC	FCCU1 and FCCU2 inputs monitoring activated by pair

Fault Monitor		
FLT_ERR_CNT	1	1
DIS8S	RSTb LOW 8s	RSTb LOW 8s Counter enabled
BACKUP_SAFETY_PATH_FS1B	RSTb assertion	RSTb assertion
BACKUP_SAFETY_PATH_FS0B	RSTb assertion	RSTb assertion
RSTB_DUR	10 ms	10 ms
FLT_ERR_REACTION	RSTb and FS0	RSTb and FS0b are asserted low if FLTERRCNT ≥ intermediate value
FLT_ERR_CNT_LIMIT	6	6

FS1B Configuration		
FS1B_TDELAY	0 ms	0 ms
FS1B_TDUR	100 ms	100 ms

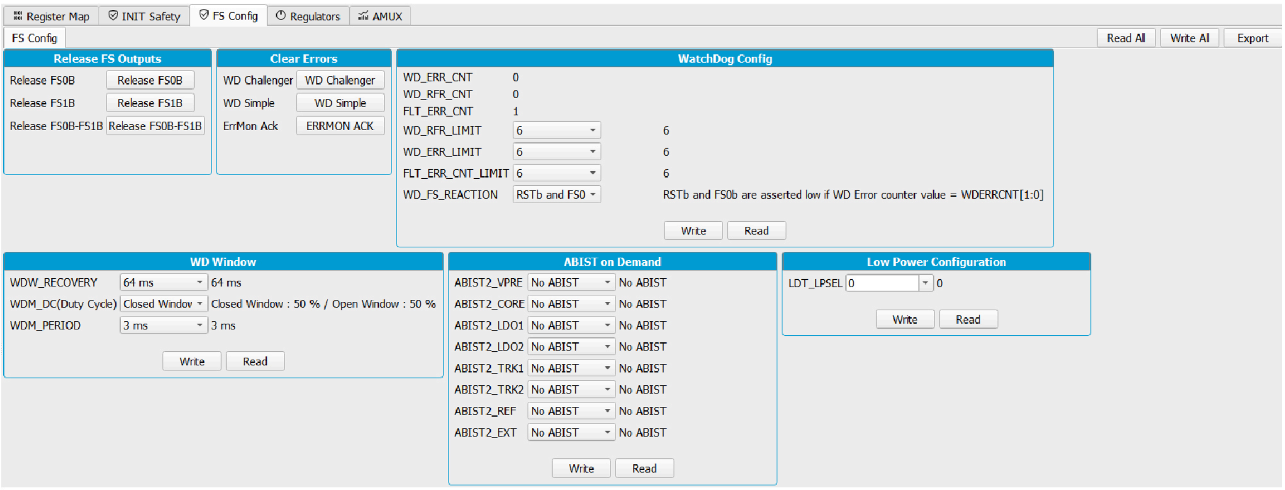
aaa-050255

Figure 57. INIT safety tab

Read All and **Write All** buttons are implemented to facilitate configuration.

7.8.3 FS Config tab

This tab helps to configure safety features, such as Watchdog and Fault Error counter. Click **Read All** to get the current configuration.



Release FS Outputs

Release FS0B
Release FS1B
Release FS0B-FS1B

Clear Errors

WD Challenger
WD Simple
ErrMon Ack

WatchDog Config

WD_ERR_CNT	0	
WD_RFR_CNT	0	
FLT_ERR_CNT	1	
WD_RFR_LIMIT	6	6
WD_ERR_LIMIT	6	6
FLT_ERR_CNT_LIMIT	6	6
WD_FS_REACTION	RSTb and FS0	RSTb and FS0b are asserted low if WD Error counter value = WDERRCNT[1:0]

WD Window

WDW_RECOVERY	64 ms	64 ms
WDM_DC(Duty Cycle)	Closed Window	Closed Window : 50 % / Open Window : 50 %
WDM_PERIOD	3 ms	3 ms

ABIST on Demand

ABIST2_VPRE	No ABIST	No ABIST
ABIST2_CORE	No ABIST	No ABIST
ABIST2_LDO1	No ABIST	No ABIST
ABIST2_LDO2	No ABIST	No ABIST
ABIST2_TRK1	No ABIST	No ABIST
ABIST2_TRK2	No ABIST	No ABIST
ABIST2_REF	No ABIST	No ABIST
ABIST2_EXT	No ABIST	No ABIST

Low Power Configuration

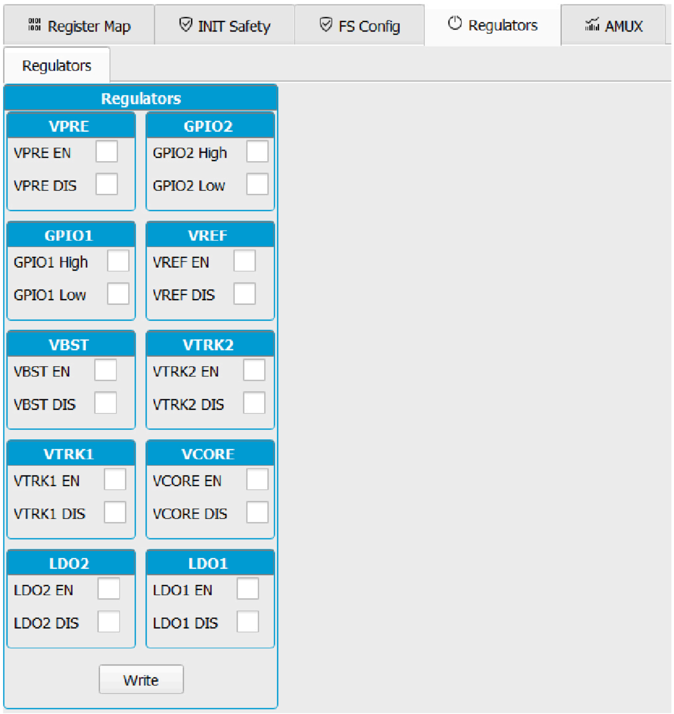
LDT_LPSEL	0	0

aaa-050256

Figure 58. FS Config tab

7.8.4 Regulators tab

The regulator tab shown in Figure 59 is used to configure the FS2600 SMPS, LDO, or GPIOs. SPI can enable or disable each regulator. Check the enable (EN) or disable (DIS) box, then click the **Write** button. These registers do not provide regulator status. The VPRE regulator can be only enabled or disabled in test mode.



VPRE: VPRE EN ☐ VPRE DIS ☐

GPIO2: GPIO2 High ☐ GPIO2 Low ☐

GPIO1: GPIO1 High ☐ GPIO1 Low ☐

VREF: VREF EN ☐ VREF DIS ☐

VBST: VBST EN ☐ VBST DIS ☐

VTRK2: VTRK2 EN ☐ VTRK2 DIS ☐

VTRK1: VTRK1 EN ☐ VTRK1 DIS ☐

VCORE: VCORE EN ☐ VCORE DIS ☐

LDO2: LDO2 EN ☐ LDO2 DIS ☐

LDO1: LDO1 EN ☐ LDO1 DIS ☐

aaa-046955

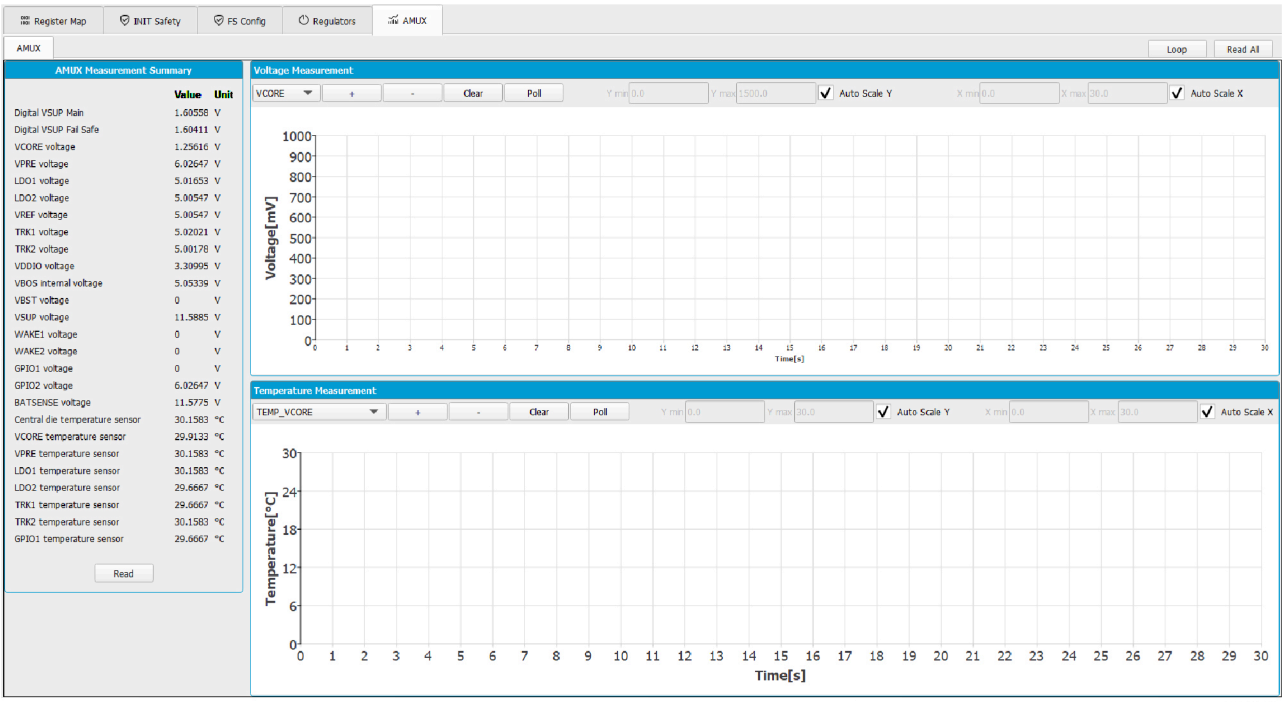
Figure 59. Regulators tab

7.8.5 AMUX tab

The AMUX tab shown in Figure 60 allows the selection of an AMUX pin channel. The pin channel gets its current value by using the KL25Z AMUX ADC pin. The user can do a single read, or display various channels dynamically on the voltage or temperature graph.

The displayed values already apply the divider and temperature formulas. Voltage regulators are also monitored independently on the KL25Z ADC pins.

To use the dynamic graph, select the channel then click the **+** button to add to the graph. To start polling, click the **Poll** button. Click the **Poll** button again to stop measurements.



AMUX Measurement Summary

	Value	Unit
Digital VSUP Main	1.60558	V
Digital VSUP Fail Safe	1.60411	V
VCORE voltage	1.25616	V
VPRE voltage	6.02647	V
LDO1 voltage	5.01653	V
LDO2 voltage	5.00547	V
VREF voltage	5.00547	V
TRK1 voltage	5.02021	V
TRK2 voltage	5.00178	V
VDDIO voltage	3.30995	V
VBOS internal voltage	5.05339	V
VBST voltage	0	V
VSUP voltage	11.5885	V
WAKE1 voltage	0	V
WAKE2 voltage	0	V
GPIO1 voltage	0	V
GPIO2 voltage	6.02647	V
BATSENSE voltage	11.5775	V
Central die temperature sensor	30.1583	°C
VCORE temperature sensor	29.9133	°C
VPRE temperature sensor	30.1583	°C
LDO1 temperature sensor	30.1583	°C
LDO2 temperature sensor	29.6667	°C
TRK1 temperature sensor	29.6667	°C
TRK2 temperature sensor	30.1583	°C
GPIO1 temperature sensor	29.6667	°C

Voltage Measurement: VCORE; Y min 0.0; Y max 1500.0; ☑ Auto Scale Y; X min 0.0; X max 30.0; ☑ Auto Scale X

Temperature Measurement: TEMP_VCORE; Y min 0.0; Y max 30.0; ☑ Auto Scale Y; X min 0.0; X max 30.0; ☑ Auto Scale X

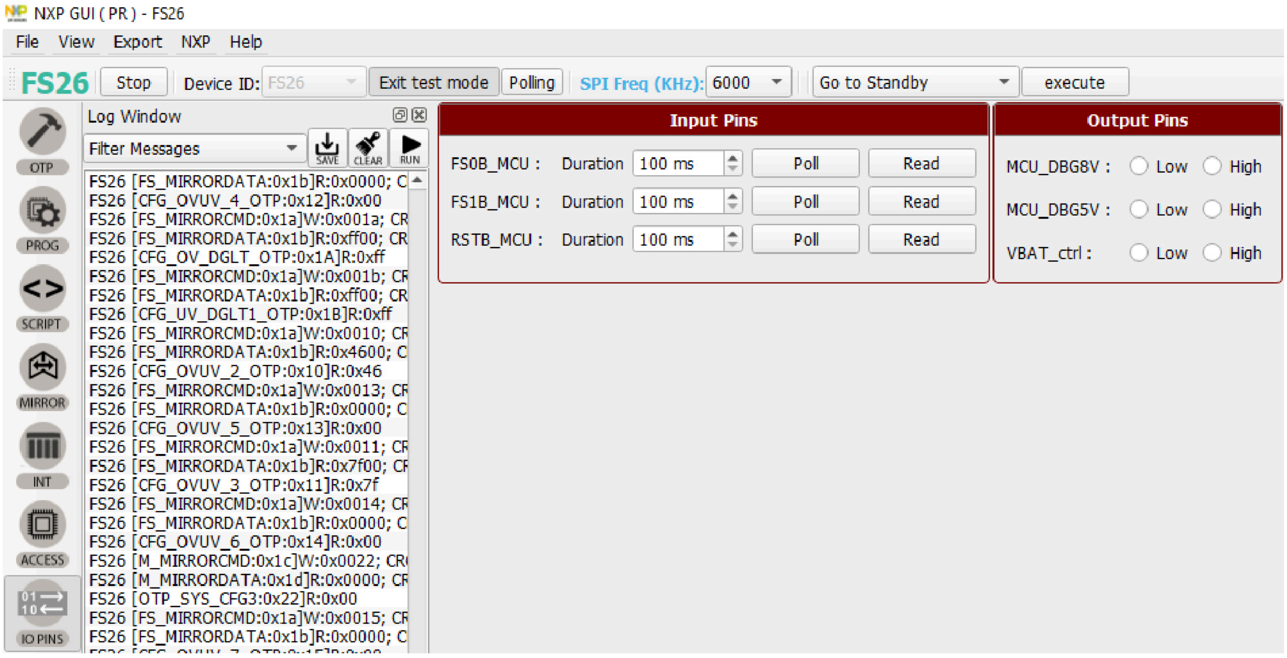
aaa-050257

Figure 60. AMUX measurements

7.9 I/O pins tab

This section can control some I/Os connected to the KL25Z plugged-in Freedom. It can read the device safety outputs externally, or control different voltage sources in order to apply sequences to apply Debug mode without moving any switches.

The input pins are the pins that can be read from the MCU. They are input pins from the MCU point of view. This section contains the safety outputs FS0B, FS1B, and RSTB. It can be read once with the **Read** button, or the user can select at which frequency the user wants to the read the pins. Select the duration, then start polling with the **Poll** button.



Device ID: FS26

SPI Freq (KHz): 6000

Go to Standby

Filter Messages

```
FS26 [FS_MIRRORDATA:0x1b]R:0x0000; C
FS26 [CFG_OVUV_4_OTP:0x12]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x001a; CR
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; CR
FS26 [CFG_OV_DGLT_OTP:0x1A]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x001b; CR
FS26 [FS_MIRRORDATA:0x1b]R:0xff00; CR
FS26 [CFG_UV_DGLT1_OTP:0x1B]R:0xff
FS26 [FS_MIRRORCMD:0x1a]W:0x0010; CR
FS26 [FS_MIRRORDATA:0x1b]R:0x4600; C
FS26 [CFG_OVUV_2_OTP:0x10]R:0x46
FS26 [FS_MIRRORCMD:0x1a]W:0x0013; CR
FS26 [FS_MIRRORDATA:0x1b]R:0x0000; C
FS26 [CFG_OVUV_5_OTP:0x13]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0011; CR
FS26 [FS_MIRRORDATA:0x1b]R:0x7f00; CR
FS26 [CFG_OVUV_3_OTP:0x11]R:0x7f
FS26 [FS_MIRRORCMD:0x1a]W:0x0014; CR
FS26 [FS_MIRRORDATA:0x1b]R:0x0000; C
FS26 [CFG_OVUV_6_OTP:0x14]R:0x00
FS26 [M_MIRRORCMD:0x1c]W:0x0022; CR
FS26 [M_MIRRORDATA:0x1d]R:0x0000; CR
FS26 [OTP_SYS_CFG3:0x22]R:0x00
FS26 [FS_MIRRORCMD:0x1a]W:0x0015; CR
FS26 [FS_MIRRORDATA:0x1b]R:0x0000; C
```

FS0B_MCU : Duration 100 ms

FS1B_MCU : Duration 100 ms

RSTB_MCU : Duration 100 ms

MCU_DBG8V : ○ Low ○ High

MCU_DBG5V : ○ Low ○ High

VBAT_ctrl : ○ Low ○ High

aaa-050258

Figure 61. I/O pins tab

The output pins are thresholds that can be controlled with the MCU. These pins are described in the FS26 Hardware User Manuals UM11503 and UM11504.

- MCU_DBG8V: 8 V on DEBUG pin
- MCU_DBG5V: 5 V on DEBUG pin
- VBAT_Ctrl: open or close VBAT power supply

They can be used instead of the manual switches SW6 and SW7. In order to use MCU_DBG5V and MCU_DBG8V for DEBUG pin control, J13 must be set for Auto mode (J13 position 3-2). Select **High** or **Low** to control the pins. The default is **Low**.

In order to use VBAT_Ctrl, the jumper JP1 next to the VBAT switch must be off. Once JP1 is removed, use VBAT_Ctrl instead of SW1 to turn the power supply on or off.

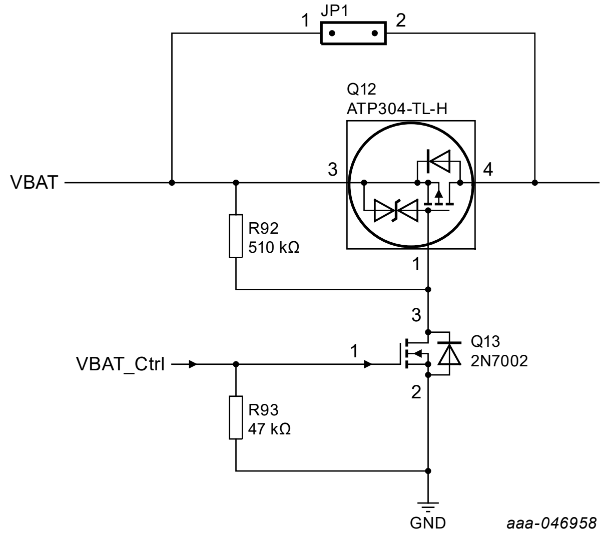


Figure 62. VBAT_Ctrl and JP1 schematic view

These pins are also accessible from the script editor and can be used to create script sequences.

8 Using an FS26 evaluation board

Before starting the process, consult the development board scheme and the hardware user manual to configure the required use case.

Learn about OTP before operating with the device. The device has a high level of flexibility due to the parameter configurations available in the OTP. It impacts the functionality of the device. It is key to understand how OTP parameters can be programmed, the interaction with mirror registers, and the FS2600 SoC.

The OTP-related operations can only be performed in OTP mode (Emulation or programming). When using emulation, the device loses the configuration when the power supply is switched off, when the device enters deep fail-safe, or when it enters standby mode.

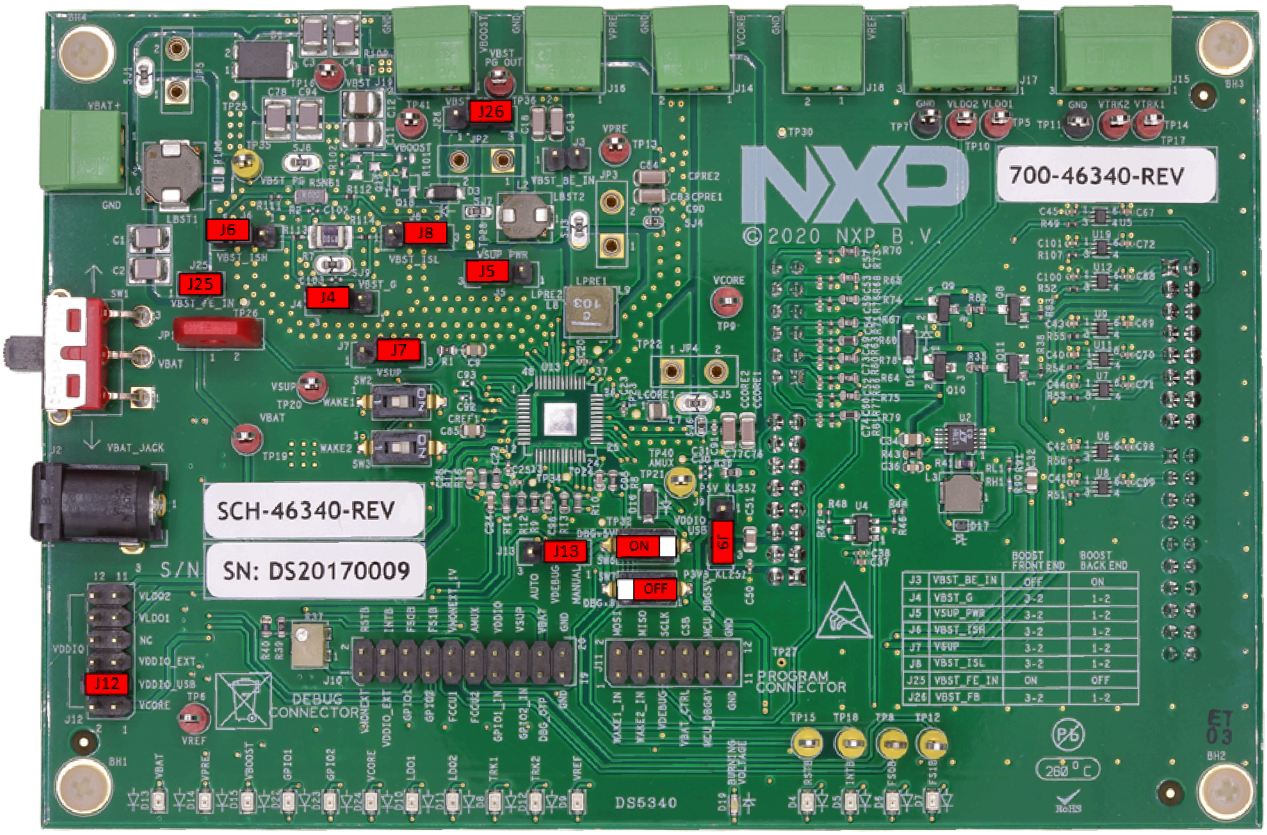
Once the NXP GUI is installed (Section 5), follow these instructions for a quick power up (Section 8.1), debug (Section 8.2), programming, or to enter the various operating modes (Section 8.3, Section 8.7, Section 8.8) of the FS26 SBC.

8.1 Power up

If the FS26 device contains an OTP configuration, connect a power supply to the VBAT Phoenix connector or the VBAT jack connector. See Section "VBAT connectors" from the hardware user manual.

NXP recommends setting the power supply to an initial value of 12 V and limiting the current to 1.0 A.

Make sure the board has the correct jumper configuration. Every kit is delivered with a default configuration shown in Figure 63. This configuration is suitable for a boost in front-end topology.

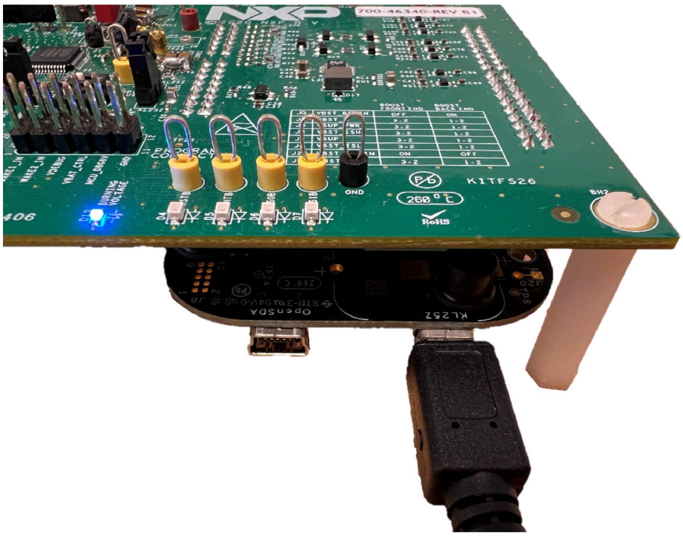


		BOOST FRONT END	BOOST BACK END
J3	VBST_BE_IN	OFF	ON
J4	VBST_G	3-2	1-2
J5	VSUP_PWR	3-2	1-2
J6	VBST_ISH	3-2	1-2
J7	VSUP	3-2	1-2
J8	VBST_ISL	3-2	1-2
J25	VBST_FE_IN	ON	OFF
J26	VBST_FB	3-2	1-2

aaa-050259

Figure 63. Jumpers default configuration

Verify that the KL25Z is plugged in, as well as the USB cable on the KL25Z USB connector side. Connecting the USB cable is important, for these reasons: It enables communication with the NXP GUI, provides voltages and references to some circuits on the board, and generates the VDDIO reference for the IC (J12 is set to VDDIO_USB by default).



aaa-050260

Figure 64. USB cable connection

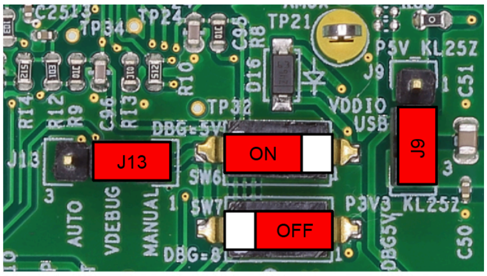
After validating or considering all the previous statements, use switch SW1 to power on the board.

If the OTP configuration has many safety features enabled, the device may restart or power off after a few seconds. To prevent this, enter Debug mode to waive some of those features.

8.2 Debug mode entry

The Debug mode is intended for MCU programming (MCU flash mode) and software debugging. During the power-up sequence, the Fail-safe state machine starts in Debug mode and goes directly to the INIT_FS state. To enter Debug mode without first entering OTP Emulation mode, follow the next steps once the kit is ready:

1. Make sure the device is powered off (SW1 in middle position).
2. Turn on SW6 to apply VDBG (~5.0 V) to the DEBUG pin. Make sure the jumper J13 has the right configuration. The default is **Manual**.

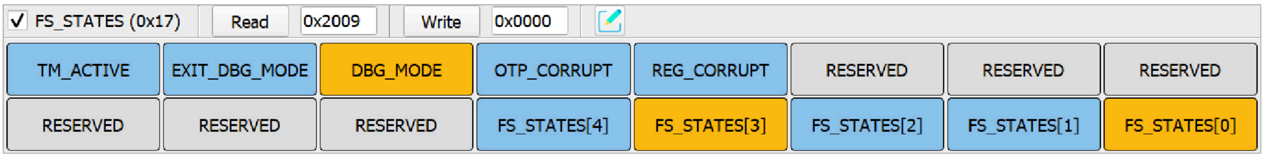


aaa-050261

Figure 65. Jumpers and switches configuration for Debug mode entry

3. Power on VBAT (SW1) and the device enters Debug mode. In this mode, the Watchdog is disabled, the RSTB 8 s counter is disabled, and FS0B is low and cannot be released.

4. To check that the device is in Debug mode, use the NXP GUI register map window (ACCESS tab) to read the DBG_MODE bit in the FS_STATES register (latched information) or VDBG_VOLT_S in M_STATUS (real-time information).

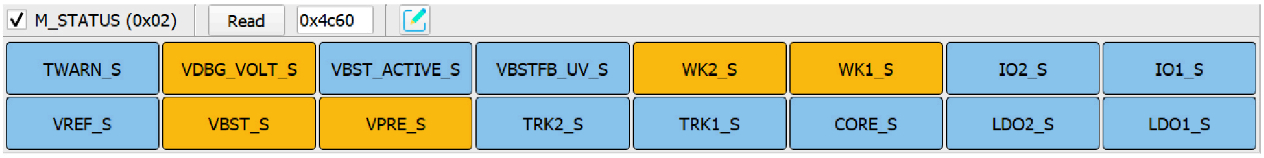


☑ FS_STATES (0x17) Read 0x2009 Write 0x0000

TM_ACTIVE	EXIT_DBG_MODE	DBG_MODE	OTP_CORRUPT	REG_CORRUPT	RESERVED	RESERVED	RESERVED
RESERVED	RESERVED	RESERVED	FS_STATES[4]	FS_STATES[3]	FS_STATES[2]	FS_STATES[1]	FS_STATES[0]

aaa-046962

Figure 66. DBG_MODE bit in FS_STATES register



☑ M_STATUS (0x02) Read 0x4c60

TWARN_S	VDBG_VOLT_S	VBST_ACTIVE_S	VBSTFB_UV_S	WK2_S	WK1_S	IO2_S	IO1_S
VREF_S	VBST_S	VPRE_S	TRK2_S	TRK1_S	CORE_S	LDO2_S	LDO1_S

aaa-046963

Figure 67. VDBG_VOLT_S bit in M_STATUS register

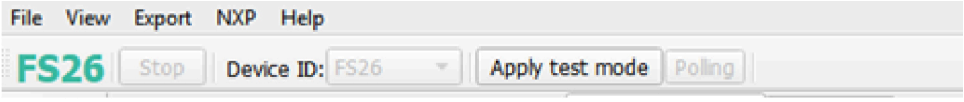
8.3 Test mode entry

To enter test mode, the device must be in Debug mode. Test mode can be accessed by writing the appropriate key sequences.

Access Test mode from the NXP GUI device manager, or write the keys in the script editor.

From device manager:

Click **Apply test mode** to send the Main and Fail-safe test mode entry keys.



aaa-046964

Figure 68. Apply test mode

From script editor:

Copy and paste the keys in the script editor:

// Main Test mode entry

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0000

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xD5A7

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xB8EE

SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0F37

//Fail Safe Test mode entry

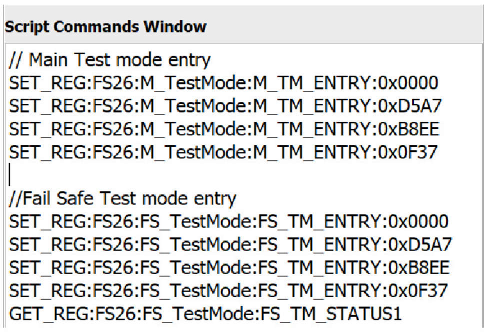
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0000

SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xD5A7

SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xB8EE

SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0F37

GET_REG:FS26:FS_TestMode:FS_TM_STATUS1



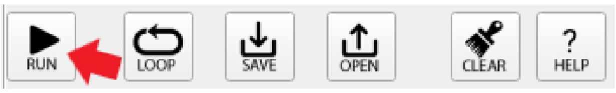
Script Commands Window

```
// Main Test mode entry
SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0000
SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xD5A7
SET_REG:FS26:M_TestMode:M_TM_ENTRY:0xB8EE
SET_REG:FS26:M_TestMode:M_TM_ENTRY:0x0F37

//Fail Safe Test mode entry
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0000
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xD5A7
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0xB8EE
SET_REG:FS26:FS_TestMode:FS_TM_ENTRY:0x0F37
GET_REG:FS26:FS_TestMode:FS_TM_STATUS1
```

aaa-046965

Click **Run** script.



aaa-046966

8.4 Emulate an OTP configuration

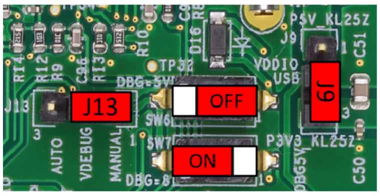
OTP mode is intended for OTP emulation and OTP programming. When an OTP configuration is emulated, the configuration remains available until the POR of the digital circuitry. The Fail-safe configuration is lost in Low Power mode (LPOFF mode or Standby mode) since the Fail-safe digital is off in these modes. The Main digital configuration is lost when VSUP is removed, which means $V_{BOS} < V_{BOS\_POR}$.

During the power-up sequence, the Main and the Fail-safe state machines stops prior to starting the regulators, waiting for SPI communication to send an OTP configuration to the device. When the OTP configuration is complete, the Fail-safe state machine starts in Debug mode when the voltage at the DEBUG pin is below V_{NORM_max} (NXP recommends applying 0 V or GND).

Before starting, make sure that the power conditions from Section 8.1 are valid.

If not in OTP Emulation mode:

1. Ensure the device is powered off (SW1 in middle position).
2. Turn on SW7 to apply ~8 V to the DEBUG pin. Make sure the jumper J13 has the right configuration. The default is **Manual**.



aaa-046967

Figure 69. Jumpers and switches configuration for OTP emulation mode entry

3. Power on VBAT (SW1) and the device enters OTP Emulation mode. The status of the LEDs should be as shown in Figure 70.

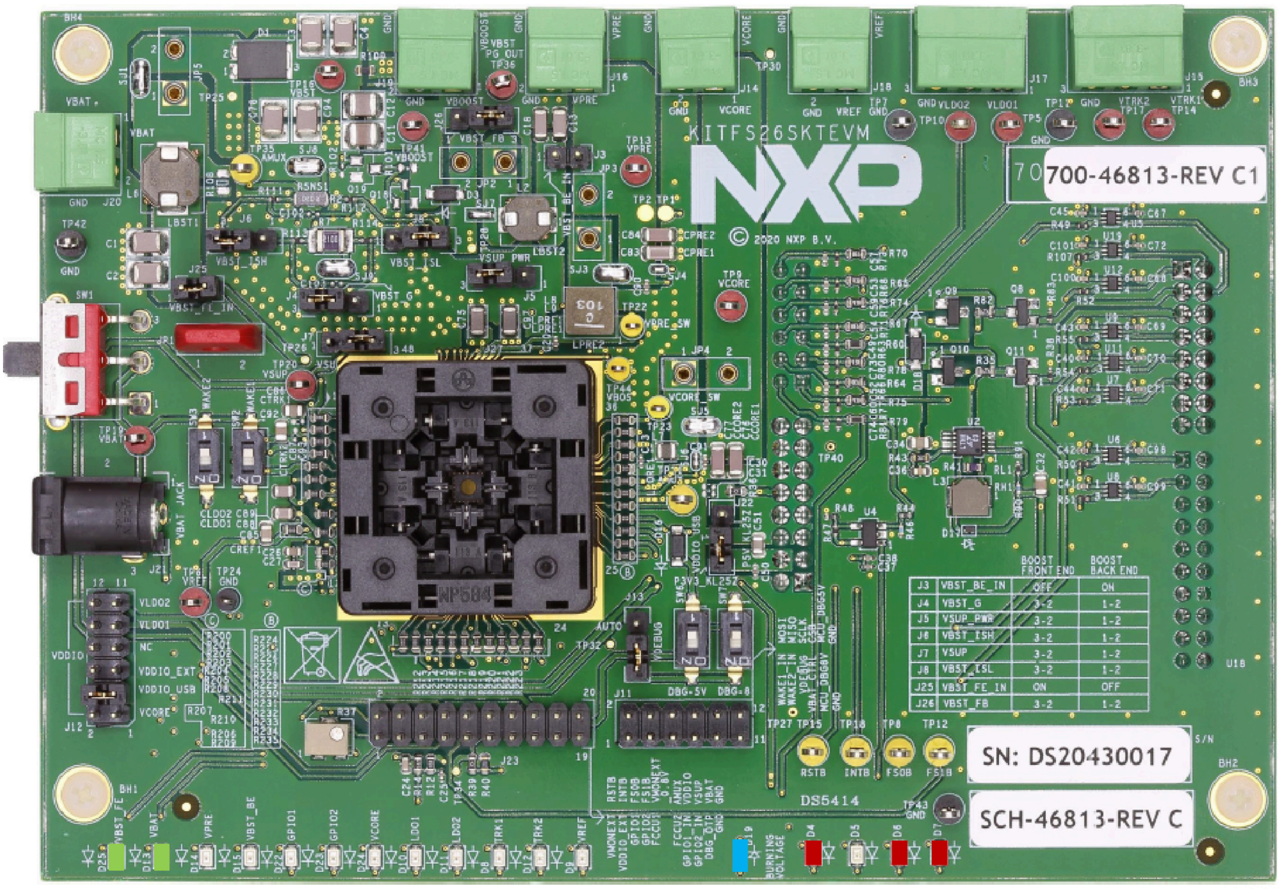
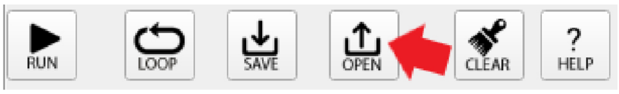


Figure 70. OTP emulation mode LEDs status

If already in OTP Emulation mode:

1. Open the NXP GUI.
2. Connect the device.
3. Open the script editor.



4. Open the provided or created OTP configuration script (TBB) to load into the mirror registers.

A TBB script usually contains the test mode entry keys. If they are not present in the script, see Section 8.3 to enter test mode.

After running the script, read the mirror registers to verify the loaded OTP configuration in the OTP Mirrors tab. Turn the SW7 off to apply 0 V on the DEBUG pin in order to start the power-up sequence and move to the **INIT_FS** state.

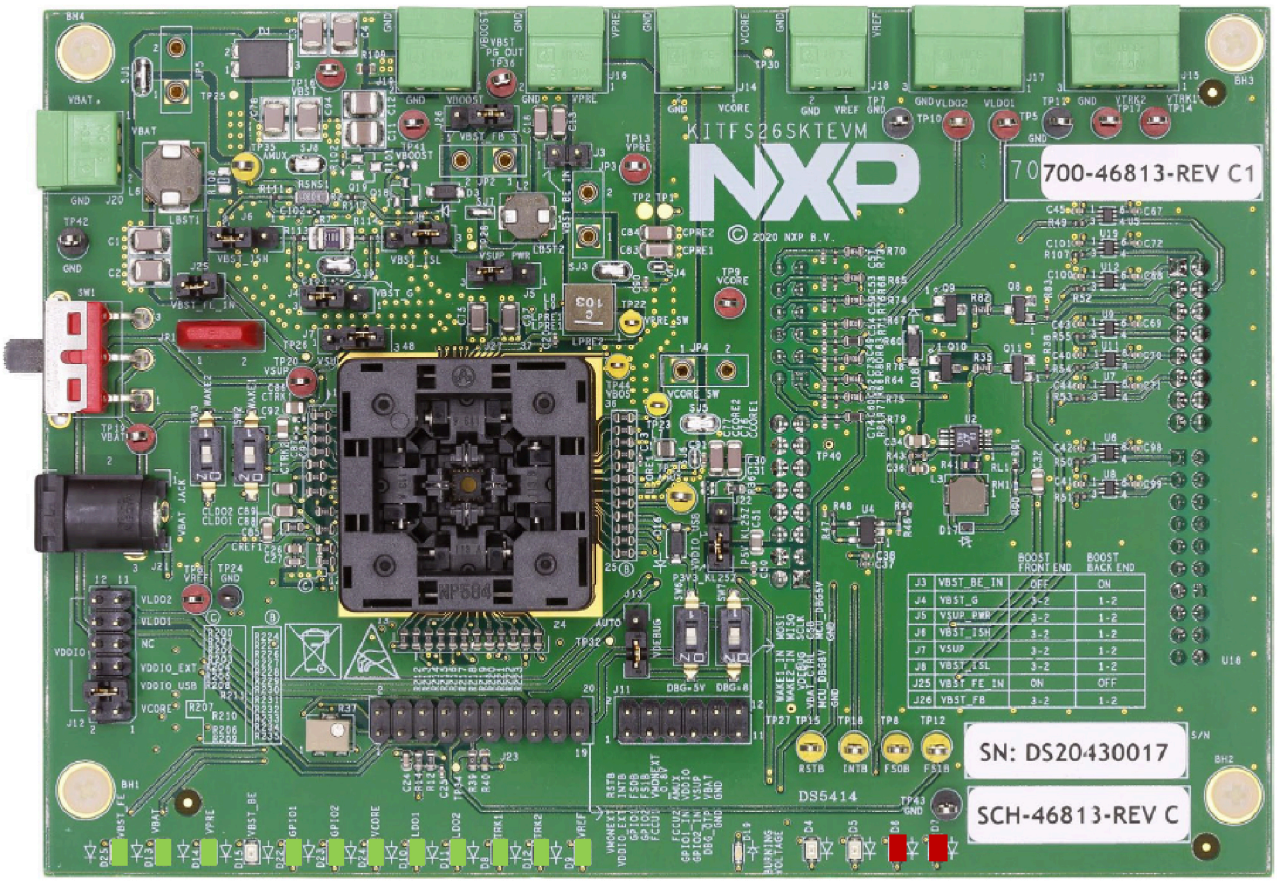
8.5 Programming the device with an OTP configuration

Instructions in this section are intended to burn an OTP configuration permanently into the fuses. The device sectors can be programmed only **one time**. Make sure that sectors are available.

The user can program an OTP configuration from the **Device Programming** tab or from the **Script editor**. See Section 7.4.

1. If not in OTP Emulation mode, see Section 8.4.
2. Apply **test mode**.
3. Go to the Device programming tab (**PROG**) on the left panel.
4. Click **Read** to get the device current fuse box status.
5. Click **Browse** and select the desired OTP configuration script.
6. Click **Program** to initiate the device programming.
7. A window appears to ask the user to turn off SW6 and SW7. Proceed to apply 0 V at the DEBUG pin.
8. OTP programming is now complete. The device has started and is now in the **INIT_FS** state.

Enabled regulators should have their respective LEDs turned on. See Figure 71.



aaa-046970

Figure 71. Status of LEDs once OTP programming is complete

Note: *Regulators LEDs status depends on the OTP configuration used.*

8.6 Go to INIT_FS

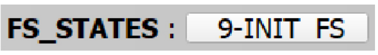
Use these instructions before powering up the device, to get to the INIT_FS state from Debug mode or from OTP Emulation mode.

In **Debug mode**:

1. Device is powered off (SW1 in the middle position).
2. Switch on the SW6 to access Debug mode.
3. Power on the device (using SW1).
4. If no programmed or emulated OTP configuration is preloaded, only VPRE will turn on. See Section 8.4 or Section 8.5 for more details.
5. Power-up sequence is complete and the device is now in INIT_FS state. The user can verify this from the Micro and Device Status bar.

In **OTP Emulation mode**:

1. Device is powered off (SW1 in the middle position).
2. Switch on the SW7 to access OTP Emulation mode.
3. Power on the device (using SW1).
4. The device state machines stop to Debug entry state (see the Micro and Device Status bar).
5. If no programmed or emulated OTP configuration is preloaded, only VPRE will turn on. See Section 8.4 or Section 8.5 for more details.
6. Turn off SW7 (0 V on DEBUG pin) to allow the state machines to resume. The device follows its power-up sequence according to the programmed or emulated OTP configuration.
7. Power-up sequence is complete and device is now in INIT_FS state. The user can verify this from the Micro and Device Status bar.



FS_STATES : 9-INIT_FS

aaa-046971

Figure 72. INIT-FS state

8.7 Go to Normal mode

To enter Normal mode from the GUI, the user must be in Debug mode and in INIT_FS state. When using the simple Watchdog (WD), the user can send a script to release the device safety output pins FS0B and FS1B. If the Watchdog is set to challenger, the sequence must be sent manually.

Using the Script editor

1. Once in INIT_FS state, the user must verify ABIST1 is PASS from the Safety diagnostics tab.
2. Configure or check the Watchdog type from the Mirrors tab.
3. Use one of the following scripts to release the safety output pins. Use script A for simple Watchdog or script B for challenger Watchdog. The script to release the safety output pins is available in the device manager Script tab: from Script editor tab → Generator → Safety outputs release → Run.
   a. Sequence to enter Normal mode with a simple Watchdog:
      ```
      //INIT FS and simple WD enabled required
      //Open WD window
      SET_REG:FS26:Safety:FS_WDW_DURATION:0x008B
      SET_REG:FS26:Safety:FS_NOT_WDW_DURATION:0xF144
      //Send 1st good wd refresh to close INIT window
      SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
      //clean fault error counter
      SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
      ```

```
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5AB2
//Exit dbg mode
SET_REG:FS26:Safety:FS_STATES:0x4000
//release FS0B and FS1B
SET_REG:FS26:Safety:FS_RELEASE_FS0B_FS1B:0xB2A5
```

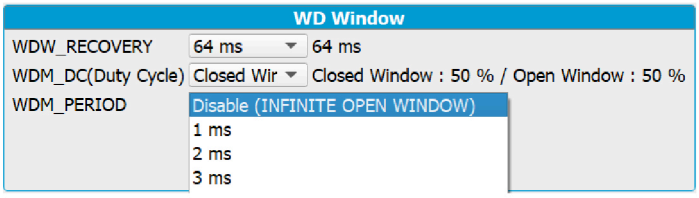
b. Sequence to enter Normal mode with a challenger Watchdog:

```
//INIT FS and WD Challenger required
//Open WD window
SET_REG:FS26:Safety:FS_WDW_DURATION:0x008B
SET_REG:FS26:Safety:FS_NOT_WDW_DURATION:0xF144
//Send 1st WD refresh to close INIT window
SET_REG:FS26:Safety:FS_WD_ANSWER:0xa54d
//clean fault error counter
SET_REG:FS26:Safety:FS_WD_ANSWER:0x4a9a
SET_REG:FS26:Safety:FS_WD_ANSWER:0x9535
SET_REG:FS26:Safety:FS_WD_ANSWER:0x2a6a
SET_REG:FS26:Safety:FS_WD_ANSWER:0x54d4
SET_REG:FS26:Safety:FS_WD_ANSWER:0xa9a9
SET_REG:FS26:Safety:FS_WD_ANSWER:0x5353
//Exit dbg mode
SET_REG:FS26:Safety:FS_STATES:0x4000
//release FS0B and FS1B
SET_REG:FS26:Safety:FS_RELEASE_FS0B_FS1B:0xA565
```

Sending commands manually

To release the safety output pins manually and step by step, proceed with the following instructions:

1. Configure the WD window. Since it is not possible to send a WD refresh periodically, the user must disable the WD window. From the **FS Config** tab (ACCESS tab on the left panel), go to the **WD Window** box, select **'Disable (INFINITE OPEN WINDOW)'**, and click **Write**.



WDW_RECOVERY 64 ms 64 ms

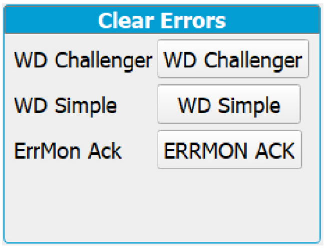
WDM_DC(Duty Cycle) Closed Wir Closed Window : 50 % / Open Window : 50 %

WDM_PERIOD Disable (INFINITE OPEN WINDOW)

Figure 73. Disable WD window

Or execute it from the Script editor: Generator → OpenWD-Window → Run.

2. From the same tab (FS Config), in the **Clear Errors** box, click **WD Challenger** or **WD Simple** (depending on the WD type) one time to send a first good WD refresh and move on the Fail-safe state machine.



Clear Errors

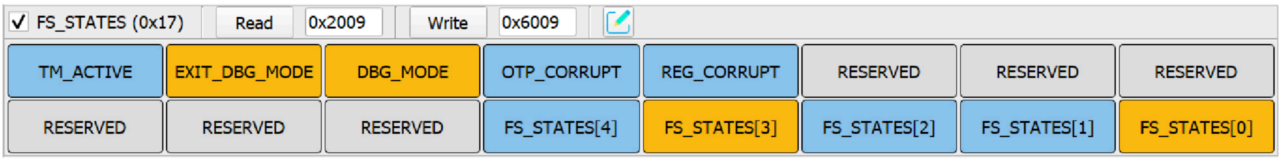
WD Challenger	WD Challenger
WD Simple	WD Simple
ErrMon Ack	ERRMON ACK

aaa-046973

Figure 74. Send a WD refresh

Or execute it from the Script editor: Generator → Simple-WD/Challenger-WD → Run.

3. Send the right number of good WD refreshes in order to clean the Fault Error counter. Example: Default number is '6'. Click six times on the **WD Challenger** or the **WD Simple** button. Verify that the Fault Error counter is now '0' (FLT_ERR_CNT) in the **FS Config** tab.
4. Exit Debug mode. Go to the **Register Map** tab, then in the Safety registers, set the **EXIT_DBG_MODE** to '1' to exit Debug mode.



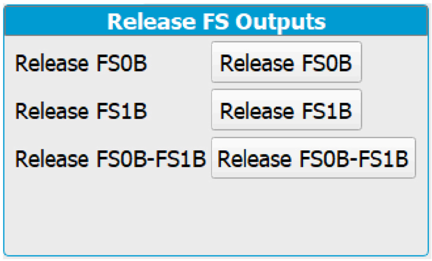
☑ FS_STATES (0x17) | Read | 0x2009 | Write | 0x6009

TM_ACTIVE	EXIT_DBG_MODE	DBG_MODE	OTP_CORRUPT	REG_CORRUPT	RESERVED	RESERVED	RESERVED
RESERVED	RESERVED	RESERVED	FS_STATES[4]	FS_STATES[3]	FS_STATES[2]	FS_STATES[1]	FS_STATES[0]

aaa-046974

Figure 75. Set EXIT_DBG_MODE to '1'

5. In the **Release FS Outputs** box from the **FS Config** tab, send a 'Release FS0B' or a 'Release FS0B-FS1B' command to move to Normal mode.



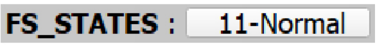
Release FS Outputs

Release FS0B	Release FS0B
Release FS1B	Release FS1B
Release FS0B-FS1B	Release FS0B-FS1B

aaa-046975

Figure 76. Release FS outputs

6. Once these steps are completed, the device should be in Normal mode. To verify the current state, read the FS_STATES status in the **Micro and Device Status** bar, or click it to update.



FS_STATES : 11-Normal

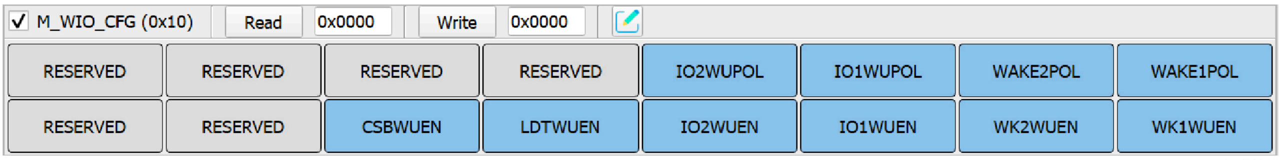
aaa-046976

Figure 77. Read FS_STATES

8.8 Go to Low Power mode

From the INIT_FS or the Normal mode state, the device can go into one of the two Low Power modes: LPOFF mode (all regulators are disabled) or Standby mode (VPRE and selected LDOs remain enabled).

Prior to going into Low Power mode, the user must select a way to wake up the device afterward. Use the ACCESS tab to find the M_WIO_CFG register in the Register map, then set the appropriate bits to '1' to enable the respective wake-up source(s) (IO1/2, WAKE1/2...).



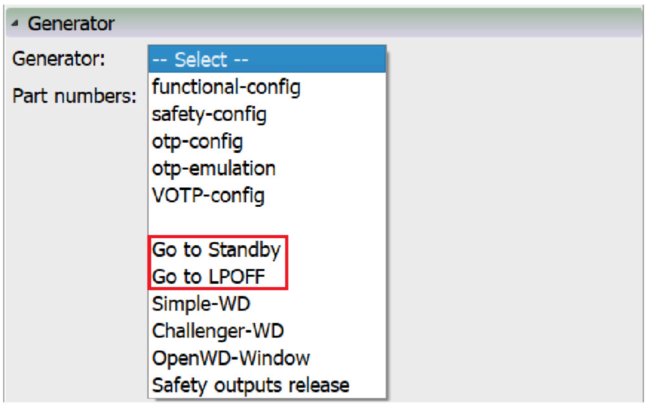
☑ M_WIO_CFG (0x10) Read 0x0000 Write 0x0000

RESERVED	RESERVED	RESERVED	RESERVED	IO2WUPOL	IO1WUPOL	WAKE2POL	WAKE1POL
RESERVED	RESERVED	CSBWUEN	LDTWUEN	IO2WUEN	IO1WUEN	WK2WUEN	WK1WUEN

aaa-046977

Figure 78. M_WIO_CFG register

The user can now either run the preset script 'Go to Standby', from the Generator in the Script editor, to go into Standby mode, or run the preset script 'Go to LPOFF' to go into LPOFF mode.



aaa-046978

Figure 79. Go to STANDBY or LPOFF

9 References

1. **FS2600 data sheet**— product information on FS2600, Safety system basis chip, fit for ASIL D
2. **Programming socket board: UM11504 KITFS26SKTEVM hardware user guide**
   Available on: https://www.nxp.com/KITFS26SKTEVM
3. **Automotive evaluation board: UM11503 KITFS26AEEVM hardware user guide**
   Available on: https://www.nxp.com/KITFS26AEEVM
4. **NXP GUI page**
   Available on: https://www.nxp.com/design/analog-expert-software-and-tools/nxp-gui-for-automotive-pmic-families:PMIC-GUI-SW

Revision history

Rev	Date	Description
v.2	20230322	• Global editing for grammar and style. • Section 3.2.1: Changed " Low Power Standby mode with 25 µA quiescent current with VPRE active" to " Low Power Standby mode with 29 µA quiescent current with VPRE active". • Section 3.2.2: Changed "Output DC current up to 0.8 A or 1.6 A (depending on part number)" to "Output DC current up to 0.8 A or 1.65 A (depending on part number)". • Section 6 – Changed "Attach the DC power supply positive and negative outputs to KITFS26 AEEVM VBAT Phoenix connector (J1), or connect the 12 V power supply toVBAT Jack (J2)." to "Attach the DC power supply positive and negative outputs to KITFS26AEEVM VBAT Phoenix connector (J20), or connect the 12 V power supply toVBAT Jack (J2)." – Table 1: Changed three occurrences of "J1" to "J20". • Updated: Figure 1; Figure 5; Figure 6; Figure 7; Figure 8; Figure 9; Figure 10; Figure 11; Figure 12; Figure 18; Figure 19; Figure 20; Figure 21; Figure 22; Figure 23; Figure 24; Figure 25; Figure 26; Figure 27; Figure 28; Figure 29; Figure 30; Figure 31; Figure 32; Figure 33; Figure 34; Figure 38; Figure 39; Figure 42; Figure 43; Figure 46; Figure 47; Figure 51; Figure 52; Figure 53; Figure 54; Figure 55; Figure 57; Figure 58; Figure 60; Figure 61; Figure 63; Figure 64; Figure 65;
v.1	20220629	Initial version

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