Description

The M66288FP is a high-speed field memory with three FIFO (First In First Out) memories of 262144-word x 8-bit configuration (2M-bit), which uses high-performance silicon gate CMOS process technology. One of three FIFO memories consists of two FIFO memories of 262144-word x 4-bit (1M-bit). Eight types of operation can be performed by mode settings.

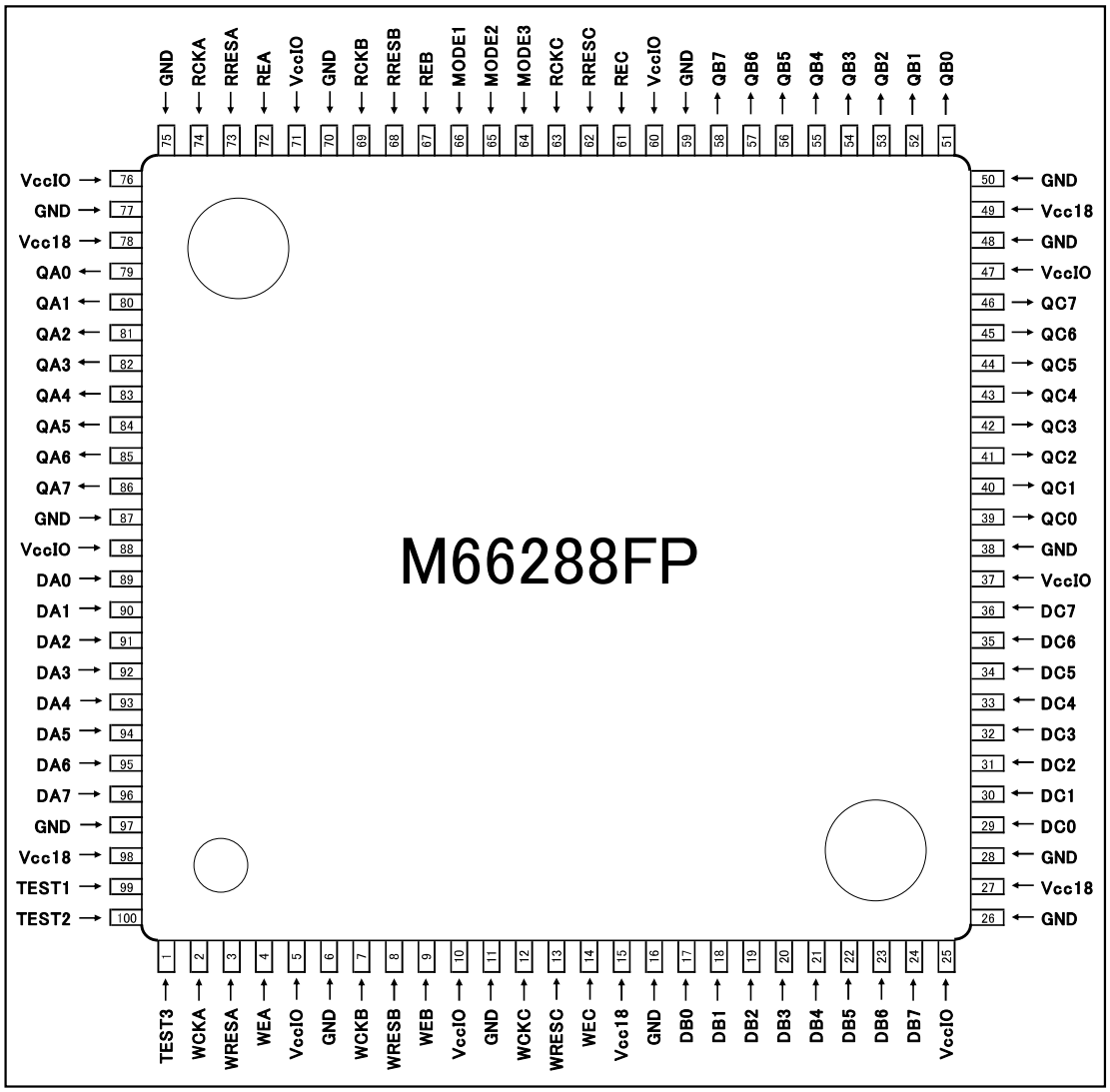
Features

- Memory configuration — Total memory capacity is 6M-bit (static memory). Eight types of memory configurations can be selected.
- High - speed cycle — 12.5 ns (Min.) fmax 80MHz
- High - speed access — 9.0 ns (Max.)
- Output hold — 2.0 ns (Min.)
- Supply voltage — Internal = 1.8 V ± 0.18 V, I/O = 3.3 V ± 0.3 V
- Variable length delay bit
- Eight modes can be selected
- Write and Read function can be operated completely independently and asynchronously
- Output type — 3 state output
- Package — 100pin 14x14mm body LQFP (PLQP0100KB-A, 100P6Q-A)

Application

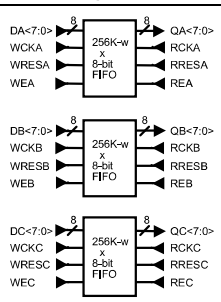
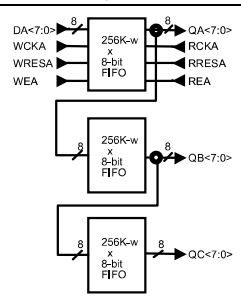
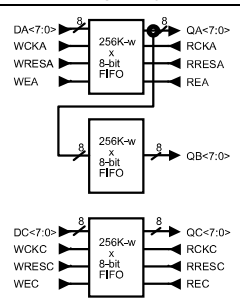
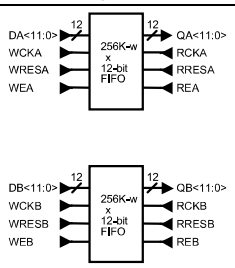
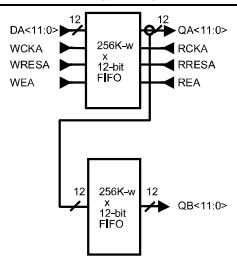
W-CDMA base station, Digital PPC, Digital television, VTR and so on.

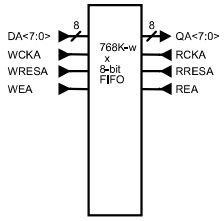
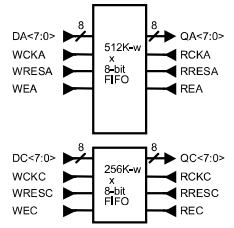
Pin Configuration (Top view)

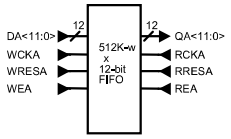


Mode Descriptions Drawing

1K-word = 1024-word

256K-word				
8-bit bus I/F			12-bit bus I/F	
MODE 1	MODE 2	MODE 3	MODE 4	MODE 5
				
The three pieces of 256K-word x 8-bit FIFO can be operated completely independently.	The three pieces of 256K-word x 8-bit FIFO are cascade-connected. (Note 1)	The two pieces of 256K-word x 8-bit FIFO are cascade-connected and, a piece of 256K-word x 8-bit FIFO can be operated completely independently. (Note 1)	The two pieces of 256K-word x 12-bit FIFO can be operated completely independently. (Note 2)	The two pieces of 256K-word x 12-bit FIFO are cascade-connected (Note 1, Note 2)
3-system individual input	1-system input	(1) 1-system input (2) 1-system input	2-system individual input.	1-system input
3-system individual output	The simultaneous output of the 1, 2, 3 line delay data.	(1) The simultaneous output of the 1, 2 line delay data. (2) 1-system output	2-system individual output.	The simultaneous output of the 1, 2 line delay data.

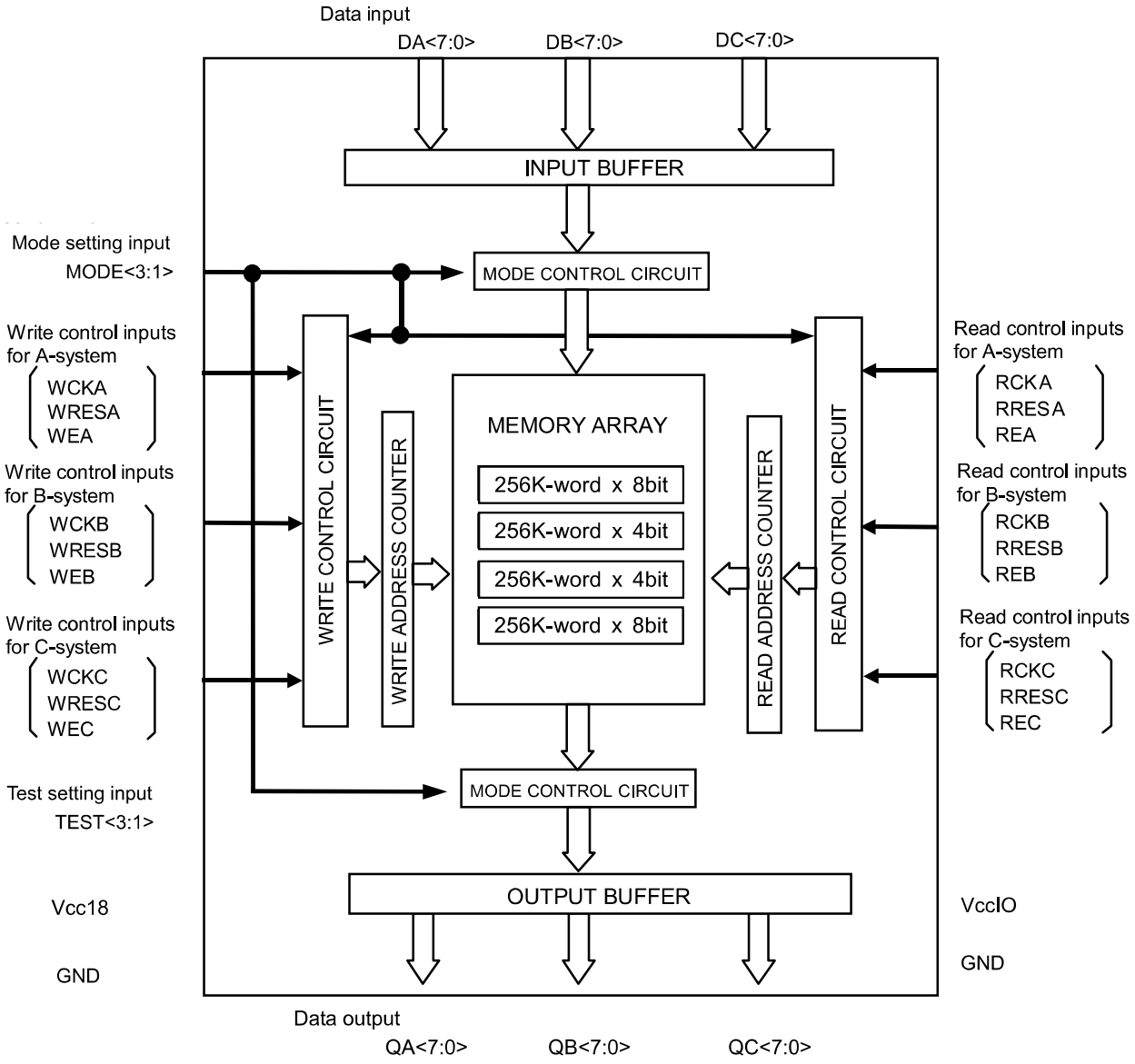
768K-word	512K-word & 256K-word
8-bit bus I/F	
MODE 6	MODE 7
	
A piece of 768K-word x 8-bit FIFO can be operated completely independently.	A piece of 512K-word x 8-bit FIFO and a piece of 256K-word x 8-bit FIFO can be operated completely independently.
1-system input	2-system individual input
1-system output	2-system individual output

512K-word
12-bit bus I/F
MODE 8

A piece of 512K-word x 12-bit FIFO can be operated completely independently. (Note 2)
1-system input
1-system output

Note1: Write and read operation of FIFO after the 2nd line is controlled by the read system pin of the 1st line FIFO. Maximum number of words on this mode is 256K-word. Line delay is achieved without outer connection.

Note2: Please refer to pin assignment tables in “Operation Description” of Mode 4, Mode 5, and Mode 8 for assignment of external pins, Dx<11:0> and Qx<11:0> when used in 12-bit bus interface.

Block Diagram



Pin Function Descriptions

Pin name	Name	Input / Output	Number of pins	Function
WCK x	Write clock input	Input	3	They are write clock inputs.
WE x	Write enable input	Input	3	They are write enable control inputs. When they are "L", a write enable status is provided.
WRES x	Write reset input	Input	3	They are write reset inputs to initialize a write address counter of internal FIFO. When they are "L", a write reset status is provided.
RCK x	Read clock input	Input	3	They are read clock inputs.
RE x	Read enable input	Input	3	They are read enable control inputs. When they are "L", a read enable status is provided.
RRES x	Read reset input	Input	3	They are read reset inputs to initialize a read address counter of internal FIFO. When they are "L", a read reset status is provided.
Dx <7:0>	Data input	Input	24	They are 8-bit input data bus.
Qx <7:0>	Data output	Output	24	They are 8-bit output data bus.
MODE<3:1>	Mode setting input	Input	3	They are operation mode setting inputs. For setting, refer to Mode setting table of Page5.
TEST<3:1>	Test setting input	Input	3	They are test setting inputs. Setting of TEST1 depends on the rising time of the 1.8 V system power supply. For further details, refer to page 12. TEST2 and TEST3 should be fixed at "L".
VccIO	Power supply pin for I/O	-	9	This is a 3.3 V power supply pin for I/O.
Vcc18	Power supply pin for internal circuit	-	5	This is a 1.8 V power supply pin for internal circuit.
GND	Ground pin	-	14	This is a ground pin.

Note: X of the pin name shows A, B and C.

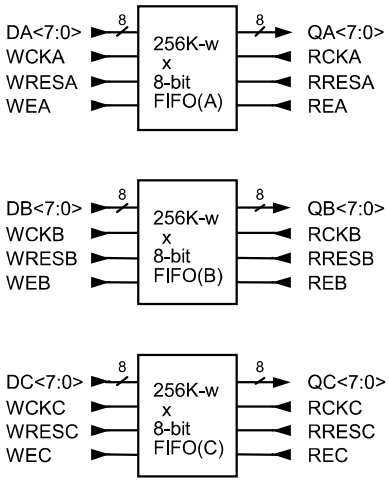
A = A-system, B = B-system, C = C-system.

Mode Setting

MODE<3:1> should be set to “L” or “H” as shown below to select the 8 operation modes.

MODE 3	MODE 2	MODE 1	Operation mode
L	L	L	MODE 1
L	L	H	MODE 2
L	H	L	MODE 3
L	H	H	MODE 4
H	L	L	MODE 5
H	L	H	MODE 6
H	H	L	MODE 7
H	H	H	MODE 8

Mode1 Operation Description



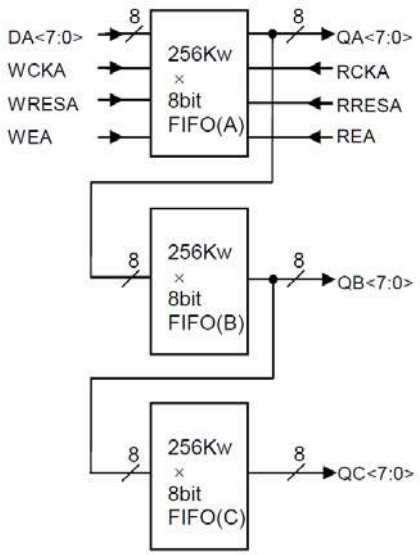
<Mode 1>

In mode 1, three pieces of 256K-word x 8-bit FIFO can be controlled completely independently. Taking FIFO (A) as an example, the operation of FIFO memory is described below. The operation of FIFO (B) and FIFO (C) are the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<7:0> in synchronization with the rising of read clock input RCKA.
At this time, the read address counter of FIFO (A) is incremented.
When REA is "H", this IC disable to read data from FIFO (A) and the read address counter of FIFO (A) is not incremented. Also QA<7:0> become high impedance state.
When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

Mode2 Operation Description



<Mode 2>

In mode 2, three pieces of 256K-word x 8-bit FIFO are cascade-connected and it is possible to generate delay data for 3-lines without external wiring.

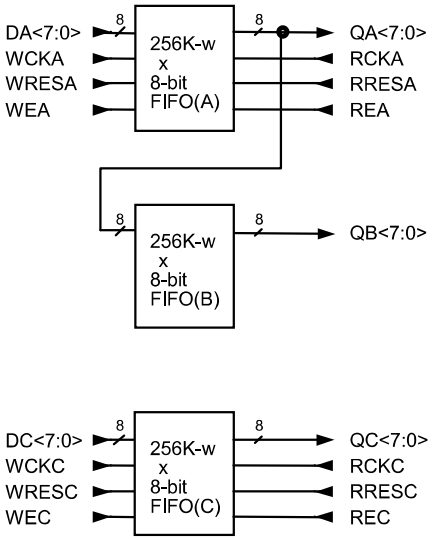
When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented. When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A), FIFO (B) and FIFO (C) are outputted to each QA<7:0>, QB<7:0>, QC<7:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of all FIFOs are incremented.
Also the data of the upper FIFO is written into the lower FIFO in synchronization with the rising of RCKA. At this time, the write address counters of FIFO (B) and FIFO (C) are incremented simultaneously.
When REA is "H", this IC disable to read data from FIFO (A), FIFO (B) and FIFO (C) and the read address counter of each FIFO is not incremented. All data outputs become high impedance state. And this IC also disable to write data into FIFO (B) and FIFO (C) and the write address counter of FIFO (B) and FIFO (C) is not incremented.
When read reset input RRESA is "L", the read address counter of FIFO (A) and the write/read address counters of FIFO (B) and FIFO (C) are initialized.

In mode 2, only all pins for the A-system, QB<7:0> and QC<7:0> are used. Therefore, the write/read control pins for the B/C-system, DB<7:0> and DC<7:0> should be fixed at "L" or "H".

Note: Write and read operation of FIFO (B) and FIFO (C) after the 2nd line is controlled by the read system pin of the 1st line FIFO (A).
Maximum number of words on this mode is 256K-word.

Mode3 Operation Description



<Mode 3>

In mode 3, two pieces of 256K-word x 8-bit FIFO are cascade-connected and the other FIFO is configured completely independently.

This makes it possible to generate delay data for 2-lines without external wiring and to control the other independent one FIFO memory.

When write enable input WEA is "L", the contents of data input DA<7:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.

When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.

When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

When read enable input REA is "L", the contents of FIFO (A) and FIFO (B) are outputted to each QA<7:0> and QB<7:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of FIFO (A) and FIFO (B) are incremented.

Also the data of FIFO (A) is written into FIFO (B) in synchronization with the rising of RCKA. At this time, the write address counter of FIFO (B) is incremented simultaneously.

When REA is "H", this IC disable to read data from FIFO (A) and FIFO (B) and the read address counter of each FIFO is not incremented. QA<7:0> and QB<7:0> become high impedance state. And this IC also disable to write data into FIFO (B) and the write address counter of FIFO (B) is not incremented.

When read reset input RRESA is "L", the read address counter of FIFO (A) and the write/read address counter of FIFO (B) are initialized.

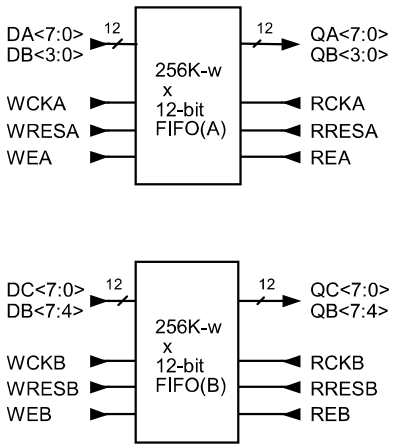
The operation of FIFO (C) is the same as that of mode 1.

In mode 3, only all pins for the A/C-system and QB<7:0> are used. Therefore the write/read control pins for the B-system and DB<7:0> should be fixed at "L" or "H".

Note: Write and read operation of FIFO (B) at the 2nd line is controlled by the read system pin of the 1st line FIFO (A).

Maximum number of words on this mode is 256K-word.

Mode4 Operation Description



<Mode 4>

In mode 4, two pieces of 256K-word x 12-bit FIFO can be controlled completely independently. Taking FIFO (A) as an example, the operation of FIFO memory is described below. The operation of FIFO (B) is the same as that of FIFO (A).

When write enable input WEA is "L", the contents of data input DA<7:0> and DB<3:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented. When WEA is "H", this IC disable to write data into FIFO(A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.

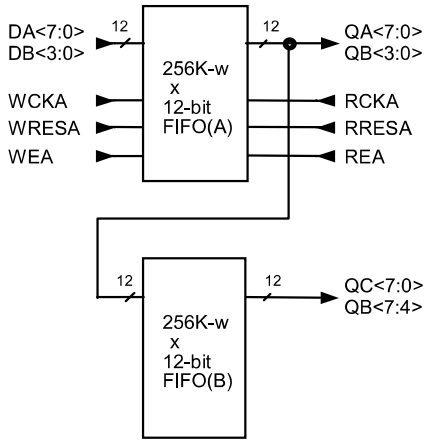
When read enable input REA is "L", the contents of FIFO (A) are outputted to data output QA<7:0> and QB<3:0> in synchronization with the rising of read clock input RCKA. At this time, the read address counter of FIFO (A) is incremented. When REA is "H", this IC disable to read data from FIFO (A) and the read address counter of FIFO (A) is not incremented. Also QA<7:0> and QB<3:0> become high impedance state.
When read reset input RRESA is "L", the read address counter of FIFO (A) is initialized.

Also, set the 12-bit I/O buses of FIFO (A) and FIFO (B) as shown in the table below. In mode 4, only all pins for the A/B-system, DC<7:0> and QC<7:0> are used. Therefore the write/read control pins for the C-system should be fixed at "L" or "H".

External pin name	Data input bus of FIFO (A)	External pin name	Data output bus of FIFO (A)
DA<7>	11^{th}-bit	QA<7>	11^{th}-bit
DA<6>	10^{th}-bit	QA<6>	10^{th}-bit
DA<5>	9^{th}-bit	QA<5>	9^{th}-bit
DA<4>	8^{th}-bit	QA<4>	8^{th}-bit
DA<3>	7^{th}-bit	QA<3>	7^{th}-bit
DA<2>	6^{th}-bit	QA<2>	6^{th}-bit
DA<1>	5^{th}-bit	QA<1>	5^{th}-bit
DA<0>	4^{th}-bit	QA<0>	4^{th}-bit
DB<3>	3^{rd}-bit	QB<3>	3^{rd}-bit
DB<2>	2^{nd}-bit	QB<2>	2^{nd}-bit
DB<1>	1^{st}-bit	QB<1>	1^{st}-bit
DB<0>	0^{th}-bit	QB<0>	0^{th}-bit

External pin name	Data input bus of FIFO (B)	External pin Name	Data output bus of FIFO (B)
DC<7>	11^{th}-bit	QC<7>	11^{th}-bit
DC<6>	10^{th}-bit	QC<6>	10^{th}-bit
DC<5>	9^{th}-bit	QC<5>	9^{th}-bit
DC<4>	8^{th}-bit	QC<4>	8^{th}-bit
DC<3>	7^{th}-bit	QC<3>	7^{th}-bit
DC<2>	6^{th}-bit	QC<2>	6^{th}-bit
DC<1>	5^{th}-bit	QC<1>	5^{th}-bit
DC<0>	4^{th}-bit	QC<0>	4^{th}-bit
DB<7>	3^{rd}-bit	QB<7>	3^{rd}-bit
DB<6>	2^{nd}-bit	QB<6>	2^{nd}-bit
DB<5>	1^{st}-bit	QB<5>	1^{st}-bit
DB<4>	0^{th}-bit	QB<4>	0^{th}-bit

Mode5 Operation Description



<Mode 5>
In mode 5, two pieces of 256K-word x 12-bit FIFO are cascade-connected and it is possible to generate delay data for 2-lines without external wiring.

When write enable input WEA is "L", the contents of data input DA<7:0> and DB<3:0> are written into FIFO (A) in synchronization with the rising of write clock input WCKA. At this time, the write address counter of FIFO (A) is incremented.
When WEA is "H", this IC disable to write data into FIFO (A) and the write address counter of FIFO (A) is not incremented.
When write reset input WRESA is "L", the write address counter of FIFO (A) is initialized.
When read enable input REA is "L", the contents of FIFO (A) and FIFO (B) are outputted to each QA<7:0>, QB<3:0> and QC<7:0>,QB<7:4> in synchronization with the rising of read clock input RCKA. At this time, the read address counters of FIFO (A) and FIFO (B) are incremented.
Also the data of FIFO (A) is written into FIFO (B) in synchronization with the rising of RCKA. At this time, the write address counter of FIFO (B) is incremented simultaneously.
When REA is "H", this IC disable to read data from FIFO (A) and FIFO (B) and the read address counter of each FIFO is not incremented.
Also all data outputs become high impedance state. And this IC also disable to write data into FIFO (B) and the write address counter of FIFO (B) is not incremented.
When read reset input RRESA is "L", the read address counter of FIFO (A) and the write /read address counter of FIFO (B) are initialized.

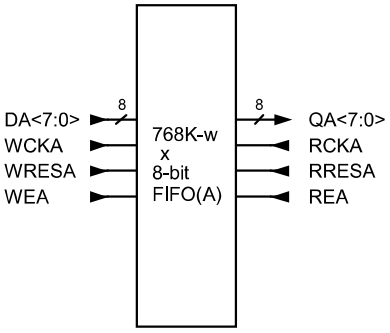
Also, set the 12-bit I/O buses of FIFO (A) and FIFO (B) as shown in the table below. In mode 5, only all pins for the A-system, DB<3:0>, QB<7:0> and QC<7:0> are used. Therefore the write/read control pins for the B/C-system, DB<7:4> and DC<7:0> should be fixed at "L" or "H".

External pin Name	Data input bus of FIFO (A)	External pin name	Data output bus of FIFO (A)
DA<7>	11th-bit	QA<7>	11th-bit
DA<6>	10th-bit	QA<6>	10th-bit
DA<5>	9th-bit	QA<5>	9th-bit
DA<4>	8th-bit	QA<4>	8th-bit
DA<3>	7th-bit	QA<3>	7th-bit
DA<2>	6th-bit	QA<2>	6th-bit
DA<1>	5th-bit	QA<1>	5th-bit
DA<0>	4th-bit	QA<0>	4th-bit
DB<3>	3rd-bit	QB<3>	3rd-bit
DB<2>	2nd-bit	QB<2>	2nd-bit
DB<1>	1st-bit	QB<1>	1st-bit
DB<0>	0th-bit	QB<0>	0th-bit

External pin Name	Data output bus of FIFO (B)
QC<7>	11th-bit
QC<6>	10th-bit
QC<5>	9th-bit
QC<4>	8th-bit
QC<3>	7th-bit
QC<2>	6th-bit
QC<1>	5th-bit
QC<0>	4th-bit
QB<7>	3rd-bit
QB<6>	2nd-bit
QB<5>	1st-bit
QB<4>	0th-bit

Note: Write and read operation of FIFO(B) at the 2nd line is controlled by the read system pin of the 1st line FIFO(A).
Maximum number of words on this mode is 256K-word.

Mode6 Operation Description



<Mode 6>

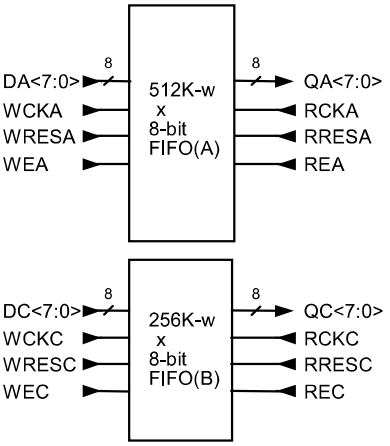
In mode 6, one FIFO memory of the 768K-word x 8-bit composition can be controlled.

The operation of FIFO (A) is the same as that of mode 1.

In mode 6, only all pins for the A-system are used. Therefore, the all input pins for the B/C-system should be fixed at "L" or "H".

Also QB<7:0> and QC<7:0> become high impedance state.

Mode7 Operation Description



<Mode 7>

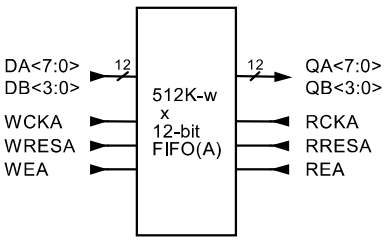
In mode 7, one of 512K-word x 8-bit FIFO and one of 256K-word x 8-bit FIFO memory can be controlled completely independently.

The operation of FIFO (A) and FIFO (B) are the same as that of mode 1.

In mode 7, only all pins for the A/C-system are used. Therefore, the all input pins for the B-system should be fixed at "L" or "H".

Also QB<7:0> become high impedance state.

Mode8 Operation Description



<Mode 8>

In mode 8, one FIFO memory of the 512K-word x 12-bit composition can be controlled.

The operation of FIFO (A) is the same as that of mode 4.

Also, please set the 12-bit I/O buses of FIFO (A) as mentioned in the table of mode 4 FIFO (A).

In mode 8, only all pins for the A-system, DB<3:0> and QB<3:0> are used. Therefore, the write/read control pins for the B/C-system, DB<7:4> and DC<7:0> should be fixed at "L" or "H".

Also QB<7:4> and QC<7:0> become high impedance state.

Electrical Characteristics

Absolute Maximum Ratings (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}18$	Supply voltage (1.8 V power supply)	A value based on GND	-0.3~+2.5	V
$V_{CC}IO$	Supply voltage (3.3 V power supply)		-0.3~+3.8	V
V_I	Input voltage		-0.3~V_{CC}IO+0.3	V
V_O	Output voltage		-0.3~V_{CC}IO+0.3	V
P_d	Maximum power dissipation	Ta = 70 °C	800	mW
T_{stg}	Storage temperature		-55~150	°C

Recommended Operating Conditions

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$V_{CC}18$	Supply voltage for internal circuit (1.8 V power supply)	A value based on GND	1.62	1.8	1.98	V
$V_{CC}IO$	Supply voltage for I/O (3.3 V power supply)		3.0	3.3	3.6	V
T_{opr}	Operating ambient temperature		0		70	°C

DC Characteristics (Ta = 0 ~ 70°C, Vcc18 = 1.8 ± 0.18 V, VccIO = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

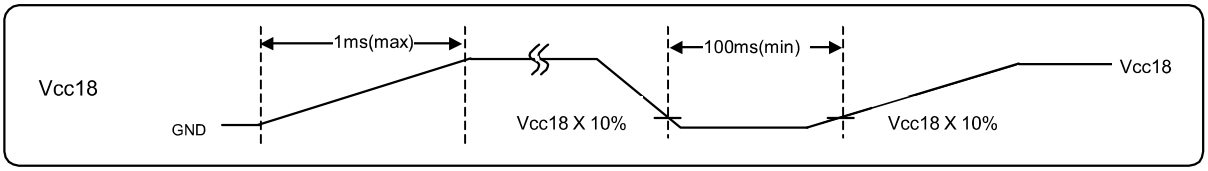
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	A value based on GND	0.8 x VccIO			V
V_{IL}	"L" input voltage				0.2 x VccIO	V
V_{OH}	"H" output voltage	I_{OH} = -4mA	VccIO - 0.4			V
V_{OL}	"L" output voltage	I_{OL} = 4mA			0.4	V
I_{IH}	"H" input current	V_I = V_{CC}IO			10	µA
I_{IL}	"L" input current	V_I = GND			-10	µA
I_{OZH}	Off state "H" output current	V_O = V_{CC}IO			10	µA
I_{OZL}	Off state "L" output current	V_O = GND			-10	µA
$I_{CC}18$	Average operating supply current (1.8 V)	$V_{CC}18$ = 1.8 V ± 0.18 V $V_{CC}IO$ = 3.3 V ± 0.3 V V_I = repeat "H" and "L" V_O= Output open tWCK = tRCK = 12.5 ns			180	mA
$I_{CC}IO$	Average operating supply current (3.3 V)				120	mA
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Off state output capacitance	f = 1 MHz			15	pF

Power - on

After power-on, this IC initializes some circuits of internal FIFO (1.8 V), using the built-in power-on reset circuit.
This power-on reset is performed by using the Vcc18 = 1.8 V system power supply.
Either of the following conditions (1) or (2) should be met according to the power-on time of the Vcc18.

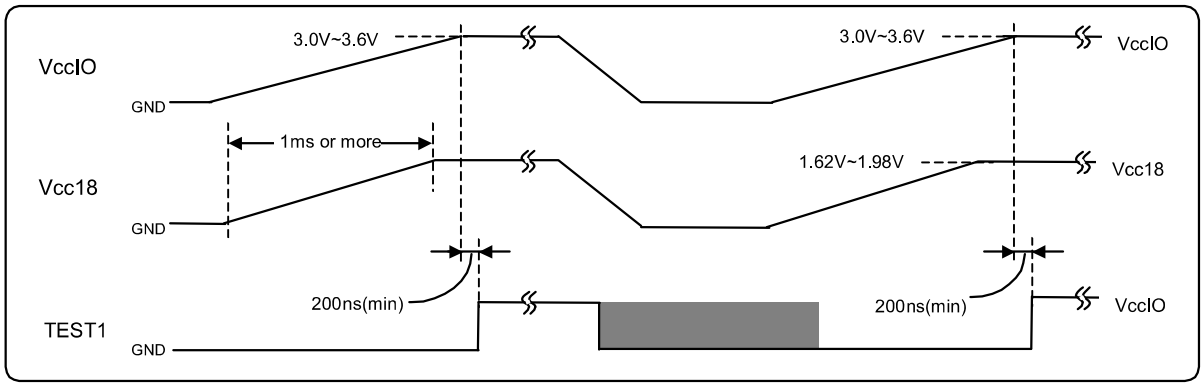
(1) When the power-on time of the Vcc18 is 1 msec or less:

Some circuits of internal FIFO are initialized by the built-in power-on reset circuit. No restriction is imposed on the power-on sequence between Vcc18 and VccIO = 3.3 V system power supply. When powering on again after power-on, provide an interval of 100 ms or more for the Vcc18. At this time, the TEST1 (pin 99) pin should be fixed at "L".



(2) When the power-on time of the Vcc18 is more than 1 msec:

Some circuits of internal FIFO should be initialized by the TEST1 (pin 99) pin.
Input an initialize reset pulse of 200 ns or more after the power supplies (VccIO, Vcc18) reach to the Vcc level.
There is no problem even if reaching to the Vcc level on which power supply.



Note: Some circuits of internal FIFO can be initialized by the TEST1 pin even if the power-on time of the Vcc18 is 1 msec or less.

Note: Important matter;

Provide write reset cycles and read reset cycles of 100 cycles or more, respectively after the Vcc reaches to the specified voltage after power-on.

When inputting a reset pulse using the TEST1 (pin 99) pin, provide write reset cycles and read reset cycles of 100 cycles or more, respectively after inputting a reset pulse at power-on.

There is no problem in this reset operation if a total of 100 cycles or more is achieved, even if discontinuous reset input is made.

Timing Requirements

(Ta = 0 ~ 70°C, Vcc18 = 1.8 ± 0.18 V, VccIO = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

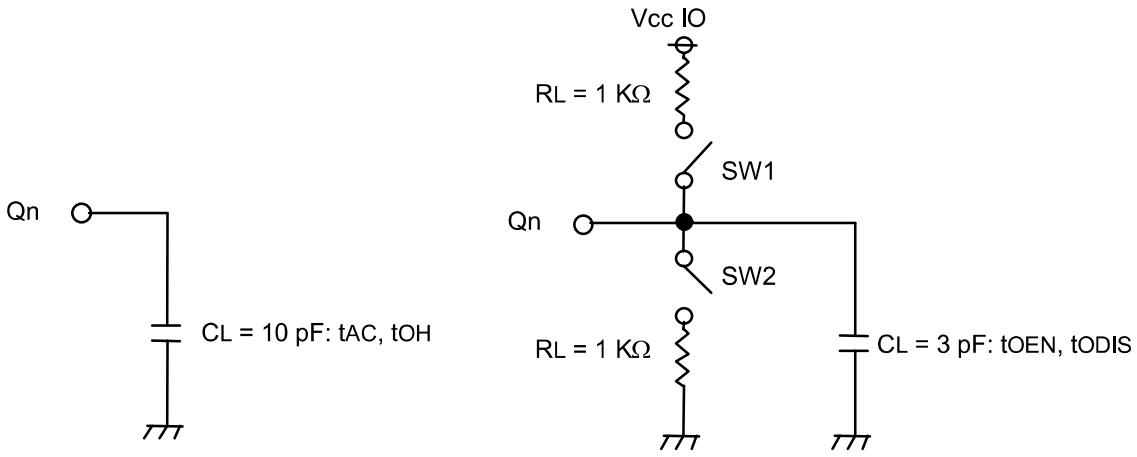
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WCK}	Write clock (WCK) cycle	12.5			ns
t_{WCKH}	Write clock (WCK) "H" pulse width	5			ns
t_{WCKL}	Write clock (WCK) "L" pulse width	5			ns
t_{RCK}	Read clock (RCK) cycle	12.5			ns
t_{RCKH}	Read clock (RCK) "H" pulse width	5			ns
t_{RCKL}	Read clock (RCK) "L" pulse width	5			ns
t_{DS}	Input data setup time to WCK	3.5			ns
t_{DH}	Input data hold time to WCK	1			ns
t_{RESS}	Reset setup time to WCK or RCK	3.5			ns
t_{RESH}	Reset hold time to WCK or RCK	1			ns
t_{NRESS}	Reset non-select setup time to WCK or RCK	3.5			ns
t_{NRESH}	Reset non-select hold time to WCK or RCK	1			ns
t_{WES}	Write enable setup time to WCK	3.5			ns
t_{WEH}	Write enable hold time to WCK	1			ns
t_{NWES}	Write enable non-select setup time to WCK	3.5			ns
t_{NWEH}	Write enable non-select hold time to WCK	1			ns
t_{RES}	Read enable setup time to RCK	3.5			ns
t_{REH}	Read enable hold time to RCK	1			ns
t_{NRES}	Read enable non-select setup time to RCK	3.5			ns
t_{NREH}	Read enable non-select hold time to RCK	1			ns
t_r, t_f	Input pulse rise / fall time			3	ns

Switching Characteristics

(Ta = 0 ~ 70°C, Vcc18 = 1.8 ± 0.18 V, VccIO = 3.3 ± 0.3 V, GND = 0 V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{AC}	Output access time to RCK			9	ns
t_{OH}	Output hold time to RCK	2			ns
t_{OEN}	Output enable time to RCK	2		9	ns
t_{ODIS}	Output disable time to RCK	2		9	ns

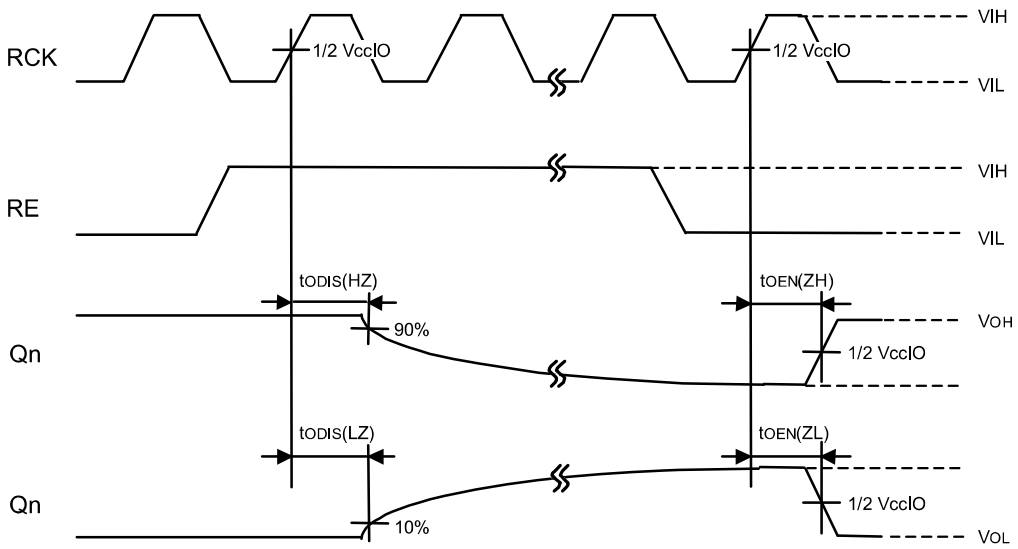
Switching Characteristics Measurement Circuit



Parameter	SW1	SW2
t_{ODIS} (LZ)	Close	Open
t_{ODIS} (HZ)	Open	Close
t_{OEN} (ZL)	Close	Open
t_{OEN} (ZH)	Open	Close

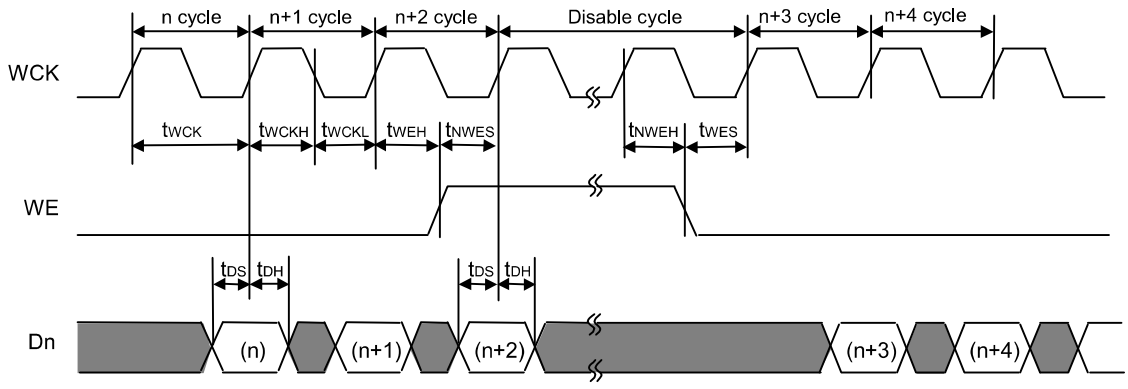
Input pulse level : 0 ~ $V_{CC}IO$
Input pulse rise/fall time : 1 ns
Decision voltage input : 1/2 $V_{CC}IO$
Decision voltage output : 1/2 $V_{CC}IO$ (However, t_{ODIS} (LZ) is 10% of output amplitude and t_{ODIS} (HZ) is 90% of that for decision).
The load capacitance CL includes the floating capacitance of connection and the input capacitance of probe.

t_{ODIS} and t_{OEN} Measurement Condition



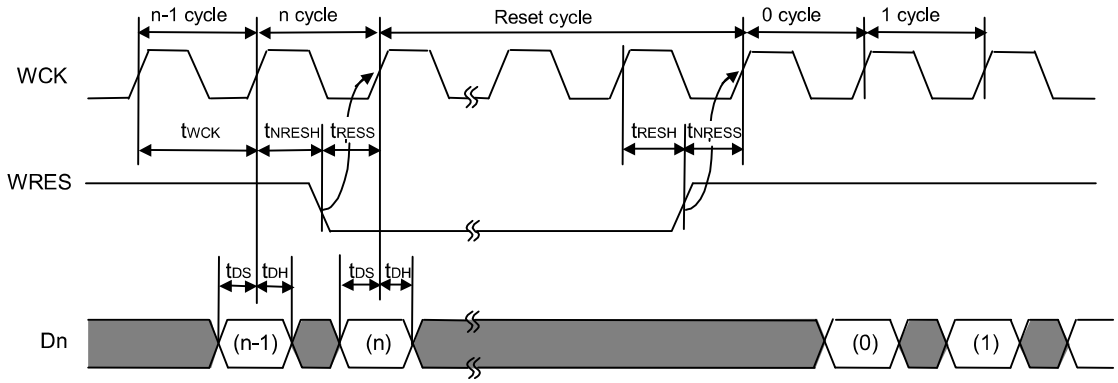
Operating Timing

● Write Cycle



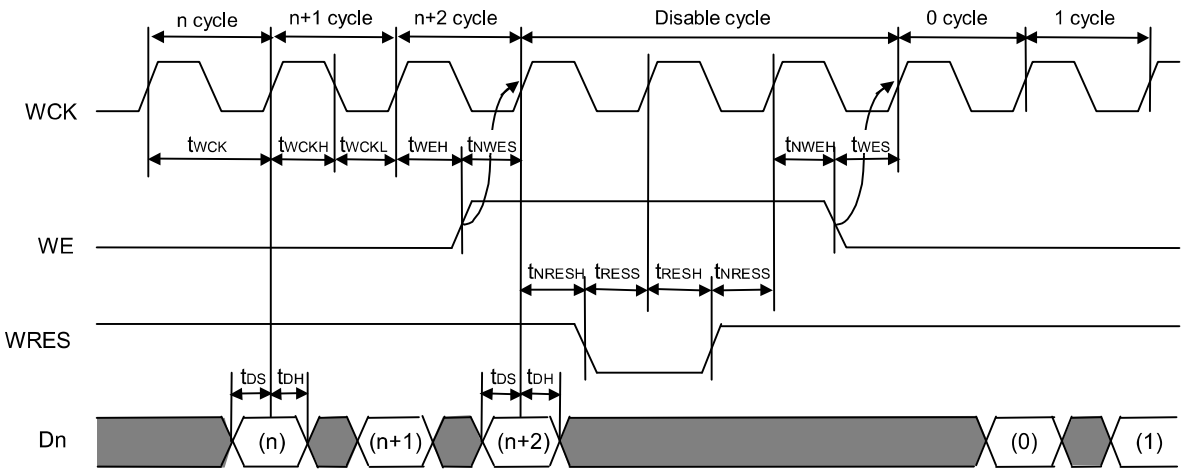
WRES = "H"

● Write Reset Cycle



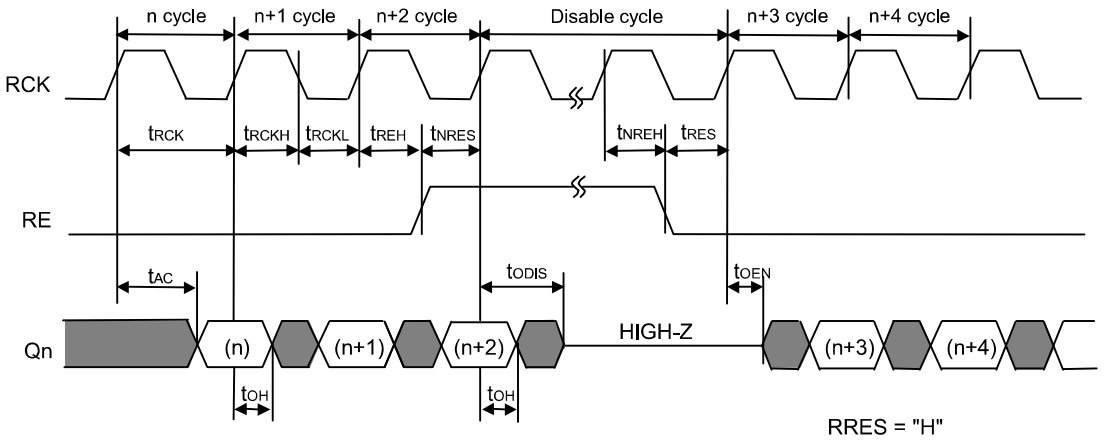
In case of WE = "L"

● Combination Cycle of Write Reset and Write Enable

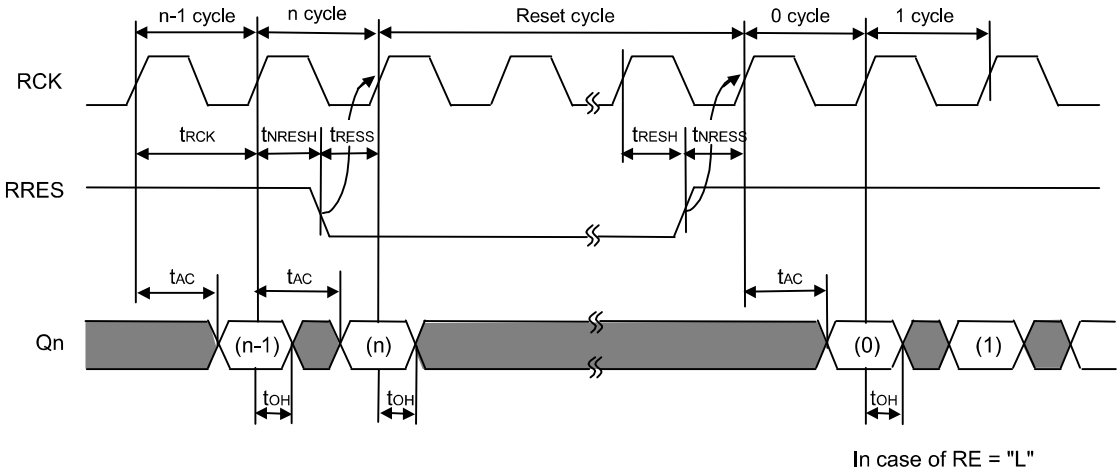


Note: There are no restrictions of WE to WRES.

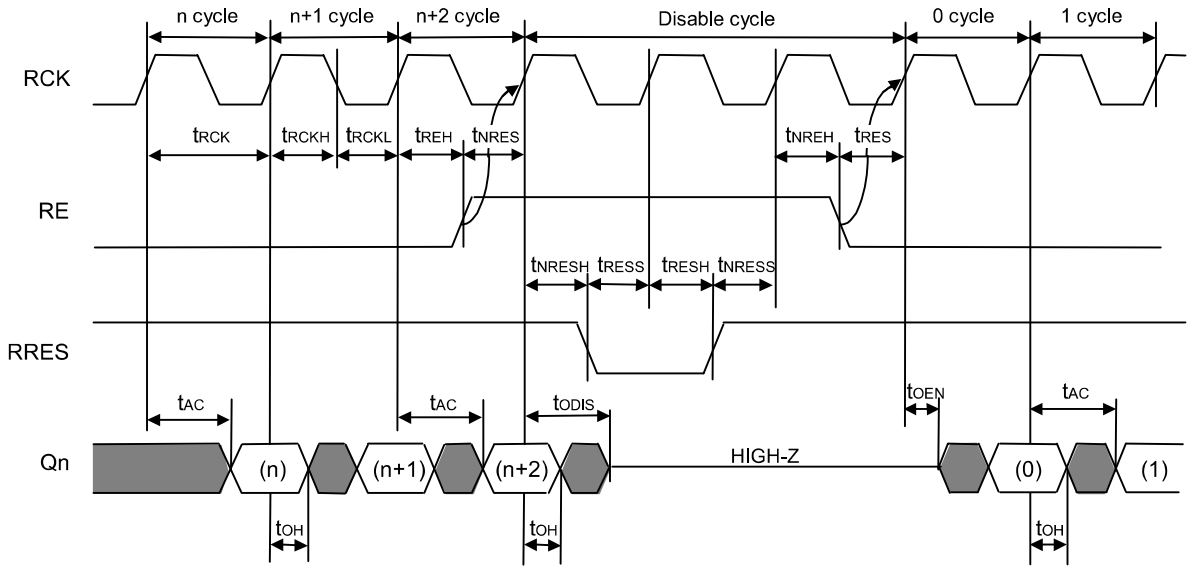
● Read Cycle



● Read Reset Cycle



● Combination Cycle of Read Reset and Read Enable



Note: There are no restrictions of RE to RRES.

Attentions when Write Cycle and Read Cycle Approach Each Other

The interval m of 16 cycles or more between a write cycle and a read cycle should be secured, when the write cycle goes ahead of the read cycle on the following conditions, that is to say the interval less than 15 cycles is forbidden.

WRES, RRES="H"; WE, RE="L", and

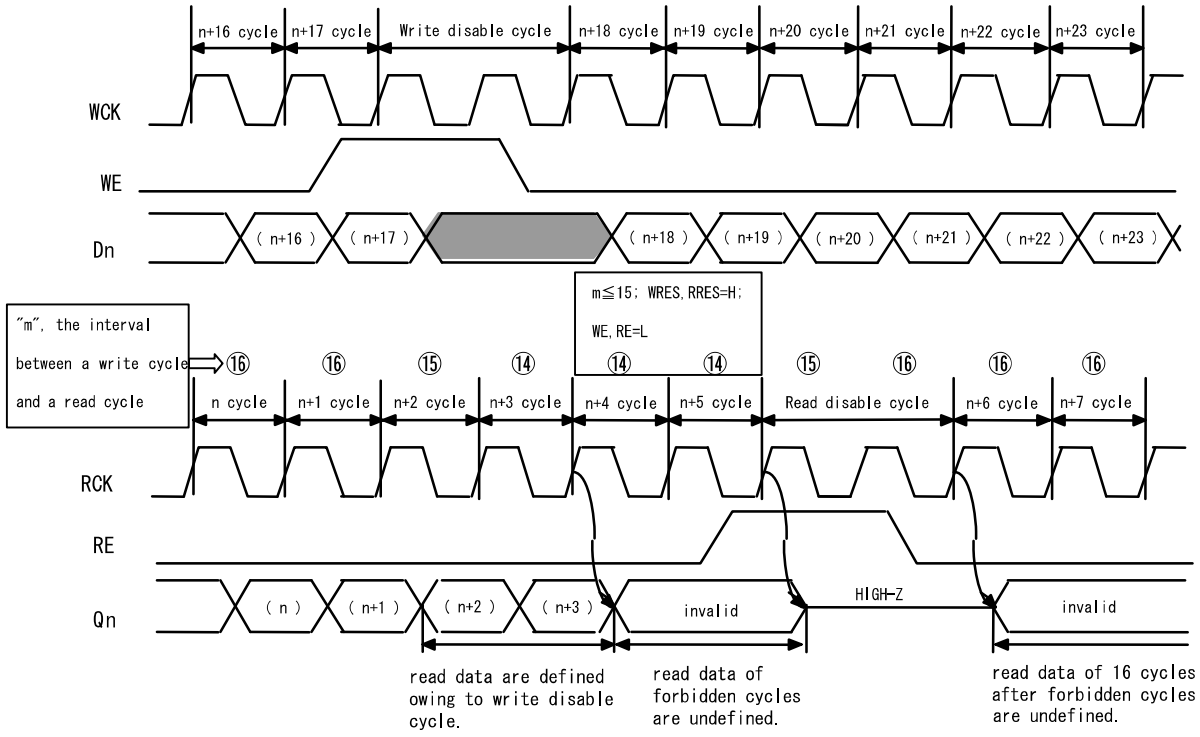
- ●Both write side and read side are activated continuously
- ●Either write side or read side is temporarily stopped owing to the stop of WCK or RCK

When this restriction to the interval is broken on these conditions, writing data is guaranteed, but reading data isn't guaranteed not only during breaking it but also during the following 16 cycles after it is applied. In this 16 cycles, read disable and read reset cycles are not counted.

But the following condition is an exception to restrict to forbid the intervals less than 15 cycles.

- ●Either write side or read side is temporarily stopped owing to reset cycles (WRES or RRES="L") or disable cycles (WE or RE ="H")

Note: Also, when the address counter is incremented up to the last cycle of 1-line and then returned to 0 cycle, the interval m of 16 cycles or more between a write and read cycles should be secured, taking account that they are cyclic and serial lines.



The conditions that the read cycle goes ahead of the write cycle or that write cycle and read cycle are accordant, are exceptions to the restriction to forbid the intervals less than 15cycles.

Variable Length Delay Bits

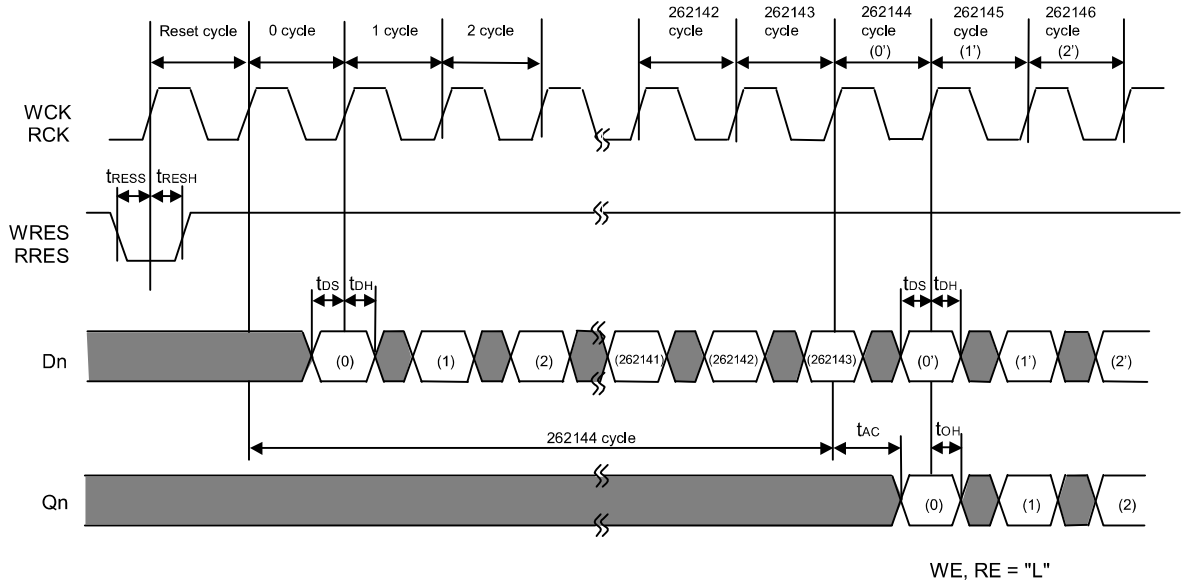
The 1-line length (cycle number) of each mode is shown in the table.

Operation MODE	1-line length
MODE 1 - MODE 5	262144-cycle
MODE 6	786432-cycle
MODE 7	524288-cycle (A-system), 262144-cycle (C-system)
MODE 8	524288-cycle

The following, the case of the MODE 1 - MODE 5 (1-line length = 262144-cycle) is explained to an example.

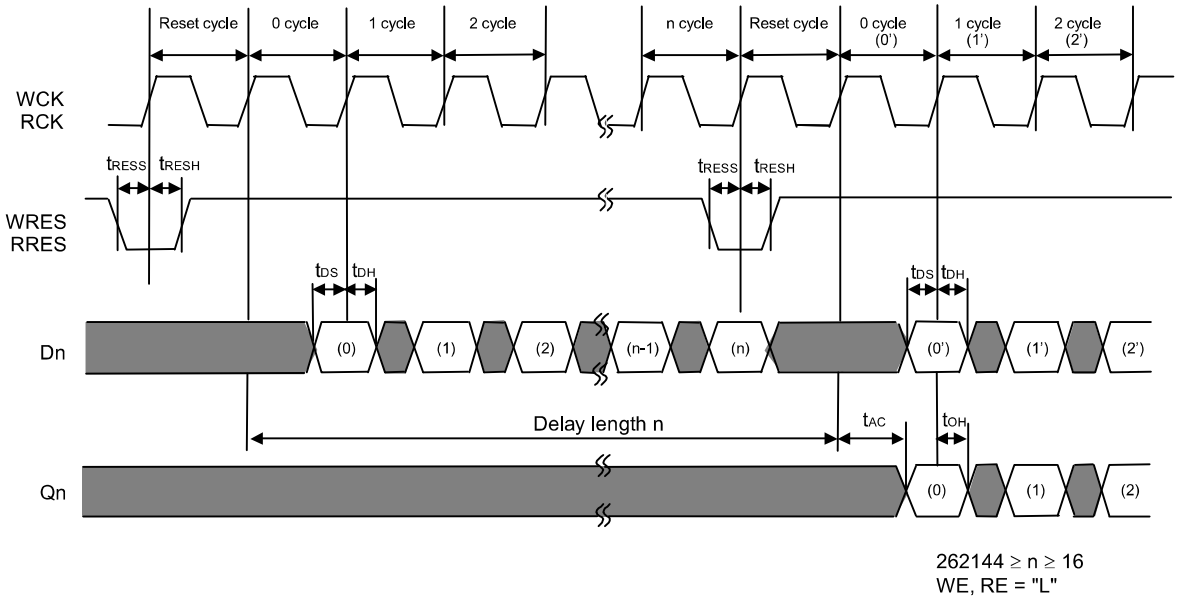
1-line (262144-bit) Delay

In read cycles, an output data is read at the (first) rising edge of RCK (i.e. the start of the cycle) . In write cycles, an input data is written at the (second) rising edge of WCK (i.e. the end of the cycle) . So 1-line delay can be made easily according to the control method of the following figure.



N-bit Delay 1

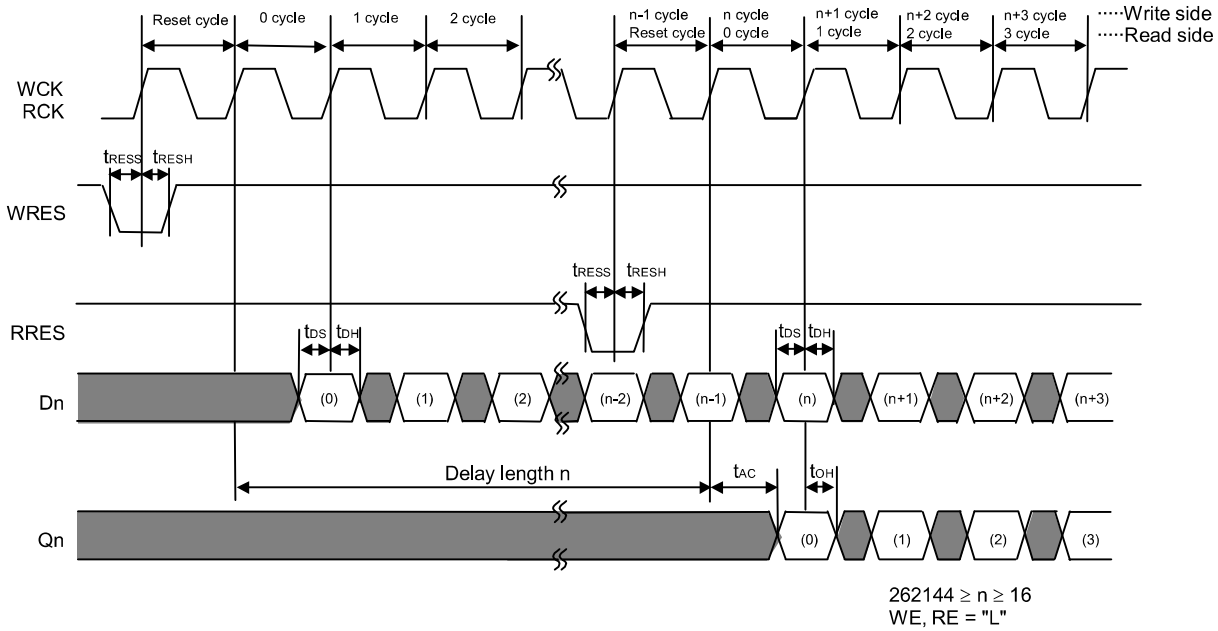
(Reset at a cycle corresponding to delay length)



Note: The interval of 16 cycles or more between a write cycle and a read cycle should be secured to read data written in a certain cycle.

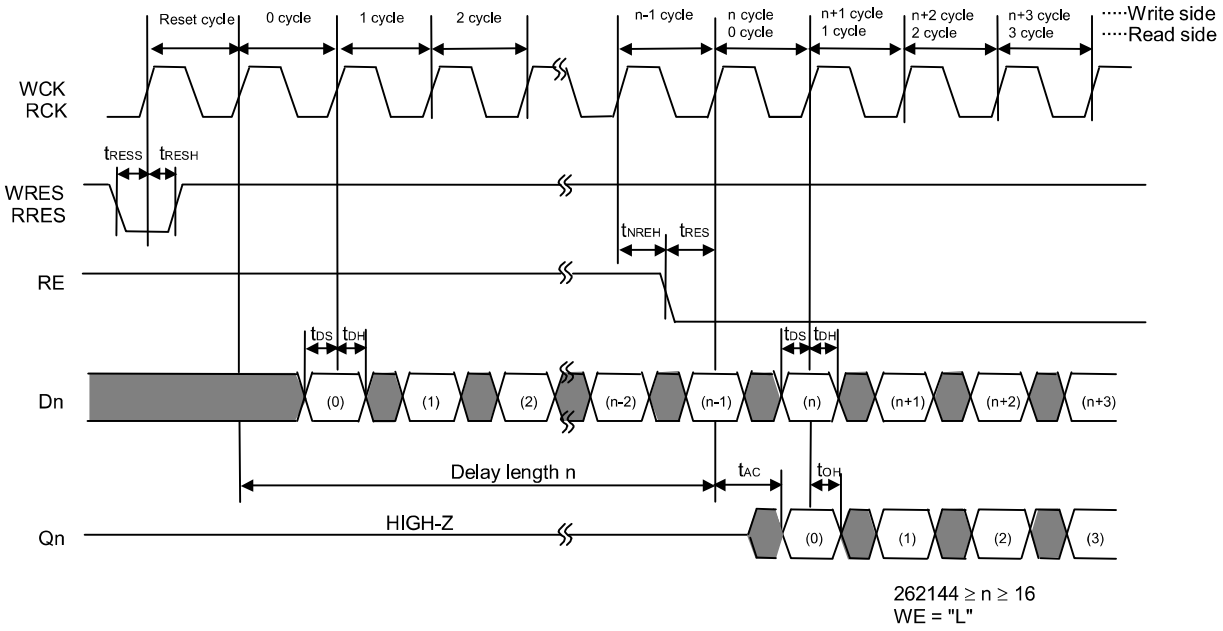
N-bit Delay 2

(Sliding timings of WRES and RRES at a cycle corresponding to delay length)



N-bit Delay 3

(Sliding address by disabling RE at a cycle corresponding to delay length)

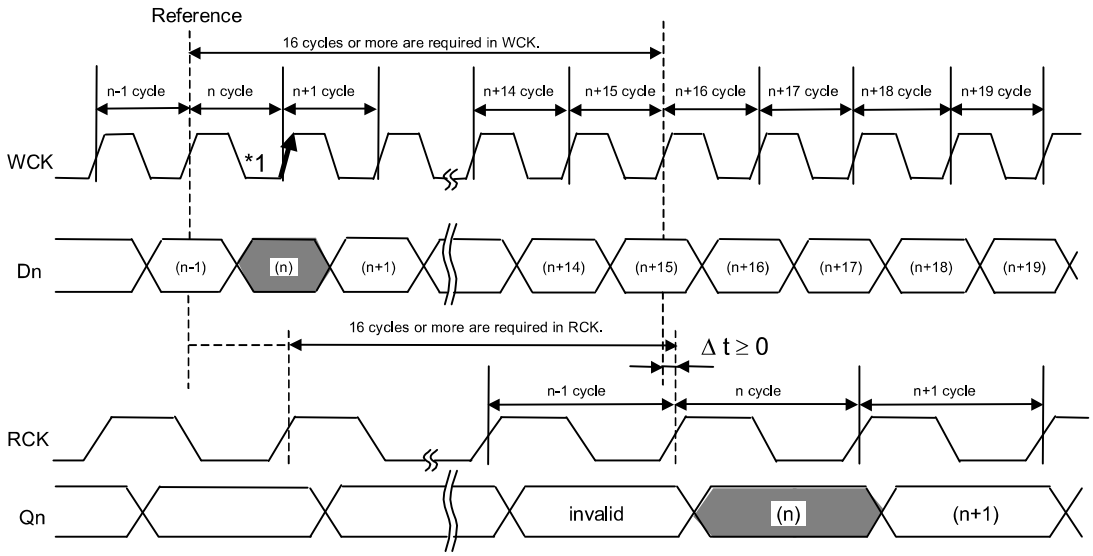


Shortest Reading of Written Data in N Cycle when Write and Read Operated Asynchronously

The interval of 16 cycles or more between a write cycle and a read cycle should be secured and WCK and RCK should be inputted for 16 cycles or more based on beginning of write n cycle at any timing to read written data (data fetched at the rising edge of WCK shown *1 in the following figure) with n cycles on write side.

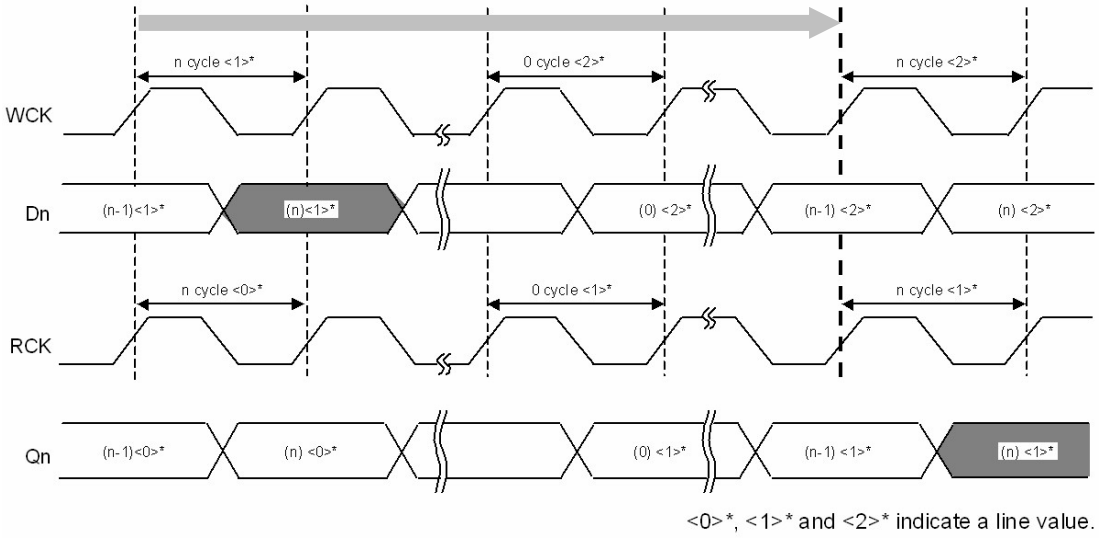
On read side, n cycles should be started after the completion of n+15 cycles on write side ($\Delta t \geq 0$ in the following figure).

Output data becomes undefined when these restrictions are not filled.



Longest Reading of Written Data in N Cycle: 1-line Delay

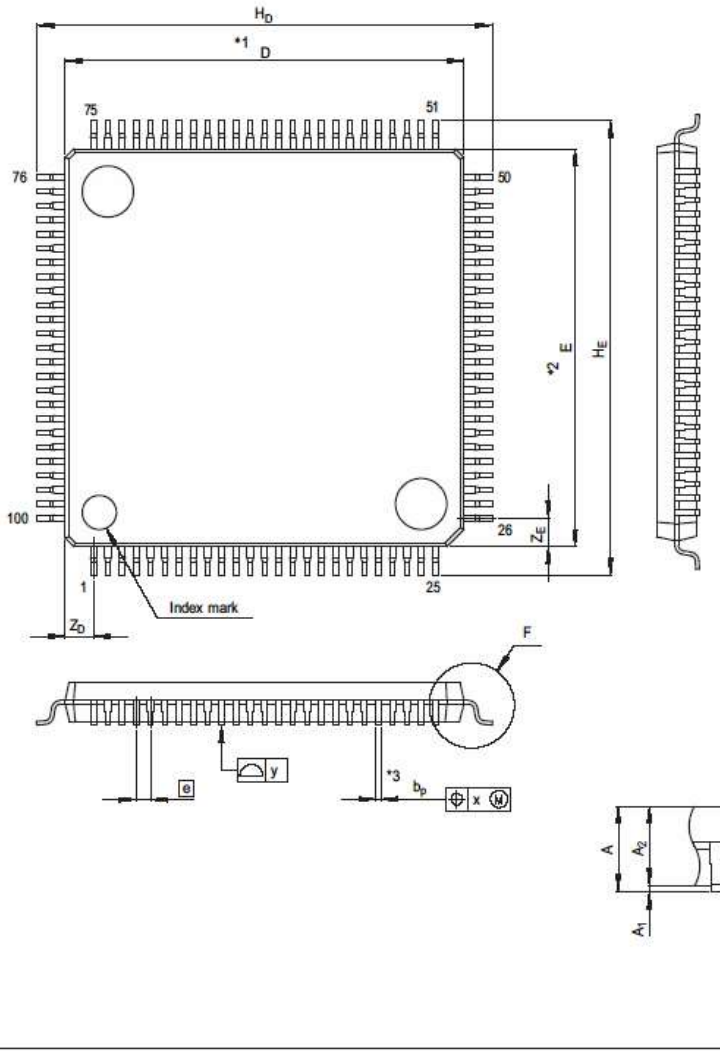
Data output Qn of n cycle <1>* can be read immediately before until the start of n cycle <1>* on read side and the start of n cycle <2>* on write side over lap each other.



<0>*, <1>* and <2>* indicate a line value.

PACKAGE OUTLINE

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

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Colophon .7.2