

AM2903A

Four-Bit Bipolar Microprocessor Slice

The AM2903A is a four-bit expandable bipolar microprocessor slice. The AM2903A performs all functions performed by the industry standard AM2901 and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the AM2903A. In addition to its complete arithmetic and logic instruction set, the AM2903A provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The AM2903A is identical to the AM2903 but up to 30% faster.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am2903A

- **Expandable Register File –**

- **Built-in Normalization Logic –**

- **Built-in Multiplication and Division Logic –**

- **Built-in Division Logic -**
Executes non-restoring, multiple-length division with correction of the quotient.

provided by the Am2903A. In addition to its complete arithmetic and logic instruction set, the Am2903A provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903A is identical to the Am2903 but up to 30% faster.

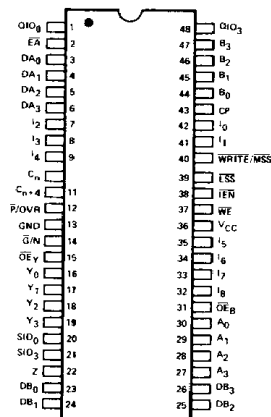
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RELATED PRODUCTS

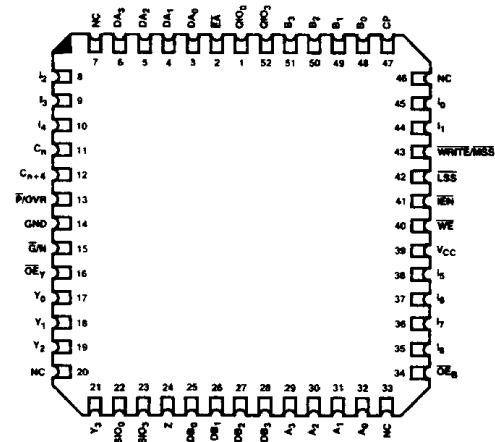
Part No.	Description
Am2902A	Carry Look-Ahead Generator
Am2904	Status and Shift Control Unit
Am2910A	Microprogram Controller
Am2914	Vectored Priority Interrupt Controller
Am2918	Pipeline Register
Am2920	Octal Register
Am2922	Condition Code MUX
Am2925	System Clock Generator
Am2940	DMA Address Generator
Am2952	Bidirectional I/O Port
Am29705A	Two-Port RAM
Am27S35	Registered PROM

CONNECTION DIAGRAMS*

Top View



CD004292

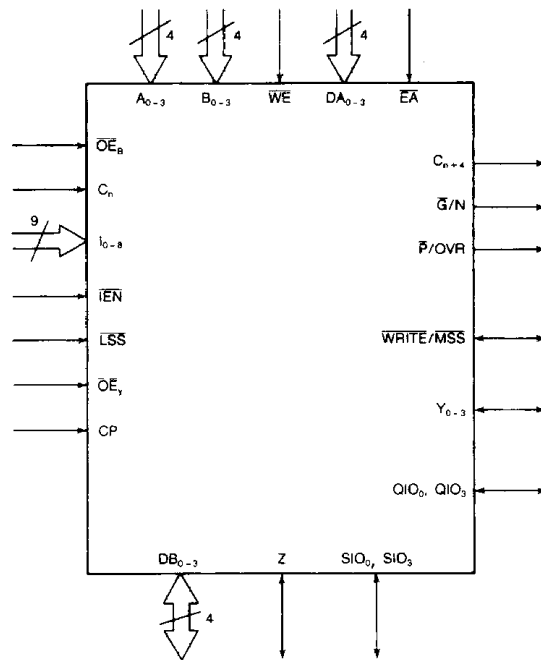


CD004282

Note: Pin 1 is marked for orientation.

*This device is also available in a 48-Pin Flatpack (CFT048).
Pinouts are the same as the DIP.

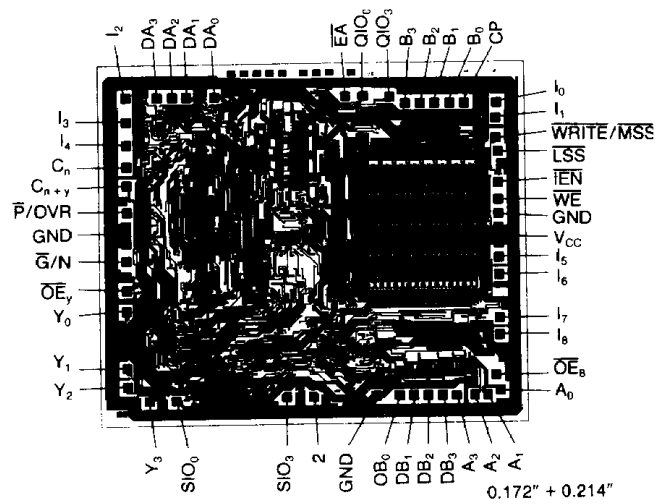
LOGIC SYMBOL



LS002280

V_{CC} = Power Supply
GND = Ground

METALLIZATION AND PAD LAYOUT



DIE SIZE 0.172" x 0.218"

ORDERING INFORMATION

APL and CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) is formed by a combination of:

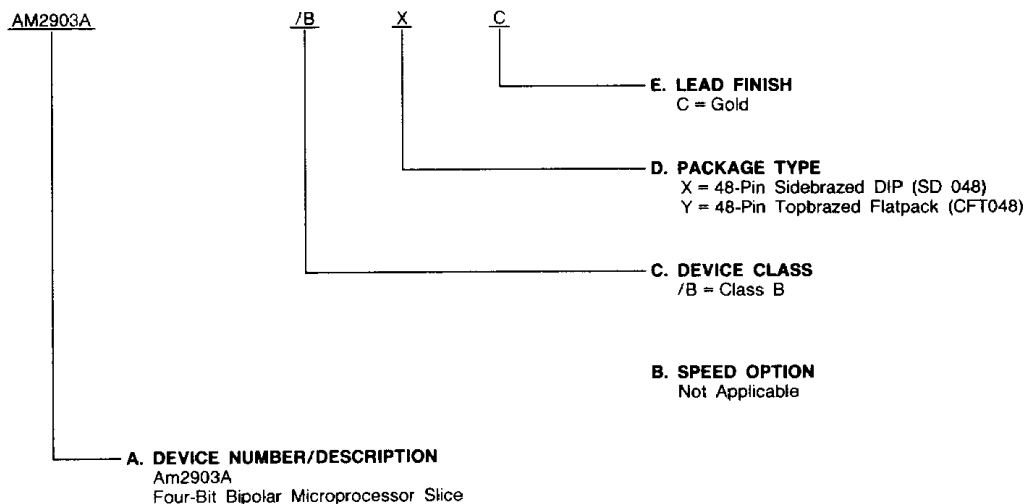
APL Products: A. Device Number

- B. Speed Option (if applicable)
- C. Device Class
- D. Package Type
- E. Lead Finish

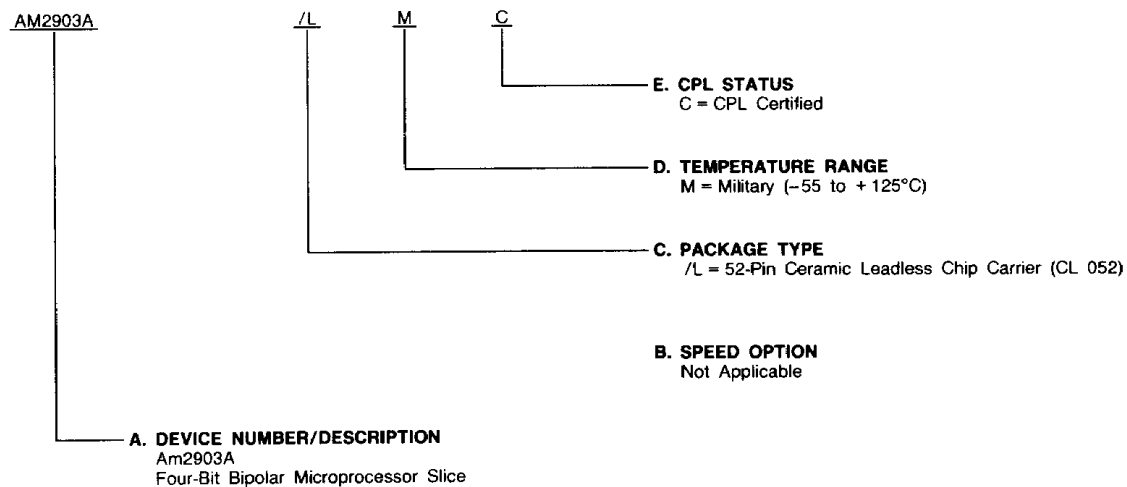
CPL Products: A. Device Number

- B. Speed Option (if applicable)
- C. Package Type
- D. Temperature Range
- E. CPL Status

APL Products



CPL Products



Valid Combinations

Valid Combinations		
APL	AM2903A	/BXC, /BYC
CPL	AM2903A	/LMC

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

A₀₋₃ RAM A Address Inputs (TTL Input)

Four RAM address inputs that contain the address of the RAM word appearing at the RAM A output port.

B₀₋₃ RAM B Address Inputs (TTL Input)

Four RAM address inputs that contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the \overline{WE} input and the CP input are LOW.

\overline{WE} Write Enable Input (TTL Input)

The RAM write enable input. If \overline{WE} is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When \overline{WE} is HIGH, writing data into the RAM is inhibited.

DA₀₋₃ External Data Inputs (TTL Input)

A four-bit external data input that can be selected as one of the Am2903A ALU operand sources; DA₀ is the least significant bit.

\overline{EA} Control Input (TTL Input)

A control input that, when HIGH, selects DA₀₋₃ as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand.

DB₀₋₃ External Data Inputs/Outputs (Three-State Input/Output)

A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ Control Input (TTL Input)

A control input that, when LOW, enables RAM output B onto the DB₀₋₃ lines and, when HIGH, disables the RAM output B three-state buffers.

C_n Carry-In Input (TTL Input)

The carry-in input to the Am2903A ALU.

I₀₋₈ Instruction Inputs (TTL Input)

The nine instruction inputs used to select the Am2903A operation to be performed.

\overline{IEN} Instruction Enable Input (TTL Input)

The instruction enable input that, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When \overline{IEN} is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the Am2903A, \overline{IEN} also controls \overline{WRITE} .

C_{n+4} Carry-Out Output (TTL Output)

This output generally indicates the carry-out of the Am2903A ALU. Refer to Table 5 for an exact definition of this pin.

\overline{G}/N Carry-Generate Output (TTL Output)

A multi-purpose pin that indicates the carry generate, \overline{G} , function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

\overline{P}/OVR Carry-Propagate Output (TTL Output)

A multi-purpose pin that indicates the carry propagate, \overline{P} , function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z Open-Collector I/O Pin (Open-Collector Input/Output)

An open-collector input/output pin that, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO₀, SIO₃ Bidirectional Serial Shift I/Os for the ALU (Three-State Input/Output)

Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO₀ is an input and SIO₃ an output. During a shift-down operation, SIO₃ is an input and SIO₀ is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO₀, QIO₃ Bidirectional Serial Shift I/Os for the Q Shifter (Three-State Input/Output)

Bidirectional serial shift inputs/outputs for the Q shifter that operate like SIO₀ and SIO₃. Refer to Tables 3 and 4 for an exact definition of these pins.

\overline{LSS} Control Input (TTL Input)

An input pin that, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903A array and enables the \overline{WRITE} output onto the \overline{WRITE}/MSS pin. When \overline{LSS} is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the \overline{WRITE} output buffer is disabled.

\overline{WRITE}/MSS Control Input (Three-State Input/Output)

When \overline{LSS} is tied LOW, the \overline{WRITE} output signal appears at this pin; the \overline{WRITE} signal is LOW when an instruction that writes data into the RAM is being executed. When \overline{LSS} is tied HIGH, \overline{WRITE}/MSS is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y₀₋₃ Data Inputs/Outputs (Three-State Input/Output)

Four data inputs/outputs of the Am2903A. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ Control Input (TTL Input)

A control input that, when LOW, enables the ALU shifter output data onto the Y₀₋₃ lines and, when HIGH, disables the Y₀₋₃ three-state output buffers.

CP Clock Input (TTL Input)

The clock input to the Am2903A. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by \overline{WE} , data is written in the RAM when CP is LOW.

FUNCTIONAL DESCRIPTION

Architecture of the Am2903A

The Am2903A is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903A allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function and destination. The Am2903A is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced IMOXTM processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE_B}$ three-state output enable, RAM data can be read directly at the Am2903A DB (I/O) port.

External data at the Am2903A Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, \overline{WE} , is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903A high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The \overline{EA} input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE_B}$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903A ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table 1 shows all possible pairs of ALU source operands as a function of the \overline{EA} , $\overline{OE_B}$, and I_0 inputs.

When instruction bits I_4 , I_3 , I_2 , I_1 , and I_0 are LOW, the Am2903A executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903A executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4 , I_3 , I_2 , and I_1 . Table 2 defines the ALU operation as a function of these four instruction bits.

TABLE 1. ALU OPERAND SOURCES

\overline{EA}	I_0	$\overline{OE_B}$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB ₀₋₃
L	H	X	RAM Output A	Q Register
H	L	L	DA ₀₋₃	RAM Output B
H	L	H	DA ₀₋₃	DB ₀₋₃
H	H	X	DA ₀₋₃	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. Am2903A ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU FUNCTIONS
L	L	L	L	0	$I_0 = L$ Special Functions $I_0 = H$ $F_i = \text{HIGH}$
L	L	L	H	1	$F = S \text{ Minus } R \text{ Minus } 1 \text{ plus } C_n$
L	L	H	L	2	$F = R \text{ Minus } S \text{ Minus } 1 \text{ Plus } C_n$
L	L	H	H	3	$F = R \text{ Plus } S \text{ Plus } C_n$
L	H	L	L	4	$F = S \text{ Plus } C_n$
L	H	L	H	5	$F = \overline{S} \text{ Plus } C_n$
L	H	H	L	6	$F = R \text{ Plus } C_n$
L	H	H	H	7	$F = \overline{R} \text{ Plus } C_n$
H	L	L	L	8	$F_i = \text{LOW}$
H	L	L	H	9	$F_i = \overline{R_i} \text{ AND } S_i$
H	L	H	L	A	$F_i = R_i \text{ EXCLUSIVE NOR } S_i$
H	L	H	H	B	$F_i = R_i \text{ EXCLUSIVE OR } S_i$
H	H	L	L	C	$F_i = R_i \text{ AND } S_i$
H	H	L	H	D	$F_i = R_i \text{ NOR } S_i$
H	H	H	L	E	$F_i = R_i \text{ NAND } S_i$
H	H	H	H	F	$F_i = R_i \text{ OR } S_i$

L = LOW H = HIGH i = 0 to 3

Am2903As may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903As are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, G, and carry propagate, P, signals required for a lookahead carry scheme are generated by the Am2903A and are available as outputs of the least significant and intermediate slices.

The Am2903A also generates a carry-out signal, C_{n+4} , which is generally available as an output of each slice. Both the carry-in, C_n , and carry-out, C_{n+4} , signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N

and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose \bar{G}/N and \bar{P}/OVR outputs indicate \bar{G} and \bar{P} at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4} , \bar{P}/OVR , and \bar{G}/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903A instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure 1). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0 , Y_1 , Y_2 , Y_3 and propagated to the SIO_3 output.

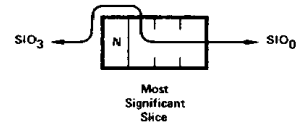
A cascable, five-bit parity generator/checker is designed into the Am2903A ALU shifter and provides ALU error detection capability. Parity for the F_0 , F_1 , F_2 , F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903A executes instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8 , I_7 , I_6 , I_5 . Table 3 defines the ALU shifter operation as a function of these four bits.

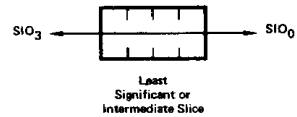
Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and

QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

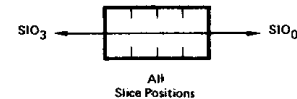


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DF000410

Figure 1-1.
Am2903A Arithmetic Shift Path



DF000420

Figure 1-2.
Am2903A Logical Shift Path

Double-length arithmetic and logical shifting capability is provided by the Am2903A. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903A special functions and the operations which the Q Register and shifter perform for each. When the Am2903A executes instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits I_8 , I_7 , I_6 , I_5 . Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the \overline{OE}_Y input is LOW and are in the high impedance state when \overline{OE}_Y is HIGH. The DB output buffers are enabled when the \overline{OE}_B input is LOW.

TABLE 3. ALU DESTINATION CONTROL FOR I₀ OR I₁ OR I₂ OR I₃ = HIGH, $\overline{\text{IEN}}$ = LOW.

I ₈	I ₇	I ₆	I ₅	Hex Code	ALU Shifter Function	SIO ₃		Y ₃		Y ₂		Y ₁	Y ₀	SIO ₀	$\overline{\text{Write}}$	Q Reg & Shifter Function	QIO ₃	QIO ₀
						Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Other Slices							
L	L	L	L	0	Arith. F/2→Y	Input	Input	F ₃	SIO ₃	SIO ₃	F ₃	F ₂	F ₁	F ₀	L	Hold	Z	Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO ₃	SIO ₃	F ₃	F ₃	F ₂	F ₁	F ₀	L	Hold	Z	Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F ₃	SIO ₃	SIO ₃	F ₃	F ₂	F ₁	F ₀	L	Log. Q/2→Q	Input	Q ₀
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO ₃	SIO ₃	F ₃	F ₃	F ₂	F ₁	F ₀	L	Log. Q/2→Q	Input	Q ₀
L	H	L	L	4	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	L	Hold	Z	Z
L	H	L	H	5	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	H	Log. Q/2→Q	Input	Q ₀
L	H	H	L	6	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	H	F→Q	Z	Z
L	H	H	H	7	F→Y	Input	Input	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Parity	L	F→Q	Z	Z
H	L	L	L	8	Arith. 2F→Y	F ₂	F ₃	F ₃	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Hold	Z	Z
H	L	L	H	9	Log. 2F→Y	F ₃	F ₃	F ₂	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Hold	Z	Z
H	L	H	L	A	Arith. 2F→Y	F ₂	F ₃	F ₃	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Log. 2Q→Q	Q ₃	Input
H	L	H	H	B	Log. 2F→Y	F ₃	F ₃	F ₂	F ₂	F ₁	F ₁	F ₀	SIO ₀	Input	L	Log. 2Q→Q	Q ₃	Input
H	H	L	L	C	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Z	H	Hold	Z	Z
H	H	L	H	D	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Z	H	Log. 2Q→Q	Q ₃	Input
H	H	H	L	E	SIO ₀ →Y ₀ , Y ₁ , Y ₂ , Y ₃	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	SIO ₀	Input	L	Hold	Z	Z
H	H	H	H	F	F→Y	F ₃	F ₃	F ₃	F ₃	F ₂	F ₂	F ₁	F ₀	Z	L	Hold	Z	Z

Parity = F₃ ∇ F₂ ∇ F₁ ∇ F₀ ∇ SIO₃
 ∇ = Exclusive OR

L = LOW
 H = HIGH

Z = High-Impedance

TABLE 4. SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0 = \text{LOW}$ (Note 4)

(Hex) $I_8 I_7 I_6 I_5$	Special Function	ALU Function	ALU Shifter Function	SIO ₃		SIO ₀	Q Reg & Shifter Function	QIO ₃	QIO ₀	WRITE
				Most Sig Slice	Other Slices					
0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 1)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
1	(Note 5)									
2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
3	(Note 5)									
4	Increment by One or Two	$F = S + 1 + C_n$	$F \rightarrow Y$	Input	Input	Parity	Hold	Z	Z	L
5	Sign/Magnitude Two's Complement	$F = S + C_n$ if $Z = L$ $F = S + C_n$ if $Z = H$	$F \rightarrow Y$ (Note 3)	Input	Input	Parity	Hold	Z	Z	L
6	Two's Complement Multiply, Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $F/2 \rightarrow Y$ (Note 2)	Z	Input	F_0	Log $Q/2 \rightarrow Q$	Input	Q_0	L
7	(Note 5)									
8	Single Length Normalize	$F = S + C_n$	$F \rightarrow Y$	F_3	F_3	Z	Log $2Q \rightarrow Q$	Q_3	Input	L
9	(Note 5)									
A	Double Length Normalize and First Divide Op	$F = S + C_n$	Log $2F \rightarrow Y$	$R_3 \nabla F_3$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
B	(Note 5)									
C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log $2F \rightarrow Y$	$R_3 \nabla F_3$	F_3	Input	Log $2Q \rightarrow Q$	Q_3	Input	L
D	(Note 5)									
E	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	$F \rightarrow Y$	F_3	F_3	Z	Log $2Q \rightarrow Q$	Q_3	Input	L
F	(Note 5)									

Notes: 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \nabla \text{OVR}$ is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \nabla F_3$ is generated at the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Not valid.

L = LOW Z = High-Impedance
H = HIGH ∇ = Exclusive OR
X = Don't Care Parity = $\text{SIO}_3 \nabla F_3 \nabla F_2 \nabla F_1 \nabla F_0$

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the $Y_{0,3}$ pins are all LOW. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903A instructions.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine instruction inputs, I_{0-8} ; the Instruction Enable input, IEN; the LSS input; and the WRITE/MSS input/output.

The $\overline{\text{WRITE}}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{\text{WRITE}}$ output as a function of the Am2903A instruction inputs.

On the Am2903A, when $\overline{\text{IEN}}$ is HIGH, the $\overline{\text{WRITE}}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{\text{IEN}}$ is LOW, the $\overline{\text{WRITE}}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903A instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903A divide operation (see Figure 2).

Programming the Am2903A Slice Position

Tying the $\overline{\text{LSS}}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{\text{WRITE}}$ output signal onto the $\overline{\text{WRITE/MSS}}$ bidirectional I/O pin. When $\overline{\text{LSS}}$ is tied HIGH, the $\overline{\text{WRITE/MSS}}$ pin becomes an input pin; tying the $\overline{\text{WRITE/MSS}}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS). The $\overline{\text{WRITE/MSS}}$ pin must be tied HIGH through a resistor. $\overline{\text{WRITE/MSS}}$ and $\overline{\text{LSS}}$ should not be connected together.

TABLE 5. Am2903A STATUS OUTPUTS

(Hex) 16171615	(Hex) 14131211	I ₀	G _i (i = 0 to 3)	P _i (i = 0 to 3)	C _{n+4}	P/OVR		G/N		Z(ŌE _Y = LOW)		
						Most Sig Slice	Other Slices	Most Sig Slice	Other Slices	Most Sig Slice	Intermediate Slice	Least Sig Slice
X	0	H	0	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	1	X	$\bar{R}_i \wedge S_i$	$\bar{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	2	X	$R_i \wedge \bar{S}_i$	$R_i \vee \bar{S}_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	4	X	0	S _i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	5	X	0	\bar{S}_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	6	X	0	R _i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	7	X	0	\bar{R}_i	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	8	X	0	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	9	X	$\bar{R}_i \wedge S_i$	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	B	X	$\bar{R}_i \wedge \bar{S}_i$	$R_i \vee S_i$	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	D	X	$\bar{R}_i \wedge \bar{S}_i$	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
X	F	X	$\bar{R}_i \wedge \bar{S}_i$	1	0	0	0	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S _i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	Input	Input	Q ₀
1	0	L	(Note 6)									
1	8	L	(Note 6)									
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S _i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	Input	Input	Q ₀
3	0	L	(Note 6)									
4	0	L	(Note 1)	(Note 2)	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$	$\bar{Y}_0\bar{Y}_1\bar{Y}_2\bar{Y}_3$
5	0	L	0	S _i if Z = L S _i if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃ if Z = L $F_3 \nabla S_3$ if Z = H	\bar{G}	S ₃	Input	Input
6	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S _i if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	Input	Input	Q ₀
7	0	L	(Note 6)									
8	0	L	0	S _i	(Note 3)	Q ₂ ∇ Q ₁	\bar{P}	Q ₃	\bar{G}	$\bar{Q}_0\bar{Q}_1\bar{Q}_2\bar{Q}_3$	$\bar{Q}_0\bar{Q}_1\bar{Q}_2\bar{Q}_3$	$\bar{Q}_0\bar{Q}_1\bar{Q}_2\bar{Q}_3$
9	0	L	(Note 6)									
9	8	L	(Note 6)									
A	0	L	0	S _i	(Note 4)	F ₂ ∇ F ₁	\bar{P}	F ₃	\bar{G}	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)									
C	0	L	$R_i \wedge S_i$ if Z = L $R_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)									
E	0	L	$R_i \wedge S_i$ if Z = L $R_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $R_i \vee S_i$ if Z = H	$G \vee PC_n$	$C_{n+3} \nabla C_{n+4}$	\bar{P}	F ₃	\bar{G}	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)									

Notes: 1. If \bar{LSS} is LOW, G₀ = S₀ and G₁, 2, 3 = 0. If \bar{LSS} is HIGH, G₀, 1, 2, 3 = 0.
2. If \bar{LSS} is LOW, P₀ = 1 and P₁, 2, 3 = S₁, 2, 3. If \bar{LSS} is HIGH, P_i = S_i.
3. At the most significant slice, C_{n+4} = Q₃ ∇ Q₂. At other slices, C_{n+4} = G \vee PC_n.
4. At the most significant slice, C_{n+4} = F₃ ∇ F₂. At other slices, C_{n+4} = G \vee PC_n.
5. Z = Q₀ Q₁ Q₂ Q₃ F₀ F₁ F₂ F₃.
6. Not valid.

L = LOW = 0
H = HIGH = 1
 \vee = OR
 \wedge = AND
 ∇ = EXCLUSIVE OR
P = P₃P₂P₁P₀
G = G₃ \vee G₂P₃ \vee G₁P₂P₃ \vee G₀P₁P₂P₃
C_{n+3} = G₂ \vee G₁P₂ \vee G₀P₁P₂ \vee C_nP₀P₁P₂

Am2903A Special Functions

The Am2903A provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

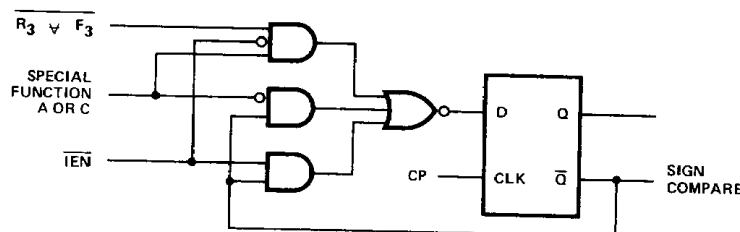
Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903A. These functions provide both single- and double-precision divide operations and can be performed in

"n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.



DF000400

Figure 2. Sign Compare Flip-Flop

The sign compare signal appears at the Z output of the most significant slice during special functions C and E. Refer to Table 5.

Cycle Times for 16-Bit System for Common Operations

Figure 3 shows a typical configuration using 4 Am2903A Superslices, an Am2902A carry lookahead chip, and the Am2904 for shift multiplexers, status registers, and carry-in control. For the system enclosed within the dashed lines, there are four major switching paths whose values for various kinds of cycles are summarized below, and shown on the timing waveform, Figure 4.

1. MICROCYCLE TIME (TCHCH).

The minimum time which must elapse between a LOW-TO-HIGH clock transition and the next LOW-TO-HIGH clock transition.

2. DATA SET-UP TIME (TDVCH).

The minimum time which must be allowed between valid, stable data on the D inputs and the clock LOW-TO-HIGH transition.

3. D TO Y (TDVYV).

The maximum time required to obtain valid Y output data after the D inputs are valid. This is the combinational delay through the parts from D to Y.

4. CP TO Y (TCHYV).

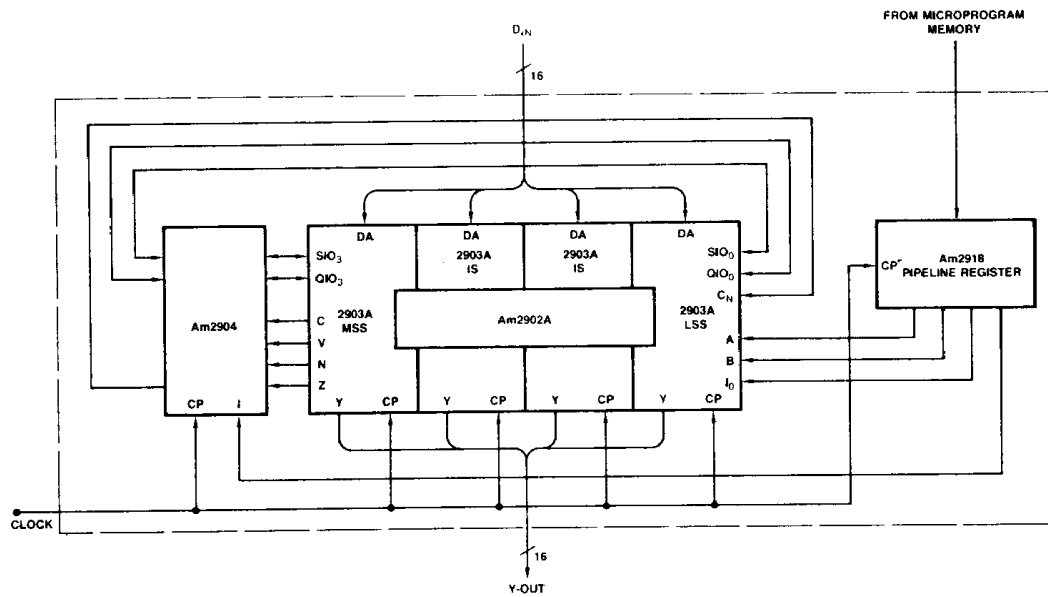
The maximum time required to obtain valid Y outputs after a clock LOW-TO-HIGH transition.

The types of cycles for which data is summarized are as follows:

1. Logic – Any logical operation without a shift.
2. Logic Rotate – Any logic operation with a rotate or shift.
3. Arithmetic – An add or subtract with no shift.
4. Multiply – The first cycle of a 2's complement multiply instruction. Subsequent cycles require less time.
5. Divide – The iterative divide cycle. The first divide instruction and the last divide (correction) instruction require less time.

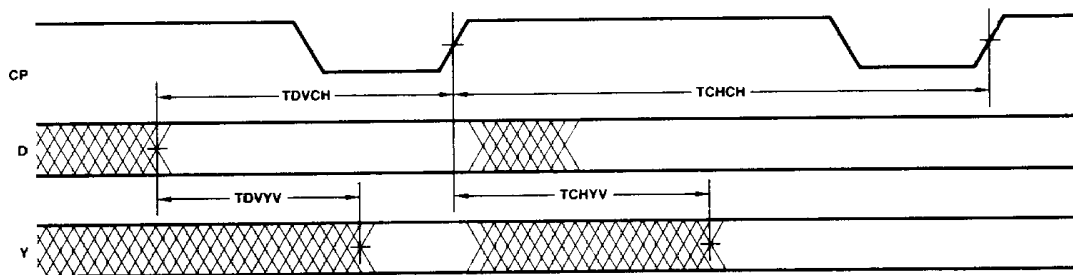
Time in ns Over Commercial Operating Range

CYCLE	TCHCH	TDVCH	TDVYV	TCHYV
LOGIC	99	79	59	81
LOGIC ROTATE	118	99	79	98
ARITHMETIC	130	109	91	112
MULTIPLY	152	113	95	135
DIVIDE	139	113	95	121



DF000441

Figure 3. 16-Bit System with Am2903A, Am2902A, Am2904



WF002590

Figure 4. Timing Waveforms for Data in, Clock, and Y Out

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 (Ambient) Temperature Under Bias -55 to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5 V to +7.0 V
 DC Voltage Applied to Outputs For
 High Output State -0.5 V to +V_{CC} Max.
 DC Input Voltage -0.5 V to +5.5 V
 DC Output Current, Into Outputs 30 mA
 DC Input Current -30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature 0 to +70°C
 Supply Voltage +4.75 V to +5.25 V

Military (M) Devices

Temperature -55 to +125°C
 Supply Voltage +4.5 V to +5.5 V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Table continued on next page

Parameters	Description	Test Conditions (Note 2)		Min.	Typ. (Note 1)	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1.6 mA Y ₀ -Y ₃ , \bar{G}/N	2.4			Volts
			I _{OH} = -800 μ A DB _{0,3} , \bar{P}/OVR SIO ₀ , SIO ₃ , QIO ₀ , QIO ₃ , WRITE, C _n + 4	2.4			
I _{CEX}	Output Leakage Current for Z Output (Note 4)	V _{CC} = Min., V _{OH} = 5.5 V V _{IN} = V _{IH} or V _{IL}				250	μ A
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	Y ₀ , Y ₁ , Y ₂ Y ₃ , Z	I _{OL} = 20 mA (COM'L) I _{OL} = 16 mA (MIL)		0.5	Volts
			DB ₀ , DB ₁ , DB ₂ , DB ₃	I _{OL} = 12 mA (COM'L) I _{OL} = 8.0 mA (MIL)		0.5	
			\bar{G}/N	I _{OL} = 18 mA		0.5	
			\bar{P}/OVR	I _{OL} = 10 mA		0.5	
			C _n + 4, SIO ₀ SIO ₃ , QIO ₀ QIO ₃ , WRITE	I _{OL} = 8.0 mA		0.5	
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)		2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)				0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = Min., I _{IN} = -18 mA				-1.5	Volts
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = 0.5 V (Note 4)	C _n			-3.6	mA
			Y ₀ , Y ₁ , Y ₂ , Y ₃			-1.13	
			I ₀ , I ₁ , I ₂ , I ₃ , I ₄ DA ₀ , DA ₁ , DA ₂ , DA ₃			-0.72	
			SIO ₀ , SIO ₃ , QIO ₀ , QIO ₃ , MSS, DB ₀ , DB ₁ DB ₂ , DB ₃			-0.77	
			All other inputs			-0.36	
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = 2.7 V (Note 4)	C _n			200	μ A
			Y ₀ , Y ₁ , Y ₂ , Y ₃			110	
			I ₀ -I ₄ , DA ₀ -DA ₃			40	
			SIO ₀ , SIO ₃ , QIO ₀ , QIO ₃ , DB _{0,3} , MSS			90	
			All other inputs			20	

DC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 2)				Min.	Typ. (Note 1)	Max.	Units
I _I	Input HIGH Current	V _{CC} = Max., V _{IN} = 5.5 V						1.0	mA
I _{OZH} I _{OZL}	Off State (HIGH Impedance) Output Current	V _{CC} = Max., (Note 4)	Y ₀ -Y ₃	V _O = 2.4 V			110	μA	
	V _O = 0.5 V					-1130			
			DB ₀₋₃ , QIO ₀ , QIO ₃ , SIO ₀ , SIO ₃ , WRITE/MSS	V _O = 2.4 V			90		
				V _O = 0.5 V			-770		
I _{OS}	Output Short Circuit Current (Note 3)	V _{CC} = Max. + 0.5 V V _O = 0.5 V				-30		-85	mA
I _{CC}	Power Supply Current (Note 5)	V _{CC} = Max.	T _A = 25°C			220	335	mA	
			COM'L	T _A = 0 to 70°C			350		
				T _A = 70°C			291		
			MIL	T _C = -55 to 125°C			395		
				T _C = 125°C			258		

- Notes: 1. Typical limits are at $V_{CC} = 5.0 \text{ V}$, 25°C ambient and maximum loading.
2. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_0-3 , DB₀₋₃, SIO_{0,3}, QIO_{0,3} and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be static tested in a noise-free environment (not functionally tested).

I. Am2903A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The Am2903A Switching Characteristics are a function of the power supply voltage, the temperature, and the operating

mode of the devices. The data has been condensed onto the tables below. All numbers in the tables are in ns.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable to
6	Clock and Write Pulse	4.75 to 5.25 V, 0 to 70°C	All Functions
7	Enable/Disable Times	4.75 to 5.25 V, 0 to 70°C	All Functions
8	Setup and Hold Times	4.75 to 5.25 V, 0 to 70°C	All Functions
1-2	Combinational Delays	4.75 to 5.25 V, 0 to 70°C	Standard Function and Increment by 1 or 2
1-3	Combinational Delays	4.75 to 5.25 V, 0 to 70°C	Multiply Instructions
1-4	Combinational Delays	4.75 to 5.25 V, 0 to 70°C	Divide Instructions
1-5	Combinational Delays	4.75 to 5.25 V, 0 to 70°C	Sign Magnitude to Two's Complement Conversion
1-6	Combinational Delays	4.75 to 5.25 V, 0 to 70°C	Single Length Normalization

I-1. Am2903A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the Am2903A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25 V. All data are in ns, with inputs switching between 0 and 3 V at 1 V/ns and measurements made at 1.5 V. All outputs have maximum DC load.

TABLE 6. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS


Minimum Clock Low Time	30 ns
Minimum Clock High Time	30 ns
Minimum Time CP and WE both Low to Write	15 ns

TABLE 7. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
$\overline{OE}Y$	Y	25	21
\overline{OEB}	DB	25	21
I_B	SIO	25	21
I_B	QIO	38	38
I_{B765}	QIO	38	38
I_{43210}	QIO	38	38
\overline{LSS}	WR	25	21

Note: $C_L = 5.0$ pF for output disable tests. Measurement is made to a 0.5 V change on the output.

TABLE 8. SETUP AND HOLD TIMES ALL FUNCTIONS

		HIGH-to-LOW		LOW-to-HIGH		
						
From	With Respect to	Setup	Hold	Setup	Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q (Note 1)
WE HIGH	CP	15	Tpwl		0	Prevent Writing
WE LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
QIO _{0, 3}	CP	Don't Care	Don't Care	17	3	Shift Q
I ₈₇₆₅	CP	12	–	20	0	Write into Q (Note 2)
IEN HIGH	CP	24			0	Prevent Writing into Q
IEN LOW	CP	Don't Care	Don't Care	21	0	Write into Q
I ₄₃₂₁₀	CP	18	–	32	0	Write into Q (Note 2)

- Notes:
1. The internal Y-bus to RAM setup condition will be met 5 ns after valid Y output ($\overline{OE}_Y = 0$).
 2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
 3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
 4. \overline{WE} controls writing into the RAM. \overline{IEN} controls writing into Q and, indirectly, controls \overline{WE} through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, \overline{IEN} and \overline{WE} must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the \overline{WE} LOW and \overline{IEN} LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
 5. A and B addresses must be set up prior to the clock HIGH-to-LOW transition to latch data at the RAM output.
 6. Writing occurs when CP and \overline{WE} are both LOW. The B address should be stable during this entire period.
 7. Because I₈₇₆₅ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless \overline{IEN} is HIGH, which prevents writing.
 8. The setup time prior to the clock LOW-to-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual setup time requirement on I₄₃₂₁₀ relative to the clock LOW-to-HIGH transition is the longer of (1) the setup time prior to clock L → H and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified

I-2 STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

From	To											
	Y	C _{n+4}	\bar{G}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₀	SIO ₃	SIO ₀ Parity
A, B Addr	67	55	52	74	61	67	28	-	-	41	62	78
DA, DB	58	50	40	65	54	58	-	-	-	35	59	65
Cn	33	18	-	35	28	26	-	-	-	23	30	38
lg-0	64	64	50	72	61	62	-	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	-	22	37	54	60
SIO ₀ , SIO ₃	23	-	-	29	-	-	-	-	-	-	29	19
MSS	44	-	44	44	44	44	-	-	-	44	44	44
Y	-	-	-	17	-	-	-	-	-	-	-	-
IEN	-	-	-	-	-	-	-	20	-	-	-	-
EA	58	50	40	65	54	58	-	-	-	35	59	65

Notes: 1. A "-" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.

Standard Functions: See Table 2

Increment SF 4: $F = S + 1 + C_n$

I-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To											
	Slice	Y	C _{n+4}	\bar{G}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₀	
A, B Addr	MSS	67	(55)	-	-	(61)	(67)	(28)	-	-	(41)	
	IS	(67)	(55)	(52)	-	-	-	(28)	-	-	(41)	
	LSS	(67)	(55)	(52)	-	-	-	(28)	-	-	(41)	
DA, DB	MSS	58	(50)	-	-	(54)	(58)	-	-	-	(35)	
	IS	(58)	(50)	(40)	-	-	-	-	-	-	(35)	
	LSS	(58)	(50)	(40)	-	-	-	-	-	-	(35)	
Cn	MSS	35	(18)	-	-	(28)	(26)	-	-	-	(23)	
	IS	(33)	(18)	-	-	-	-	-	-	-	(23)	
	LSS	(33)	(18)	-	-	-	-	-	-	-	(23)	
lg-0	MSS	94	75	-	-	88	88	-	-	(26)	73*	
	IS	94	75	71	-	-	-	-	-	(26)	73*	
	LSS	94	75	71	30	-	-	-	(34)	(26)	73*	
CP	MSS	58	(42)	-	-	(54)	(58)	(22)	-	(22)	(37)	
	IS	(58)	(42)	(43)	-	-	-	(22)	-	(22)	(37)	
	LSS	90	71	67	26	-	-	(22)	-	(22)	69	
Z	MSS	64	45	-	-	58	58	-	-	-	43	
	IS	64	45	41	-	-	-	-	-	-	43	
	LSS	-	-	-	-	-	-	-	-	-	-	
SIO ₀ , SIO ₃	Any	(23)	-	-	-	-	-	-	-	-	-	

Notes: 1. A "-" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

Unsigned Multiply

SF 0: $F = S + C_n$ if $Z = 0$
 $F = S + R + C_n$ if $Z = 1$
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$
 $Y_3 = C_n + 4$ (MSS)
 $Z = Q_0$ (LSS)

Two's Complement Multiply

SF 2: $F = S + C_n$ if $Z = 0$
 $F = R + S + C_n$ if $Z = 1$
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$
 $Y_3 = F_3 \oplus \text{OVR}$ (MSS)
 $Z = Q_0$ (LSS)

Two's Complement Multiply Last Cycle

SF 6: $F = S + C_n$ if $Z = 0$
 $F = S - R - 1 + C_n$ if $Z = 1$
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$
 $Y_3 = \text{OVR} \oplus$ (MSS)
 $Z = Q_0$ (LSS)

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified

I-4 DIVIDE INSTRUCTIONS (SF A/SF C, SF E)

From	To										
	Slice	Y	C _n + 4	\bar{Q}, \bar{P}	Z	N	OVR	DB	WR	QIO _{0,3}	SIO ₃
A, B Addr	MSS	(67)	61/(55)	—	74/—	61	67	(28)	—	—	62
	IS	(67)	(55)	(52)	(74)/—	—	—	(28)	—	—	(62)
	LSS	(67)	(55)	(52)	(74)/—	—	—	(28)	—	—	(62)
DA, DB	MSS	(58)	55/(50)	—	65/—	54	58	—	—	—	59
	IS	(58)	(50)	(40)	(65)/—	—	—	—	—	—	(59)
	LSS	(58)	(50)	(40)	(65)/—	—	—	—	—	—	(59)
C _n	MSS	(33)	33/(18)	—	35/—	28	27	—	—	—	32
	IS	(33)	(18)	—	(35)/—	—	—	—	—	—	(30)
	LSS	(33)	(18)	—	(35)/—	—	—	—	—	—	(30)
I ₈₋₀	MSS	64/84	75/68	—	72/29	61/77	62/77	—	—	(26)	62/83*
	IS	64/84	64/68	50/70	72/—	—	—	—	—	(26)	62/83*
	LSS	64/84	64/68	50/70	72/—	—	—	—	(34)	(26)	62/83*
CP	MSS	(58)/80	46/64	—	61/25	54/66	58/66	(22)	—	(22)	54/79
	IS	(58)	(42)	(43)	(61)/—	—	—	(22)	—	(22)	(54)
	LSS	(58)	(42)	(43)	(61)/—	—	—	(22)	—	(22)	(54)
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—/55	—/39	—/41	—	—	—	—	—	—	—/54
	LSS	—/55	—/39	—/41	—	—	—	—	—	—	—/54
SIO ₀ , SIO ₃	Any	(23)	—	—	—	—	—	—	—	—	—

- Notes: 1. A "—" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op

SF A: $F = S + C_n$
 $Y = \text{Log. } 2F$
 $Q = \text{Log. } 2Q$
 $SIO_3 = F_3 \oplus R_3$ (MSS)
 $C_n + 4 = F_3 \oplus F_2$ (MSS)
 $OVR = F_2 \oplus F_1$ (MSS)
 $Z = Q_0 \bar{Q}_1 \bar{Q}_2 \bar{Q}_3 \bar{F}_0 \bar{F}_1 \bar{F}_2 \bar{F}_3$

Two's Complement Divide

SF C: $F = R + S + C_n$ if $Z = 0$
 $F = S - R - 1 + C_n$ if $Z = 1$
 $Y = \text{Log. } 2F$
 $Q = \text{Log. } 2Q$
 $SIO_3 = F_3 \oplus R_3$ (MSS)
 $Z = F_3 \oplus R_3$ (MSS) from previous cycle

Two's Complement Divide Correction and Remainder

SF E: $F = R + S + C_n$ if $Z = 0$
 $F = S - R - 1 + C_n$ if $Z = 1$
 $Y = F$
 $Q = \text{Log. } 2Q$
 $Z = F_3 \oplus R_3$ (MSS) from previous cycle

SWITCHING CHARACTERISTICS over the COMMERCIAL operating range unless otherwise specified

I-5 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

From	To										
	Slice	Y	C _{n+4}	\bar{G}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₃
A, B Addr	MSS	97	81	-	42	89	89	(28)	-	-	102
	IS	(67)	(55)	(52)	-	-	-	(28)	-	-	(62)
	LSS	(67)	(55)	(52)	-	-	-	(28)	-	-	(62)
DA, DB	MSS	94	76	-	37	84	84	-	-	-	97
	IS	(58)	(50)	(40)	-	-	-	-	-	-	(59)
	LSS	(58)	(50)	(40)	-	-	-	-	-	-	(59)
Cn	MSS	33	(18)	-	-	32	27	-	-	-	(30)
	IS	(33)	(18)	-	-	-	-	-	-	-	(30)
	LSS	(33)	(18)	-	-	-	-	-	-	-	(30)
I ₈₋₀	MSS	85	67	-	28	82	73	-	-	(26)	88*
	IS	85	67	63	-	-	-	-	-	(26)	88*
	LSS	85	67	63	-	-	-	-	(34)	(26)	88*
CP	MSS	94	76	-	37	84	84	(22)	-	(22)	97
	IS	(58)	(42)	(43)	-	-	-	(22)	-	(22)	(54)
	LSS	(58)	(42)	(43)	-	-	-	(22)	-	(22)	(54)
Z	MSS	-	-	-	-	-	-	-	-	-	-
	IS	57	39	35	-	-	-	-	-	-	60
	LSS	57	39	35	-	-	-	-	-	-	60
SIO ₀ , SIO ₃	Any	(23)	-	-	-	-	-	-	-	-	-

Notes: 1. A "-" means the delay path does not exist.

2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.

3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

SF 5: $F = S + C_n$ if $Z = 0$
 $F = \bar{S} + C_n$ if $Z = 1$

$Y_3 = S_3 \oplus F_3$ (MSS)
 $Z = S_3$ (MSS)

$Q = Q$
 $N = F_3$ if $Z = 0$
 $N = F_3 \oplus S_3$ if $Z = 1$

I-6 SINGLE LENGTH NORMALIZATION (SF 8)

From	To										
	Slice	Y	C _n + 4	\bar{Q}_0, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₃
A, B Addr	MSS	(67)	-	-	-	-	-	(28)	-	-	(62)
	IS	(67)	(55)	(52)	-	-	-	(28)	-	-	(62)
	LSS	(67)	(55)	(52)	-	-	-	(28)	-	-	(62)
DA, DB	MSS	(58)	-	-	-	-	-	-	-	-	(59)
	IS	(58)	(50)	(40)	-	-	-	-	-	-	(59)
	LSS	(58)	(50)	(40)	-	-	-	-	-	-	(59)
Cn	MSS	(33)	-	-	-	-	-	-	-	-	(30)
	IS	(33)	(18)	-	-	-	-	-	-	-	(30)
	LSS	(33)	(18)	-	-	-	-	-	-	-	(30)
I ₈₋₀	MSS	64	37	-	29	24	24	-	-	(26)	62*
	IS	64	64	50	29	-	-	-	-	(26)	62*
	LSS	64	64	50	29	-	-	-	(34)	(26)	62*
CP	MSS	(58)	29	-	26	26	29	(22)	-	(22)	(54)
	IS	(58)	(42)	(43)	26	-	-	(22)	-	(22)	(54)
	LSS	(58)	(42)	(43)	26	-	-	(22)	-	(22)	(54)
Z	MSS	-	-	-	-	-	-	-	-	-	-
	IS	-	-	-	-	-	-	-	-	-	-
	LSS	-	-	-	-	-	-	-	-	-	-
SIO ₀ , SIO ₃	Any	(23)	-	-	-	-	-	-	-	-	-

Notes: 1. A "-" means the delay path does not exist.

2. An "****" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "****" is the delay to correct data on an enabled output.

3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

SF 8: F = S + Cn
N = Q₃ (MSS)
Y = F
Q = Log. 2Q

$$C_n + 4 = Q_3 \oplus Q_2 \text{ (MSS)}$$

$$Z = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$$

$$OVR = Q_2 \oplus Q_1 \text{ (MSS)}$$

II. Am2903A GUARANTEED MILITARY RANGE PERFORMANCE

The Am2903A Switching Characteristics are a function of the power supply voltage, the temperature, and the operating

mode of the devices. The data has been condensed onto the tables below. All numbers are in ns.

INDEX TO SWITCHING TABLES

Table	Data Type	Conditions	Applicable to
9	Clock and Write Pulse	4.5 to 5.5 V, -55 to 125°C	All Functions
10	Enable/Disable Times	4.5 to 5.5 V, -55 to 125°C	All Functions
11	Setup and Hold Times	4.5 to 5.5 V, -55 to 125°C	All Functions
1-2	Combinational Delays	4.5 to 5.5 V, -55 to 125°C	Standard Function and Increment by 1 or 2
1-3	Combinational Delays	4.5 to 5.5 V, -55 to 125°C	Multiply Instructions
1-4	Combinational Delays	4.5 to 5.5 V, -55 to 125°C	Divide Instructions
1-5	Combinational Delays	4.5 to 5.5 V, -55 to 125°C	Sign Magnitude to Two's Complement Conversion
1-6	Combinational Delays	4.5 to 5.5 V, -55 to 125°C	Single Length Normalization

II-1. Am2903A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the Am2903A over the military operating range of -55 to 125°C, with V_{CC} from 4.5 to 5.5 V. All data are in ns, with inputs switching between 0 and 3 V at 1 V/ns and measurements made at 1.5 V. All outputs have maximum DC load.

TABLE 9. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

Minimum Clock Low Time	30 ns
Minimum Clock High Time	30 ns
Minimum Time CP and WE both Low to Write	30 ns

TABLE 10. ENABLE/DISABLE TIMES ALL FUNCTIONS

From	To	Enable	Disable
\overline{OEY}	Y	25	21
\overline{OEB}	DB	25	21
I_8	SIO	25	21
I_8	QIO	38	38
I_{8765}	QIO	38	38
I_{43210}	QIO	38	38
\overline{LSS}	WR	30	25

Note: $C_L = 5.0$ pF for output disable tests. Measurement is made to a 0.5 V change on the output.

TABLE 11. SETUP AND HOLD TIMES ALL FUNCTIONS

		HIGH-to-LOW		LOW-to-HIGH		
		Setup	Hold	Setup	Hold	
From	With Respect to	Setup	Hold	Setup	Hold	Comments
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q (Note 1)
\overline{WE} HIGH	CP	15	Tpwl		0	Prevent Writing
\overline{WE} LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	Tpwl		3	Write Data into B Address
QIO _{0,3}	CP	Don't Care	Don't Care	17	3	Shift Q
I ₈₇₆₅	CP	12	–	20	0	Write into Q (Note 2)
\overline{IEN} HIGH	CP	24			0	Prevent Writing into Q
\overline{IEN} LOW	CP	Don't Care	Don't Care	21	0	Write into Q
I ₄₃₂₁₀	CP	18	–	32	0	Write into Q (Note 2)

- Notes:
1. The internal Y-bus to RAM setup condition will be met 5 ns after valid Y output ($\overline{OE}_Y = 0$).
 2. The setup time with respect to CP falling edge is to prevent writing. The setup time with respect to CP rising edge is to enable writing.
 3. For all other setup conditions not specified in this table, the setup time should be the delay to stable Y output, plus the Y to RAM internal setup time. Even if the RAM is not being loaded, this setup condition ensures valid writing into the Q register and sign compare flip-flop.
 4. \overline{WE} controls writing into the RAM. \overline{IEN} controls writing into Q and, indirectly, controls \overline{WE} through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, \overline{IEN} and \overline{WE} must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the \overline{WE} LOW and \overline{IEN} LOW setup times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
 5. A and B addresses must be set up prior to the clock HIGH-to-LOW transition to latch data at the RAM output.
 6. Writing occurs when CP and \overline{WE} are both LOW. The B address should be stable during this entire period.
 7. Because I₈₇₆₅ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless \overline{IEN} is HIGH, which prevents writing.
 8. The setup time prior to the clock LOW-to-HIGH transition occurs in parallel with the setup time prior to the clock HIGH-to-LOW transition and the clock LOW time. The actual setup time requirement on I₄₃₂₁₀ relative to the clock LOW-to-HIGH transition is the longer of (1) the setup time prior to clock L → H and (2) the sum of the setup time prior to clock H → L and the clock LOW time.

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified

II-2 STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF 4)

From	To											
	Y	C _{n+4}	\bar{G}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₀	SIO ₃	SIO ₀ Parity
A, B Addr	70	58	52	78	68	67	28	—	—	47	71	84
DA, DB	60	52	40	66	55	58	—	—	—	35	61	74
Cn	35	19	—	41	31	29	—	—	—	23	33	40
I ₈₋₀	72	69	56	80	71	69	—	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	—	25	41	61	66
SIO ₀ , SIO ₃	26	—	—	29	—	—	—	—	—	—	29	19
MSS	44	—	44	44	44	44	—	—	—	44	44	44
Y	—	—	—	17	—	—	—	—	—	—	—	—
TEN	—	—	—	—	—	—	—	20	—	—	—	—
EA	60	52	40	66	55	58	—	—	—	35	61	74

Notes: 1. A "—" means the delay path does not exist.

2. An "****" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "****" is the delay to correct data on an enabled output.

Standard Functions: See Table 2

Increment SF 4: $F = S + 1 + C_n$

II-3 MULTIPLY INSTRUCTIONS (SF 0, SF 2, SF 6)

From	To										
	Slice	Y	C _{n+4}	\bar{G}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₀
A, B Addr	MSS	72	(58)	—	—	(68)	(67)	(28)	—	—	(47)
	IS	(70)	(58)	(52)	—	—	—	(28)	—	—	(47)
	LSS	(70)	(58)	(52)	—	—	—	(28)	—	—	(47)
DA, DB	MSS	62	(52)	—	—	(55)	(58)	—	—	—	(35)
	IS	(60)	(52)	(40)	—	—	—	—	—	—	(35)
	LSS	(60)	(52)	(40)	—	—	—	—	—	—	(35)
Cn	MSS	40	(19)	—	—	(31)	(29)	—	—	—	(23)
	IS	(35)	(19)	—	—	—	—	—	—	—	(23)
	LSS	(35)	(19)	—	—	—	—	—	—	—	(23)
I ₈₋₀	MSS	108	84	—	—	98	98	—	—	(26)	81*
	IS	108	84	80	—	—	—	—	—	(26)	81*
	LSS	108	84	80	33	—	—	—	(36)	(26)	81*
CP	MSS	62	(42)	—	—	(55)	(58)	(22)	—	(25)	(41)
	IS	(60)	(42)	(43)	—	—	—	(22)	—	(25)	(41)
	LSS	104	80	74	29	—	—	(22)	—	(25)	77
Z	MSS	75	51	—	—	65	65	—	—	—	48
	IS	75	51	47	—	—	—	—	—	—	48
	LSS	—	—	—	—	—	—	—	—	—	—
SIO ₀ , SIO ₃	Any	(26)	—	—	—	—	—	—	—	—	—

Notes: 1. A "—" means the delay path does not exist.

2. An "****" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "****" is the delay to correct data on an enabled output.

3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

Unsigned Multiply

SF 0: $F = S + C_n$ if $Z = 0$
 $F = S + R + C_n$ if $Z = 1$
 $Y_3 = C_{n+4}$ (MSS)
 $Z = Q_0$ (LSS)
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$

Two's Complement Multiply

SF 2: $F = S + C_n$ if $Z = 0$
 $F = R + S + C_n$ if $Z = 1$
 $Y_3 = F_3 \oplus \text{OVR}$ (MSS)
 $Z = Q_0$ (LSS)
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$

Two's Complement Multiply Last Cycle

SF 6: $F = S + C_n$ if $Z = 0$
 $F = S - R - 1 + C_n$ if $Z = 1$
 $Y_3 = \text{OVR} \oplus F_3$ (MSS)
 $Z = Q_0$ (LSS)
 $Y = \text{Log. } F/2$
 $Q = \text{Log. } Q/2$

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified

II-4 DIVIDE INSTRUCTION (SF A/SF C, SF E)

From	To										
	Slice	Y	C _n + 4	\bar{G}, \bar{P}	Z	N	OVR	DB	$\bar{W}R$	QIO _{0,3}	SIO ₃
A, B Addr	MSS	(70)	72/(58)	-	78/-	68	67	(28)	-	-	71
	IS	(70)	(58)	(52)	(78)/-	-	-	(28)	-	-	(71)
	LSS	(70)	(58)	(52)	(78)/-	-	-	(28)	-	-	(71)
DA, DB	MSS	(60)	66/(52)	-	66/-	55	58	-	-	-	61
	IS	(60)	(52)	(40)	(66)/-	-	-	-	-	-	(61)
	LSS	(60)	(52)	(40)	(66)/-	-	-	-	-	-	(61)
C _n	MSS	(35)	37/(19)	-	41/-	31	29	-	-	-	36
	IS	(35)	(19)	-	(41)/-	-	-	-	-	-	(33)
	LSS	(35)	(19)	-	(41)/-	-	-	-	-	-	(33)
I _{g-0}	MSS	72/96	89/79	-	80/33	71/91	69/91	-	-	(26)	75/98
	IS	72/96	69/79	56/79	80/-	-	-	-	-	(26)	75/98
	LSS	72/96	69/79	56/79	80/-	-	-	-	(36)	(26)	75/98
CP	MSS	(60)/91	51/74	-	67/28	55/74	58/74	(22)	-	(25)	61/93
	IS	(60)	(42)	(43)	(67)/-	-	-	(22)	-	(25)	(61)
	LSS	(60)	(42)	(43)	(67)/-	-	-	(22)	-	(25)	(61)
Z	MSS	-	-	-	-	-	-	-	-	-	-
	IS	-/63	-/46	-/46	-	-	-	-	-	-	-/65
	LSS	-/63	-/46	-/46	-	-	-	-	-	-	-/65
SIO ₀ , SIO ₃	Any	(26)	-	-	-	-	-	-	-	-	-

- Notes: 1. A "-" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.

Double Length Normalize and First Divide Op

SF A: $F = S + C_n$

$$SIO_3 = F_3 \oplus R_3 \text{ (MSS)}$$

$$C_n + 4 = F_3 \oplus F_2 \text{ (MSS)}$$

$$OVR = F_2 \oplus F_1 \text{ (MSS)}$$

$$Z = Q_0 \bar{Q}_1 \bar{Q}_2 \bar{Q}_3 \bar{F}_0 \bar{F}_1 \bar{F}_2 \bar{F}_3$$

$$Y = \text{Log. } 2F$$

$$Q = \text{Log. } 2Q$$

Two's Complement Divide

SF C: $F = R + S + C_n$ if $Z = 0$

$$F = S - R - 1 + C_n \text{ if } Z = 1$$

$$Y = \text{Log. } 2F$$

$$Q = \text{Log. } 2Q$$

$$SIO_3 = F_3 \oplus R_3 \text{ (MSS)}$$

$$Z = F_3 \oplus R_3 \text{ (MSS) from previous cycle}$$

Two's Complement Divide Correction and Remainder

SF E: $F = R + S + C_n$ if $Z = 0$

$$F = S - R - 1 + C_n \text{ if } Z = 1$$

$$Y = F$$

$$Q = \text{Log. } 2Q$$

$$Z = F_3 \oplus R_3 \text{ (MSS) from previous cycle}$$

SWITCHING CHARACTERISTICS over the MILITARY operating range unless otherwise specified

II-5 SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF 5)

From	To										
	Slice	Y	C _{n+4}	\bar{Q}, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₃
A, B Addr	MSS	114	95	-	49	106	106	(28)	-	-	125
	IS	(70)	(58)	(52)	-	-	-	(28)	-	-	(71)
	LSS	(70)	(58)	(52)	-	-	-	(28)	-	-	(71)
DA, DB	MSS	108	89	-	43	101	101	-	-	-	119
	IS	(60)	(52)	(40)	-	-	-	-	-	-	(61)
	LSS	(60)	(52)	(40)	-	-	-	-	-	-	(61)
Cn	MSS	36	(19)	-	-	35	29	-	-	-	(33)
	IS	(35)	(19)	-	-	-	-	-	-	-	(33)
	LSS	(35)	(19)	-	-	-	-	-	-	-	(33)
I ₈₋₀	MSS	98	79	-	33	97	88	-	-	(26)	109*
	IS	98	79	73	-	-	-	-	-	(26)	109*
	LSS	98	79	73	-	-	-	-	(36)	(26)	109*
CP	MSS	108	89	-	43	101	101	(22)	-	(25)	119
	IS	(60)	(42)	(43)	-	-	-	(22)	-	(25)	(61)
	LSS	(60)	(42)	(43)	-	-	-	(22)	-	(25)	(61)
Z	MSS	-	-	-	-	-	-	-	-	-	-
	IS	65	46	40	-	-	-	-	-	-	76
	LSS	65	46	40	-	-	-	-	-	-	76
IEN											
SIO ₀ , SIO ₃	Any	-	-	-	-	-	-	-	-	-	-

- Notes: 1. A "-" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

SF 5: $F = S + C_n$ if $Z = 0$
 $F = \bar{S} + C_n$ if $Z = 1$

$Y_3 = S_3 \oplus F_3$ (MSS)
 $Z = S_3$ (MSS)
 $Y = F$

$Q = Q$
 $N = F_3; Z = 0$
 $N = F_3 \oplus S_3; Z = 1$

II-6 SINGLE LENGTH NORMALIZATION (SF 8)

From	To										
	Slice	Y	C _n + 4	\bar{Q}_0, \bar{P}	Z	N	OVR	DB	WRITE/ MSS	QIO _{0,3}	SIO ₃
A, B Addr	MSS	(70)	—	—	—	—	—	(28)	—	—	(71)
	IS	(70)	(58)	(52)	—	—	—	(28)	—	—	(71)
	LSS	(70)	(58)	(52)	—	—	—	(28)	—	—	(71)
DA, DB	MSS	(60)	—	—	—	—	—	—	—	—	(61)
	IS	(60)	(52)	(40)	—	—	—	—	—	—	(61)
	LSS	(60)	(52)	(40)	—	—	—	—	—	—	(61)
C _n	MSS	(35)	—	—	—	—	—	—	—	—	(33)
	IS	(35)	(19)	—	—	—	—	—	—	—	(33)
	LSS	(35)	(19)	—	—	—	—	—	—	—	(33)
I ₈₋₀	MSS	72	47	—	33	27	27	—	—	(26)	75*
	IS	72	69	56	33	—	—	—	—	(26)	75*
	LSS	72	69	56	33	—	—	—	—	(26)	75*
CP	MSS	(60)	31	—	28	26	31	(22)	—	(25)	(61)
	IS	(60)	(42)	(43)	28	—	—	(22)	—	(25)	(61)
	LSS	(60)	(42)	(43)	28	—	—	(22)	—	(25)	(61)
Z	MSS	—	—	—	—	—	—	—	—	—	—
	IS	—	—	—	—	—	—	—	—	—	—
	LSS	—	—	—	—	—	—	—	—	—	—
SIO ₀ , SIO ₃	Any	(26)	—	—	—	—	—	—	—	—	—

Notes: 1. A "—" means the delay path does not exist.

2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.

3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

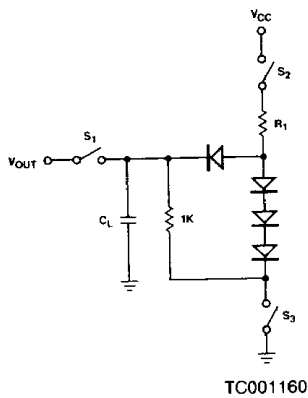
SF 8: F = S + C_n
N = Q₃ (MSS)
Y = F
Q = Log. 2Q

$$C_n + 4 = Q_3 \oplus Q_2 \text{ (MSS)}$$

$$Z = \bar{Q}_0 \bar{Q}_1 \bar{Q}_2 \bar{Q}_3$$

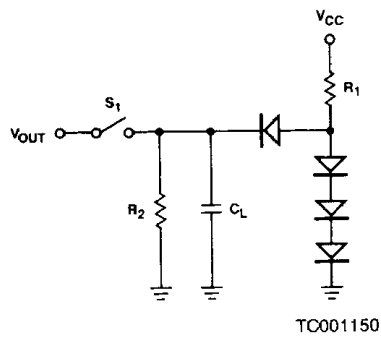
$$OVR = Q_2 \oplus Q_1 \text{ (MSS)}$$

SWITCHING TEST CIRCUITS



A. Three-State Outputs

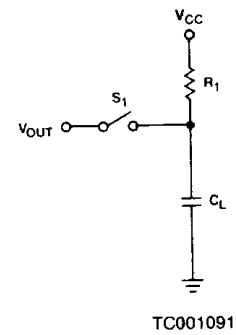
$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$



B. Normal Outputs

$$R_2 = \frac{2.4 V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$



C. Open-Collector Outputs

$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

- Notes: 1. $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in hand in test fixture.
 2. S_1, S_2, S_3 are closed during function tests and all A.C. tests except output enable tests.
 3. S_1 and S_3 are closed while S_2 is open for t_{pZH} test.
 S_1 and S_2 are closed while S_3 is open for t_{pZL} test.
 4. $C_L = 5.0$ pF for output disable tests.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

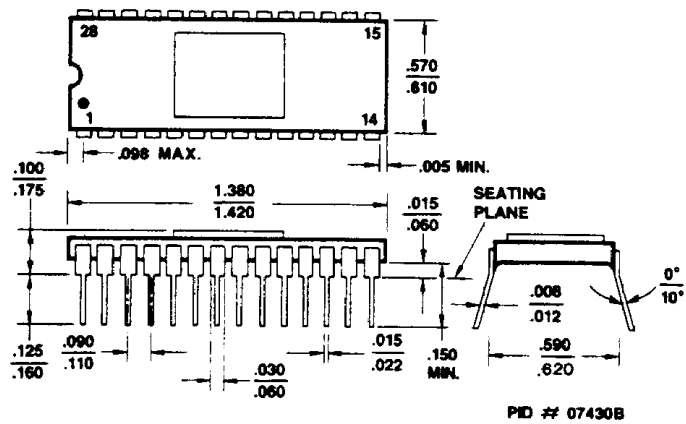
KS000010

TEST OUTPUT LOADS		
Test Circuit	$R_1 (\Omega)$	$R_2 (k\Omega)$
A	470	1
A	Y_0-3	240
B	C_n+4	470
B	\bar{P}/OVR	390
B	\bar{G}/N	220
C	270	-

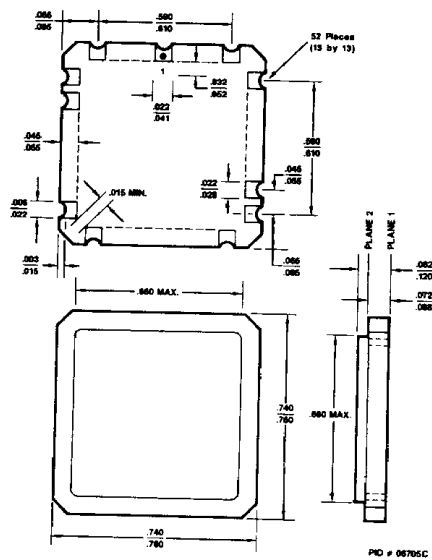
For additional information on testing, see section, "Guidelines on Testing Am2900 Family Devices," in the 1985 BMLI databook, p. 13-2.

PHYSICAL DIMENSIONS (Cont'd.)

SD 028



CL 052



CFT048

Technical drawing of a mechanical part, likely a valve or actuator, showing two views: a top view and a side view.

Top View Dimensions:

- Overall width: 1.185
- Overall height: 1.235
- Top right corner: .045 MAX.
- Right side (top to bottom): .017/.023, .045/.065, .005 MIN.
- Bottom (left to right): .620, .860, 1.140, 1.380
- Bottom right corner: 250, .370

Side View Dimensions:

- Left side (top to bottom): .030 MIN., .008/.012
- Center (left to right): .680 MAX., .520 MIN.
- Right side (top to bottom): .030 MIN., .070/.098, .030/.060

Part Labels: 1, 48, 24, 25

PID # 07869A