

AM29520A, AM29521A

Multilevel Pipeline Registers

The AM29520A and AM29521A are high speed, dual stack, register files that differ only in the way data is loaded. Both devices contain four 8-bit wide registers whose flexible architecture lends itself to virtually any system. The high output drive allows layout of the devices directly on the system bus for bit slice and array or digital signal processing applications.

In the AM29520A, data may be microprogrammed to cascade through the 4 registers in push-down pattern, no-op to hold data in the registers, or push-down data through one 2 level stack while holding data in the other stack. The AM29521A also has the cascadable 4 registers push-down and no-op features. It can also be microprogrammed to write over the first level register of one stack, while holding data in the other 3 registers.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29520A/Am29521A

Multilevel Pipeline Registers



DISTINCTIVE CHARACTERISTICS

- Four 8-bit wide registers
- Provides temporary storage for data/instruction delay/queuing
- Single 4 level or dual 2 level structure
- High-speed IMOX™ ECL internal technology, TTL compatible I/O
- All 4 registers available at three state output
- 24 pin slim (0.3") DIP packages
- 28 pin chip carrier packages

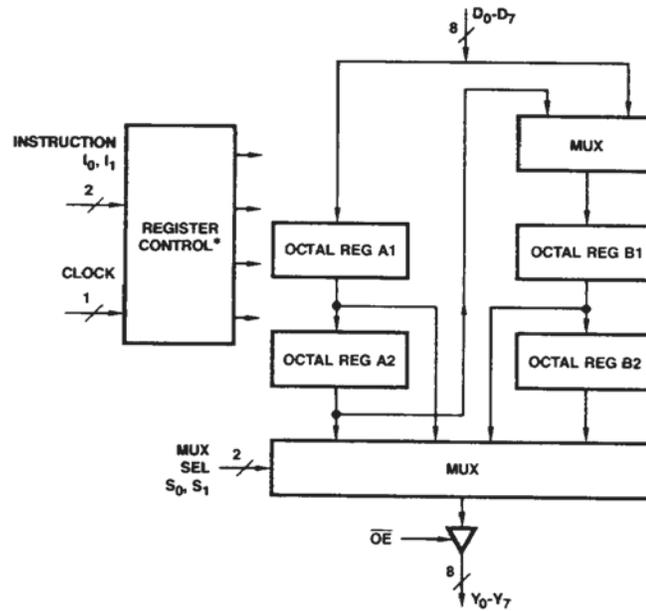
GENERAL DESCRIPTION

The Am29520A and Am29521A are high speed, dual stack, register files that differ only in the way data is loaded (see Table 1). Both devices contain four 8-bit wide registers whose flexible architecture lends itself to virtually any system. The high output drive allows layout of the devices directly on the system bus for bit slice and array or digital signal processing applications.

In the Am29520A, data may be microprogrammed to cascade through the 4 registers in push-down pattern, no-op to hold data in the registers, or push-down data through one 2 level stack while holding data in the other stack.

The Am29521A also has the cascadable 4 register push-down and no-op features. It can also be microprogrammed to write over the first level register of one stack, while holding data in the other 3 registers.

BLOCK DIAGRAM



BDR02270

*Multilevel Pipeline Register

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Publication #	Rev.	Amendment
03569	B	/0
Issue Date: September 1986		

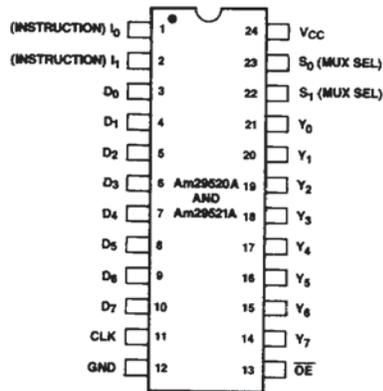
ADVANCED MICRO DEVICES

RELATED PRODUCTS

Part No.	Description
Am29540	FFT Address Sequencer
Am29116	16-bit Bipolar Microprocessor
Am29325	32-bit Floating Point Processor
Am29517A	16 x 16-bit Multiplier
Am29501	8-bit Multi-Port Pipeline Microprocessor
Am29C509	12 x 12 MAC
Am6108	8-bit A/D Converter
Am9128	2K x 8 Static RAM
Am21L47	4K x 1 Static RAM
Am29524	Dual 7 Deep Pipeline Register with 0 and Feedthrough

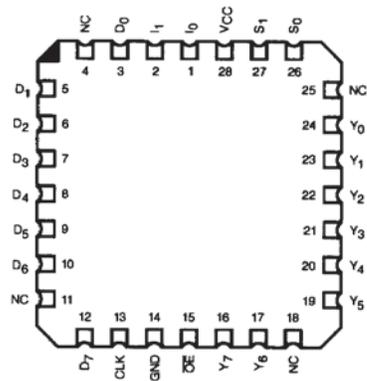
CONNECTION DIAGRAM Top View

CD3024
PD3024



CDR04471

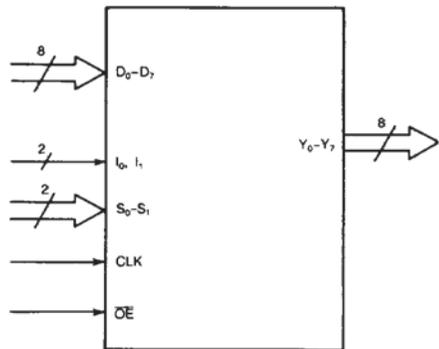
CL 028
PL 028



CD010120

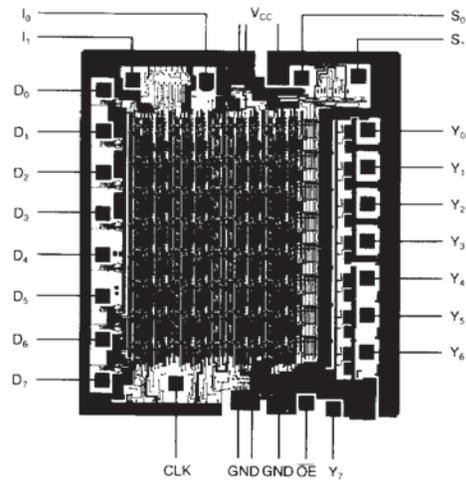
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002301

METALLIZATION AND PAD LAYOUT



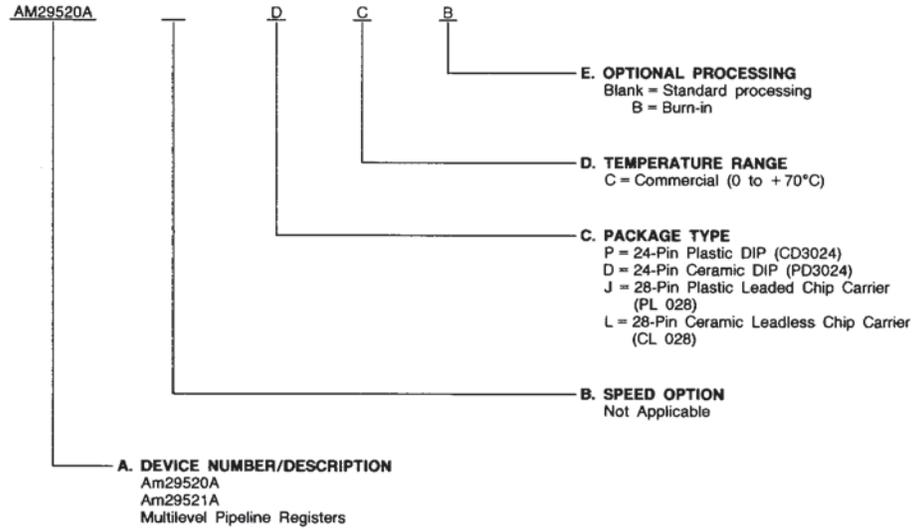
DIE SIZE: 0.117" x 0.133"
Approximate Gate Count = 362

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations	
AM29520A	DC, DCB, PC, PCB, LC, JC
AM29521A	DC, DCB, PC, PCB, LC, JC

Valid Combinations

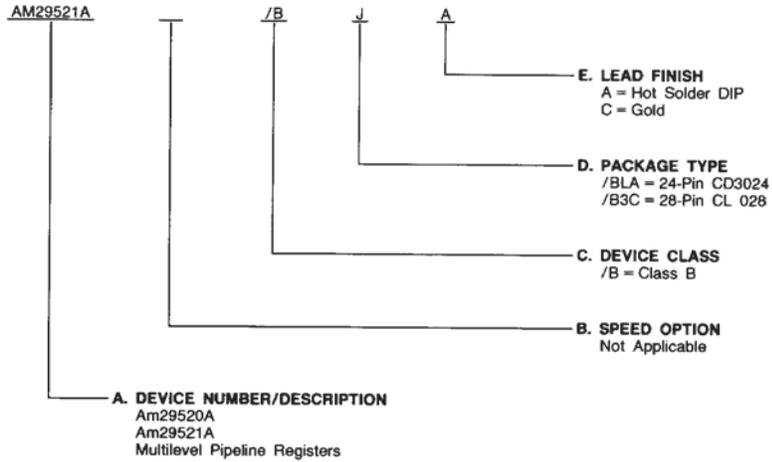
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Device Class**
- D. Package Type**
- E. Lead Finish**



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Valid Combinations	
AM29520A	BLA, B3C
AM29521A	BLA, B3C

PIN DESCRIPTION

D₀ - D₇ Register Input Port (Input, Active HIGH)

Data to be written to the internal registers is input via this port.

Y₀ - Y₇ Register Output Port (Output, Three-State)

Data to be read out of any of the internal registers is output via this three-state port.

I₀, I₁ Instruction Inputs (Input, Active HIGH)

Operational control of the device is determined by these inputs. See Tables 1 and 2 for details.

S₀, S₁ Register Output Select (Input, Active HIGH)

These inputs select which register appears on the Register Output Port. See Table 3 for details.

CLK Clock (Input)

The rising edge of the clock loads data into the appropriate registers as determined by the Instruction Inputs.

\overline{OE} Output Enable (Input, Active LOW)

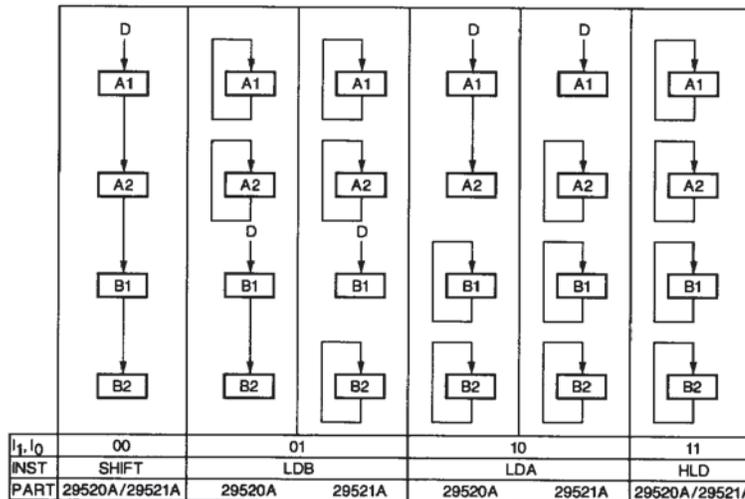
When LOW, the register selected by the Register Output Select Inputs appears on the Register Output Port. When HIGH, the Register Output Port is three-stated.

FUNCTIONAL DESCRIPTION

The following tables describe the operation of the Am29520A/29521A. Table 1 illustrates register operation in response to instruction inputs I₀ and I₁. Note that in the Am29521A, instructions "LDB" and "LDA" write over register B₁ or A₁

respectively, and hold resident data in the other 3 registers. The Am29520A instead pushes data down the two level stack. Table 2 gives the operand values corresponding to the operations illustrated in Table 1. Table 3 gives the Register Output Select codes required to access a specific register, which then appears at the Register Output Port.

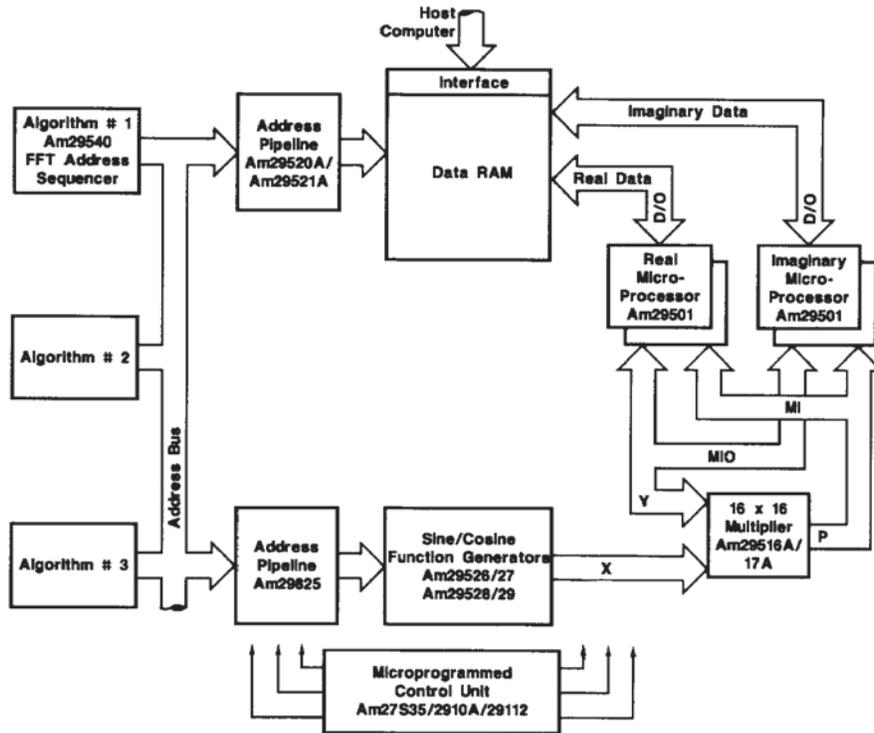
Am29520A/29521A INSTRUCTIONS



TB000240

TABLE 1. REGISTER LOAD OPERATIONS
(See Table 2 for instruction codes)

Am29500 PROCESSOR



BD002712

Mnemonic	Inputs		Description	
	I ₁	I ₀	Am29520A Only	Am29521A Only
Shift	0	0	Push A & B	Push A & B
LDB	0	1	Push B	Write Over B ₁
LDA	1	0	Push A	Write Over A ₁
HLD	1	1	No-Op	No-Op

TABLE 2. INSTRUCTION SET DESCRIPTIONS

S0	S1	Y0 - Y7
1	1	A ₁
1	0	A ₂
0	1	B ₁
0	0	B ₂

TABLE 3. SELECT OPERATION DESCRIPTIONS &vc<2>

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Temperature Under Bias- T_C -55 to +125°C
 Supply Voltage to Ground Potential
 Continuous -0.5 to +7.0V
 DC Voltage Applied to Outputs For
 High Output State -0.5V to + V_{CC} max
 DC Input Voltage -0.5 to +5.5V
 DC Output Current, Into Outputs 30mA
 DC Input Current -30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature $T_A = 0^\circ\text{C}$ to +70°C
 Supply Voltage +4.75 V to +5.25 V

Military (M) Devices

Temperature $T_C = -55^\circ\text{C}$ to +125°C
 Supply Voltage +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

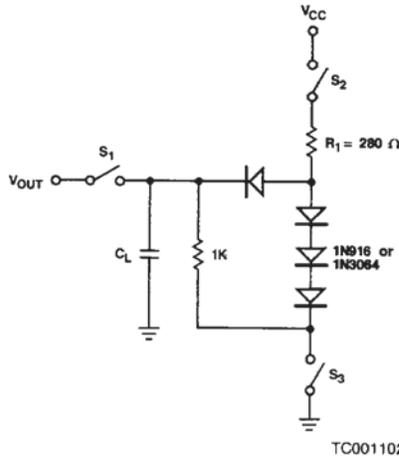
Parameters	Description	Test Conditions (Note 1)		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{MIN}$	$I_{OH} = -6.5 \text{ mA (COM'L)}$	2.4		Volts
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -2.0 \text{ mA (MIL)}$	2.4		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{MIN}$	$I_{OL} = 12 \text{ mA}$		0.45	Volts
		$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \text{ mA}$		0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0		Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V_I	Input Clamp Voltage	$V_{CC} = \text{MIN}, I_{IN} = -18 \text{ mA}$			-1.2	Volts
I_{IL}	Input LOW Current	$V_{CC} = \text{MAX}, V_{IN} = 0.5 \text{ V}$	OE		-2.0	mA
			Other Inputs		-0.4	
I_{IH}	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 2.7 \text{ V}$			50	μA
I_I	Input HIGH Current	$V_{CC} = \text{MAX}, V_{IN} = 5.5 \text{ V}$			1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	$V_{CC} = \text{MAX}$	$V_O = 2.7 \text{ V}$		50	μA
			$V_O = 0.5 \text{ V}$		-50	
I_{SC}	Output Short Circuit Current (Note 2)	$V_{CC} = \text{MAX}$		-30	-100	mA
I_{CC}	Power Supply Current (Note 3)	COM'L Only	$T_A = 0$ to +70°C		185	mA
		$V_{CC} = \text{MAX}$	$T_A = +70^\circ\text{C}$		155	
		MIL Only	$T_C = -55$ to +125°C		200	
		$V_{CC} = \text{MAX}$	$T_C = +125^\circ\text{C}$		150	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Ranges for the applicable device type.
 2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 3. All inputs LOW.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Parameters Symbols	Parameter Description	Test Conditions	COMMERCIAL		MILITARY		Units
				Min.	Max.	Min.	Max.	
1	t_{PD}	t_{PLH}	Clock to Data Output		21		24	ns
		t_{PHL}			22		24	
2	t_{PDSEL}	t_{PLH}	S_0, S_1 to Data Output		20		22	ns
		t_{PHL}			20		22	
3	t_S	Input Data to Clock	$R_L = 280\Omega$ $C_L = 50pF$	10		10		ns
4	t_H			3		3		
5	t_S			10		10		
6	t_H	Instruction (Register Enable) to Clock		3		3		ns
7	t_{PHZ}	\overline{OE} to Output	$C_L = 5 pF$		13		14	ns
8	t_{PLZ}	\overline{OE} to Output	$C_L = 5 pF$		15		16	ns
9	t_{PZH}	\overline{OE} to Output	$R_L = 280 \Omega$ $C_L = 50 pF$		20		22	ns
10	t_{PZL}	\overline{OE} to Output			21		22	ns
11	t_{PWH}	Clock Pulse Width HIGH		10		10		ns
12	t_{PWL}	Clock Pulse Width LOW	10		10		ns	

SWITCHING TEST CIRCUITS

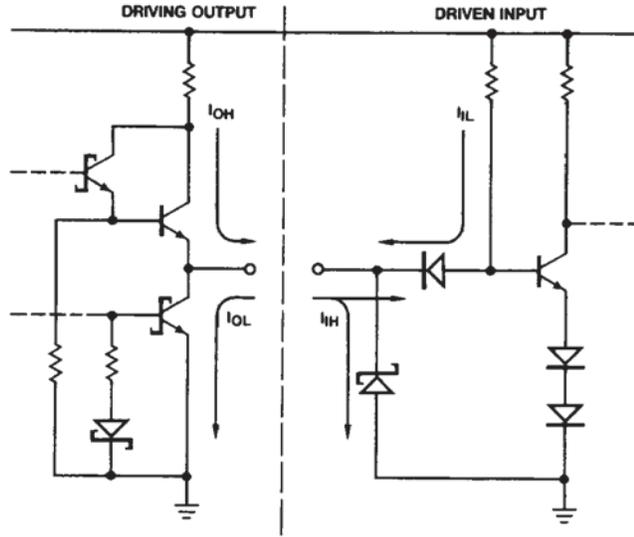


TC001102

Three-State Outputs

- Notes: 1. $C_L = 50 pF$ includes scope probe, wiring and stray capacitances without device in test fixture.
- 2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
- 3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
 S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
- 4. $C_L = 5.0 pF$ for output disable tests.

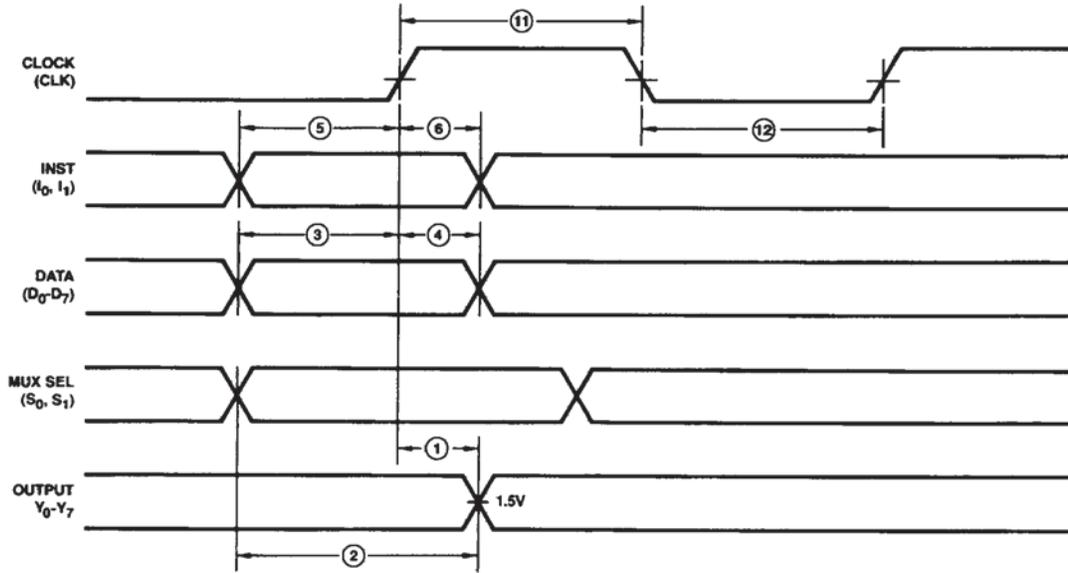
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



ICR00510

SWITCHING WAVEFORMS

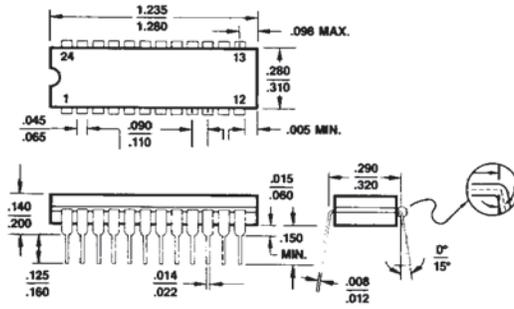
Am29520A/Am29521A



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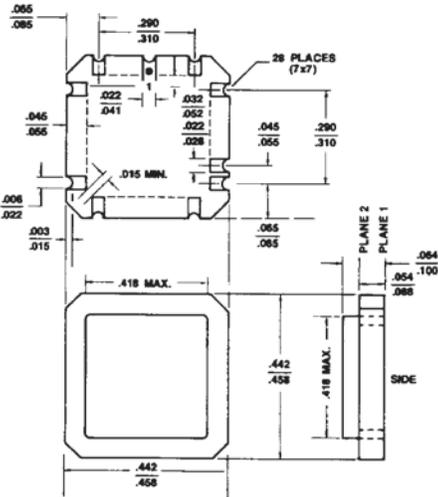
PHYSICAL DIMENSIONS*

CD3024



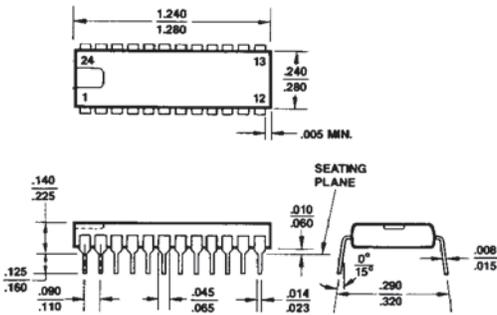
PID # 068508

CL 028



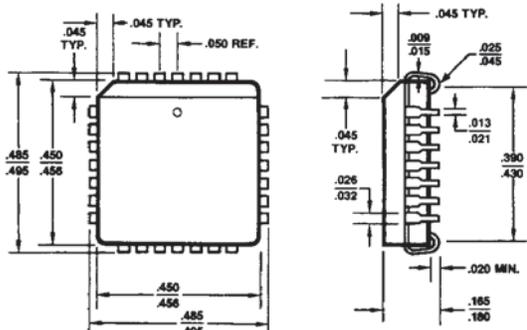
PID # 06596D

PD3024



PID # 07689B

PL 028



PID # 06751D

*For Reference Only

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