

AM29C116, AM29C116-1, AM29C116-2

16-Bit CMOS Microprocessors

The AM29C116 is a microprogrammable 16-bit CMOS microprocessor whose architecture and instruction set is optimized for high-performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applications, especially when combined with the AM29C517A, 16 x 16 Multiplier. In addition to its complete arithmetic and logic instruction set, the AM29C116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate-and-merge, rotate-and-compare, and cyclic-redundancy-check (CRC) generation.

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Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am29C116/116-1/116-2



16-Bit CMOS Microprocessors

DISTINCTIVE CHARACTERISTICS

Am29C116

Supports up to 100-ns system cycle time. Less than 1-watt power dissipation and equivalent performance to the bipolar Am29116.

- Am29C116-1
- Faster, speed-select version of the Am29C116 (90 ns).
- Am29C116-2
- Can operate with 80-ns clock cycle.
- Pin-Compatible and Functionally Equivalent to the Am29116

The architecture, instruction set, and pin-out are completely identical to the bipolar Am29116.

- Optimized for High-Performance Controllers
- The architecture is optimized for controllers providing an excellent solution for applications requiring bit-manipulation power.
- Powerful Field Insertion/Extraction and Bit-Manipulation Instructions

Rotate-and-Merge, Rotate-and-Compare and bitmanipulation instructions provided for complex bit control.

- Immediate Instruction Capability
 May be used for storing constants in microcode or for configuring a second data port.
- 16-Bit Barrel Shifter
- 32-Working Registers

GENERAL DESCRIPTION

The Am29C116 is a microprogrammable 16-bit CMOS microprocessor whose architecture and instruction set is optimized for high-performance peripheral controllers, like graphics controllers, disk controllers, communications controllers, front-end concentrators and modems. The device also performs well in microprogrammed processor applica-

tions, especially when combined with the Am29C517A, 16×16 Multiplier. In addition to its complete arithmetic and logic instruction set, the Am29C116 instruction set contains functions particularly useful in controller applications; bit set, bit reset, bit test, rotate-and-merge, rotate-and-compare, and cyclic-redundancy-check (CRC) generation.

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Am29C116/116-1/116-2

Advanced Micro Devices

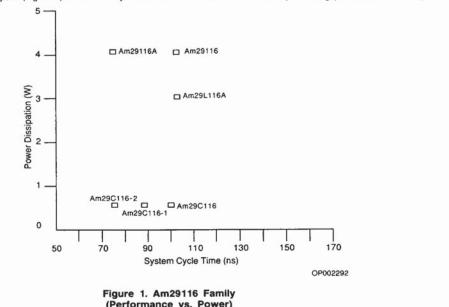
Part No.	Description
Am29C10A	CMOS 12-Bit Sequencer
Am29C111	CMOS 16-Bit Microsequencer
Am29114	8-Level Real-Time Interrupt Controller
Am29117	2-Port 16-Bit Microprocessor
Am29C117	CMOS Version of Am29117
Am29118	8-Bit Am29C116 I/O Support
Am29130	16-Bit Barrel Shifter
m29PL131	64 x 32 Field-Programmable Controller
Am29PL141	64 x 32 Field-Programmable Controller
m29CPL141	CMOS Version of Am29PL141
Am29PL142	128 x 32 Field-Programmable Controller
m29CPL144	CMOS 512 x 32 Field-Programmable Controller
Am29C331	CMOS 16-Bit Microsequencer



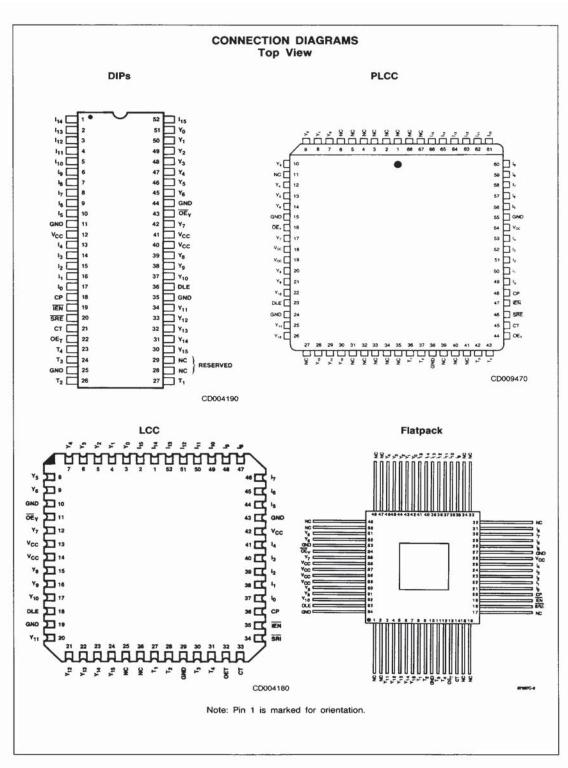
CMOS 16 x 16 Multiplier CMOS 2-Port 16 x 16 Multiplier

Am29C516A

Am29C517A

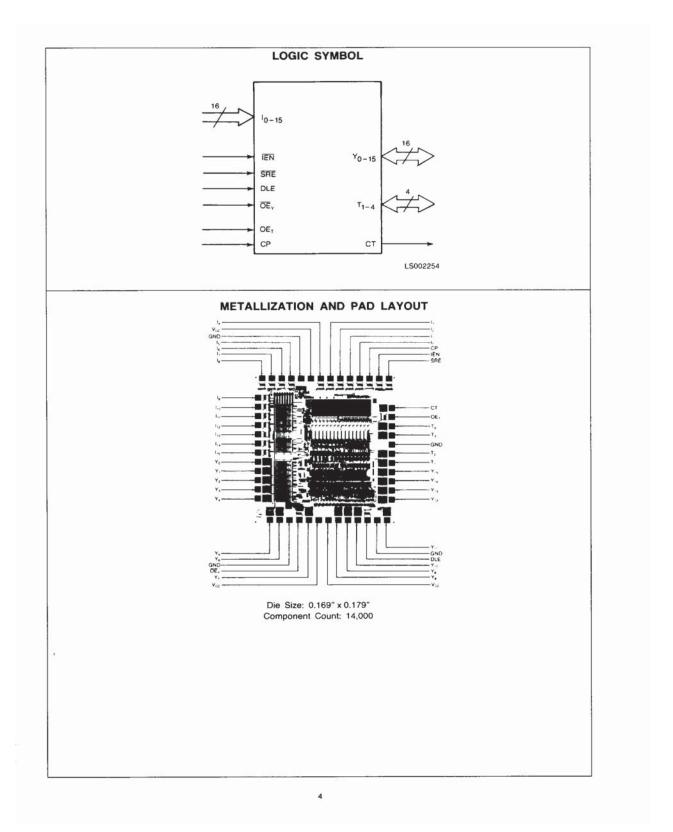


(Performance vs. Power)

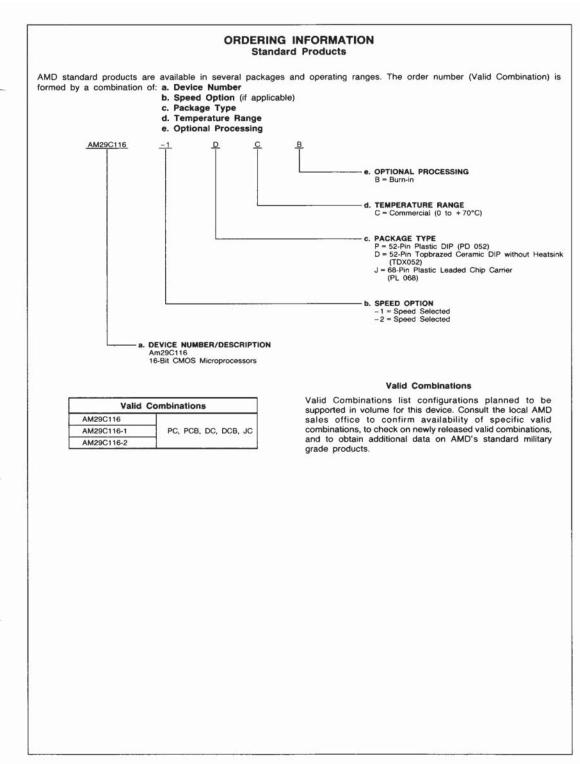


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PIN DESCRIPTION

CP Clock Pulse (Input)

The clock input to the Am29C116. The RAM latch is transparent when the clock is HIGH. When the clock goes LOW, the RAM output is latched. Data is written into the RAM during the low period of the clock provided IEN is LOW and if the instruction being executed designates the RAM as the destination of operation. The Accumulator and Status Register will accept data on the LOW-HIGH transition of the clock if IEN is also LOW. The instruction latch becomes transparent when it exits an immediate instruction mode during a LOW-HIGH transition of the clock.

Conditional Test (Output)

The condition code multiplexer selects one of the twelve condition code signals and places them on the CT output. A HIGH on the CT output indicates a passed condition and a LOW indicates a failed condition.

Data Latch Enable (Input)

When DLE is HIGH, the 16-bit data latch is transparent and is latched when DLE is LOW.

Instruction Enable (Input)

With IEN LOW, data can be written into the RAM when the clock is LOW. The Accumulator can accept data during the LOW-HIGH transition of the clock. Having IEN LOW, the Status Register can be updated when SRE is LOW. With IEN HIGH, the conditional test output, CT, is disabled as a function of the instruction inputs. IEN should be LOW for the first half of the first cycle of an immediate instruction.

I₀-I₁₅ Instruction Inputs -- 16 (Input)

Used to select the operations to be performed in the Am29C116. Also used as data inputs while performing immediate instructions.

OE_T Output Enable (Input)

When OET is LOW, the 4-bit T outputs are disabled (highimpedance); when OET is HIGH, the 4-bit T outputs are enabled (HIGH or LOW).

Output Enable (Input)

When OEY is HIGH, the 16-bit Y outputs are disabled (highimpedance); when OEy is LOW, the 16-bit Y outputs are enabled (HIGH or LOW).

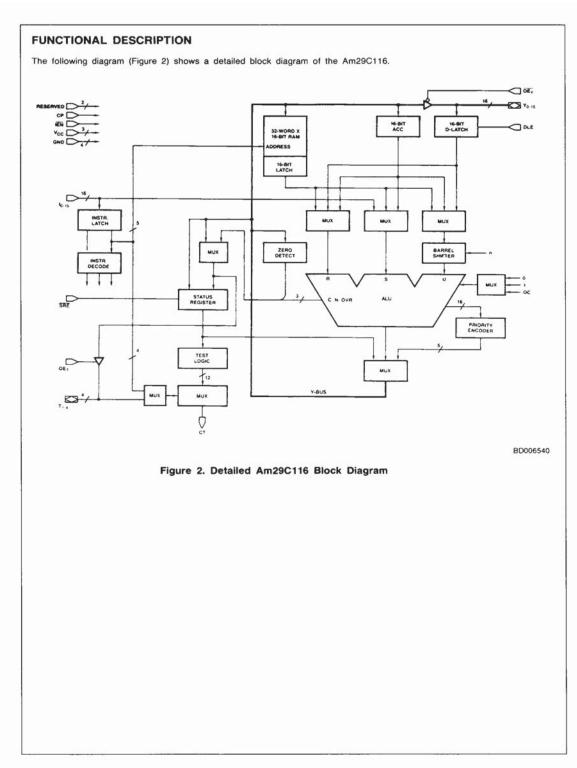
SRE Status Register Enable (Input)

When SRE and IEN are both LOW, the Status Register is updated at the end of all instructions with the exception of NO-OP, Save Status, and Test Status. Having either SRE or IEN HIGH will inhibit the Status Register from changing.

T₁-T₄ Input/Output Pins — 4 (Input/Output)

Under the control of OET, the four lower status bits Z, C, N, OVR, become outputs on T_1 - T_4 , respectively, when OE_T goes HIGH. When OE_T is LOW, T_1 - T_4 are used as inputs to generate the CT output.

Y₀ - Y₁₅ Data I/O Lines — 16 (Input/Output)
When \overrightarrow{OE}_Y is HIGH, Y₀-Y₁₅ are used as external data inputs which allow data to be directly loaded into the 16-bit data latch. Having OEy LOW allows the ALU data to be output on



Architecture of the Am29C116

The Am29C116 is a high-performance, microprogrammable 16-bit CMOS microprocessor.

As shown in the Block Diagrams, the device consists of the following elements interconnected with 16-bit data paths.

- 32-Word by 16-Bit RAM
- Accumulator
- Data Latch
- Barrel Shifter
- ALU
- Priority Encoder
- Status Register
- Condition-Code Generator/Multiplexer
- Three-State Output Buffers
- Instruction Latch and Decoder

32-Word by 16-Bit RAM

The 32-Word by 16-Bit RAM is a single-port RAM with a 16-bit latch at its output. The latches are transparent when the clock input (CP) is HIGH and latched when the clock input is LOW. Data is written into the RAM while the clock is LOW if the IET input is also LOW and if the instruction being executed defines the RAM as the destination of the operation. For byte instructions, only the lower eight RAM bits are written into; for word instructions, all 16 bits are written into. With the use of an external multiplexer on five of the instruction inputs, it is possible to select separate read and write addresses for the same instruction. This two-address operation is not allowed for immediate instructions.

Accumulator

The 16-bit Accumulator is an edge-triggered register. The Accumulator accepts data on the LOW-to-HIGH transition of the clock input if the IEN input is LOW and if the instruction being executed defines the Accumulator as the destination of the operation. For byte instructions, only the lower eight bits of the Accumulator are written into; for word instructions, all 16 bits are written into.

Data Latch

The 16-bit Data Latch holds the data input to the Am29C116 on the bi-directional Y bus. The latch is transparent when the DLE input is HIGH and latched when the DLE input is LOW.

Barrel Shifter

A 16-bit Barrel Shifter is used as one of the ALU inputs. This permits rotating data from either the RAM, the Accumulator or the Data Latch up to 15 positions. In the word mode, the Barrel Shifter rotates a 16-bit word; in the byte mode, it rotates only the lower eight bits.

Arithmetic Logic Unit

The Am29C116 contains a 16-bit ALU with full carry lookahead across all 16 bits in the arithmetic mode. The ALU is capable of operating on either one, two or three operands, depending upon the instruction being executed. It has the ability to execute all conventional one and two operand operations, such as pass, complement, two's complement, add, subtract, AND, NAND, OR, NOR, EXOR, and EX-NOR. In addition, the ALU can also execute three-operand instructions such as rotate and merge and rotate and compare with mask. All ALU operations can be performed on either a word or byte basis, byte operations being performed on the lower eight bits only.

The ALU produces three status outputs, C (carry), N (negative) and OVR (overflow). The appropriate flags are generated at the byte or word level, depending upon whether the device is executing in the byte or word mode. The Z (zero) flag,

although not generated by the ALU, detects zero at both the byte and word level.

The carry input to the ALU is generated by the Carry Multiplexer which can select an input of zero, one, or the stored carry bit from the Status Register, QC. Using QC as the carry input allows execution of multiprecision addition and subtractions.

Priority Encoder

The Priority Encoder produces a binary-weighted code to indicate the locations of the highest order ONE at its input. The input to the Priority Encoder is generated by the ALU which performs an AND operation on the operand to be prioritized and a mask. The mask determines which bit locations to eliminate from prioritization. In the word mode, if no bit is HIGH, the output is a binary zero. If bit 15 is HIGH, the output is a binary one. Bit 14 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 16 is produced.

In the byte mode, bits 8 thru 15 do not participate. If none of bits 7 thru 0 are HIGH, the output is a binary zero. If bit 7 is HIGH a binary one is produced. Bit 6 produces a binary two, etc. Finally, if only bit 0 is HIGH, a binary 8 is produced.

Status Register

The Status Register holds the 8-bit status word. With the Status-Register Enable, (SRE) input LOW and the IEN input LOW, the Status Register is updated at the end of all instructions except NO-OP, Save-Status and Test-Status instructions. SRE going HIGH or IEN going HIGH inhibits the Status Register from changing.

The lower four bits of the Status Register contain the ALU status bits of Zero (Z), Carry (C), Negative (N), and Overflow (OVR). The upper four bits contain a Link bit and three user-definable status bits (Flag 1, Flag 2, Flag 3).

With SRE LOW and IEN LOW, the lower four status bits are updated after each instruction except those mentioned above, NO-OP, Save Status, Status Test and the Status Set/Reset instruction for the upper four bits. Under the same conditions, the upper four status bits are changed only during their respective Status Set/Reset instructions and during Status Load instructions in the word mode. The Link-Status bit is also updated after each shift instruction.

The Status Register can be loaded from the internal Y-bus, and can also be selected as a source for the internal Y-bus. When the Status Register is loaded in the word mode, all 8-bits are updated; in the byte mode, only the lower 4 bits (Z, C, N, OVR) are updated.

When the Status Register is selected as a source in the word mode, all eight bits are loaded into the lower byte of the destination; the upper byte of the destination is loaded with all zeros. In the byte mode, the Status Register again loads into the lower byte of the destination, but the upper byte remains unchanged. This Store and Load combination allows saving and restoring the Status Register for interrupt and subroutine processing. The four lower status bits (Z, C, N, OVR) can be read directly via the bidirectional T bus. These four bits are available as outputs on the T_{1-4} outputs whenever $OE_{\rm T}$ is $\rm LICLI$

Condition-Code Generator/Multiplexer

The Condition-Code Generator/Multiplexer contains the logic necessary to develop the 12 condition-code test signals. The multiplexer portion can select one of these test signals and place it on the CT output for use by the microprogram sequence. The multiplexer may be addressed in two different ways. One way is through the Test Instruction. This instruction specifies the test condition to be placed in the CT output, but

does not allow an ALU operation at the same time. The second method uses the bidirectional T bus as an input. This requires extra bits in the microword, but provides the ability to simultaneously test and execute. The test instruction lines, I₀₋₄, have priority over T₁₋₄, for testing status.

Three-State Output Buffers

There are two sets of Three-State Output Buffers in the Am29C116. One set controls the bidirectional, 16-bit Y bus. These outputs are enabled by placing a LOW on the OE input. A HIGH puts the Y outputs in the high-impedance state, allowing data to be input to the Data latch from an external source.

The second set of Three-State Output Buffers controls the bidirectional 4-bit T bus and is enabled by placing a HIGH on the OE_T input. This allows storing the four internal ALU status bits (Z, C, N, OVR) externally. A LOW OE_T input forces the T outputs into the high-impedance state. External devices can

then drive the T bus to select a test condition for the CT output.

Instruction Latch and Decoder

The 16-bit Instruction Latch is normally transparent to allow decoding of the Instruction Inputs by the Instruction Decoder into the internal control signals for the Am29C116. All instructions except Immediate Instructions are executed in a single clock cycle.

Immediate instructions require two clock cycles for execution. During the first clock cycle, the Instruction Decoder recognizes that an Immediate Instruction is being specified and captures the data on the Instruction Inputs in the Instruction Latch. During the second clock cycle, the data on the Instruction Inputs is used as one of the operands for the function specified during the first clock cycle. At the end of the second clock cycle, the Instruction Latch is returned to its transparent

Instruction Set

The instruction set of the Am29C116 is very powerful. In addition to the single and two operand logical and arithmetic instructions, the Am29C116 instruction set contains functions particularly useful in controller applications: bit set, bit reset, bit test, rotate and merge, rotate and compare, and cyclicredundancy-check (CRC) generation. Complex instructions like rotate and merge, rotate and compare, and prioritize are executed in a single microcycle.

Three data types are supported by the Am29C116.

- Bit
- Byte
- Word (16-bit)

In the byte mode, data is written into the lower half of the word and the upper half is unchanged. The special case is when the status register is specified as the destination. In the byte mode, the LSH (OVR, N, C, Z) of the status register is updated and in the word mode all eight bits of the status register are updated. The status register does not change for save status and test status instructions. In the test status instructions, the CT output has the result and the Y-bus is undefined.

The Am29C116 Instruction Set can be divided into eleven types of instructions. These are:

- Single Operand
- Two Operand
- · Single Bit Shift Rotate and Merge
- Bit Oriented
- Rotate by n Bits
- Rotate and Compare
- Prioritize
- Cyclic-Redundancy-Check
- Status
- No-Op

Each instruction type is arbitrarily divided into quadrants. Two of the sixteen instruction lines decode to four quadrants labelled from 0 to 3. The guadrants were defined mainly for convenience in classification of the instruction set and addressing modes and can be used together with the OP CODES to distinguish the instructions.

The following pages describe each of the instruction types in detail. Throughout the description OEy is assumed to be LOW allowing ALU outputs on the Y-bus.

Table 1 illustrates operand source-destination combinations for each instruction type.

TABLE 1. OPERAND SOURCE DESTINATION COMBINATIONS

Instruction Type	Operand	Combinati	ons (Note 1)			
- 553	Source	(R/S)	Destination			
Single Operand	A(Note 2) CC C DE) SE)	RAM ACC Y Bus Status ACC and Status			
	Source (R)	Source (S)	Destination			
Two Operand	RAM RAM D D ACC D	ACC I RAM ACC I	RAM ACC Y Bus Status ACC and Status			
	Source	e (U)	Destination			
Single Bit Shift	AC AC	RAM ACC ACC D D				
2000-2000	Source	e (U)	Destination			
Rotate n Bits	AC	AM CC C	RAM ACC Y Bus			
	Source	(R/S)	Destination			
Bit Oriented	AC	AM CC C	RAM ACC Y Bus			
397/23	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R)			
Rotate and Merge	D D D D ACC BAM	RAM ACC 	ACC ACC RAM RAM RAM ACC			

Instruction Type	Operand	d Combination	ons (Note 1)					
	Rotated Source (U)	Mask (S)	Non-Rotated Source/ Destination (R					
Rotate and Compare	D D D RAM	ACC	RAM RAM ACC					
	Source (R)	Mask (S)	Destination					
Prioritize (Note 3)	RAM ACC D	RAM ACC I 0	RAM ACC Y Bus					
Cyclic	Data In	Destination	Polynomial					
Redundancy Check	QLINK	RAM	ACC					
No Operation								
	Bits Affected							
Set Reset Status	OVR, N, C, Z LINK Flag1 Flag2 Flag3							
	Sou	ırce	Destination					
Store Status	Sta	atus	RAM ACC Y Bus					
	Source (R)	Source (S)	Destination					
Status Load	D ACC	ACC I	Status Status and ACC					
	D	1						
	Te	est Conditio	n (CT)					
		(N⊕OVR) N⊕OVE Z OVR						
Test Status		Low C Z + C						
	N LINK Flag 1 Flag 2							
		Flag 3						

Notes: 1. When there is no dividing line between the R&S OPERAND or SOURCE and DESTINATION, the two must be used as a given pair. But where there exists such a separation, any combination of

them is possible.

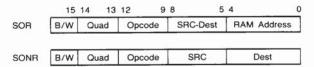
2. In the SINGLE OPERAND INSTRUCTION, RAM cannot be used when both ACC and STATUS are designated as a DESTINATION.

3. In the PRIORITIZE INSTRUCTION, OPERAND and MASK must be different sources.

SINGLE OPERAND INSTRUCTIONS

The Single Operand Instructions contain four indicators: byte or word mode, opcode, source and destination. They are further subdivided into two types. The first type uses RAM as a source or destination or both, and the second type does not use RAM as a source or destination. Both types have different instruction formats as shown below. Under the control of instruction inputs, the desired function is performed on the source and the result is either stored in the specified destination or placed on the Y-bus or both. For a special case where 8-bit to 16-bit conversion is needed, the Am29C116 is capable of extending sign bit (D(SE)) or binary zero (D(0E)) over 16-bits in the word mode. The least significant four bits of the Status Register (OVR, N, C, Z) are affected by the function performed in this category. The most significant bits of status register (FLAG1, FLAG2, FLAG3, LINK) are not affected. The only limitation in this type is that the RAM cannot be used as a source when both ACC and the Status Register are specified as a destination.

SINGLE OPERAND FIELD DEFINITIONS



SINGLE OPERAND INSTRUCTION

Instruction ¹	B/W ²	Quad ³		Opc	ode		9940	R/S4	Dest ⁴		RAM A	ddress
SOR	0 = B 1 = W	10	1100 1101 1110 1111	MOVE COMP INC NEG	SRC Dest SRC Dest SRC + 1 Dest SRC + 1 Dest	0000 0010 0011 0100 0110 0111 1000 1001 1011	SORA SORY SORS SOAR SODR SOIR SOZR SOZER SOSER SORR		ACC Y Bus Status RAM RAM RAM RAM RAM	00000	R00 R31	RAM Reg 00 RAM Reg 31
Instruction	B/W	Quad	1	Opc	ode		100000	R/S4			Desti	nation
SONR	0 = B 1 = W	11	1100 1101 1110 1111	MOVE COMP INC NEG	SRC Dest SRC Dest SRC + 1 Dest SRC + 1 Dest	0100 0110 0111 1000 1001 1010	SOA SOD SOI SOZ SOZE SOSE	D I O D(0E) D(SE)	С	00000 00001 00100 00101	NRY NRA NRS NRAS	Y Bus ACC Status ⁵ ACC, Status ⁵

1. The instruction mnemonic designates different instruction formats used in the Am29C116. They are useful in microcode assembly.

2. B = Byte Mode, W = Word Mode.

3. See Instruction Set description.

4. R = Source; S = Source; Dest = Destination.

5. When status is destination,

Status i = Yi = 0 to 3 (Byte mode)

i = 0 to 7 (Word mode)

Y BUS AND STATUS - SINGLE OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	Z
SOR	MOVE	SRC → Dest	0 = B	Y - SRC	NC	NC	NC	NC	0	U	0	U
SONR	COMP	SRC → Dest	1 = W	Y - SRC	NC	NC	NC	NC	0	U	0	U
	INC	SRC +1 - Dest	7	Y SRC +1	NC	NC	NC	NC	U	U	U	U
	NEG	SRC +1 → Dest		Y SRC +1	NC	NC	NC	NC	U	υ	U	U

SRC = Source U = Update NC = No Change

0 = Reset

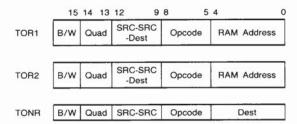
i = 0 to 15 when not specified

TWO OPERAND INSTRUCTIONS

The Two Operand Instructions contain five indicators: byte or word mode, opcode, R source, S source, and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. The first type has two formats; the only difference is in the quadrant. Under the control of instruction inputs, the desired function is performed on the specified sources and the result is stored in the

specified destination or placed on the Y-bus or both. The least significant four bits of the status register (OVR, N, C, Z) are affected by the arithmetic functions performed and only the N and Z bits are affected by the logical functions performed. The OVR and C bits of the status register are forced to ZERO for logical functions. Add with carry and Subtract with carry instructions are useful for Multiprecision Add or Subtract.

TWO OPERAND FIELD DEFINITIONS



TWO OPERAND INSTRUCTIONS

Instruction	B/W	Quad			R ¹	S ¹	Dest ¹		Opcode	е		RAM	Addre	ess
TOR1	0 = B 1 = W	00	0000 0010 0011 1000 1010 1011 11100 11110	TORAA TORIA TODRA TORAY TORIY TODRY TORAR TORIR TODRR	RAM RAM D RAM RAM D RAM D RAM D	ACC I RAM ACC I RAM ACC I RAM	ACC ACC ACC Y Bus Y Bus Y Bus RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010	SUBSC ² R SUBS R SUBSC ² R ADD R ADDC R AND R NAND R NAND R NOR R	minus R minus R minus R ithicarry i minus S i	11111	R00 R31		Reg 31
Instruction	B/W	Quad			R ¹	s ¹	Dest ¹		Opcode	е		RAM	Addre	ess
TOR2	0 = B 1 = W	10	0001 0010 0101	TODAR TOAIR TODIR	D ACC D	ACC I	RAM RAM RAM	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1011	SUBSC ² R SUBSC ² R ADD R ADDC R AND R NAND R EXOR R NOR R	iminus R iminus R iminus R iminus R iminus S iminus R imi	00000	R00 R31		Reg 00 Reg 31

Note 1: R = Source
S = Source
Dest = Destination
Note 2: During subtraction the carry is interpreted as borrow.

Instruction	B/W	Quad	es-colonia.		R ¹	S ¹		O	ocode		Des	tination
TONR	0 = B 1 = W	11	0001 0010 0101	TODA TOAI TODI	D ACC D	ACC I	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011	SUBR SUBSC SUBSC ADD ADDC AND NAND EXOR NOR OR EXNOR	S minus R S minus R S minus R with carry R minus S with carry R plus S with carry R plus S with carry R-S-S-R-S-	00000 00001 00100 00101	NRY NRA NRS NRAS	Y Bus ACC Status ² ACC, Status ²

Notes 1: R = Source
S = Source
2: When status is destination,
Status i... Y_i i = 0 to 3 (Byte mode)
i = 0 to 7 (Word mode)
3: During subtraction the carry is interpreted as borrow.
4: OVR = C₈ # C₇ (Byte mode)
OVR = C₁₆ # C₁₅ (Word mode)

Y BUS AND STATUS CONTENTS - TWO OPERAND INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y - Bus	Flag3	Flag2	Flag 1	LINK	OVR	N	С	z
	SUBR	S minus R	0 = B	Y - S + \(\overline{R} + 1 \)	NC	NC	NC	NC	U	υ	U	U
	SUBRC	S minus R with carry	1 = w	Y - S + R + QC	NC	NC	NC	NC	U	U	U	U
	SUBS	R minus S		Y - R + S + 1	NC	NC	NC	NC	U	U	U	U
TOR1 TOR2	SUBSC	R minus S with carry		Y ← R + S + QC	NC	NC	NC	NC	U	U	U	U
TONR	ADD	R plus S		Y - R + S	NC	NC	NC	NC	U	U	U	U
	ADDC	R plus S with carry		Y - R + S + QC	NC	NC	NC	NC	U	U	U	U
	AND	R·S		Y-Ri AND Si	NC	NC	NC	NC	0	U	0	U
	NAND	R·S		Yi-Ri NAND Si	NC	NC	NC	NC	0	U	0	U
	EXOR	R⊕S		Yi-Ri EXOR Si	NC	NC	NC	NC	0	U	0	U
	NOR	R+S		Yi-Ri NOR Si	NC	NC	NC	NC	0	U	0	U
	OR	R+S		Yi-Ri OR Si	NC	NC	NC	NC	0	U	0	υ
	EXNOR	R⊕S		Yi-Ri EXNOR Si	NC	NC	NC	NC	0	0	0	υ

U = Update

NC = No Change

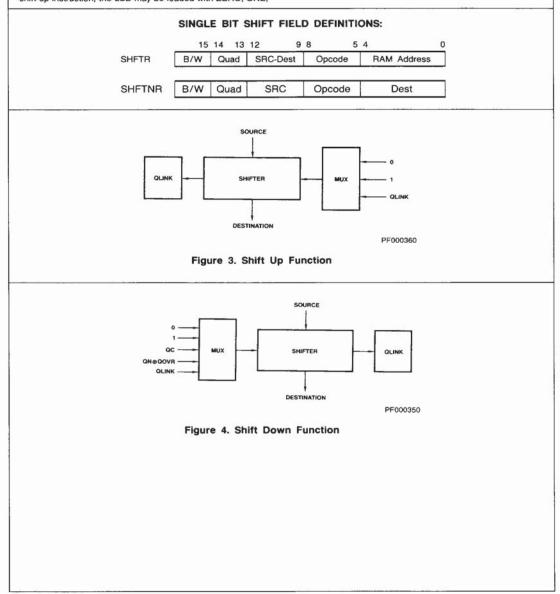
0 = Reset 1 = Set

i = 0 to 15 when not specified

SINGLE BIT SHIFT INSTRUCTIONS

The Single Bit Shift Instructions contain four indicators: byte or word mode, direction and shift linkage, source and destination. They are further subdivided into two types. The first type uses RAM as the source and/or destination and the second type does not use RAM as source or destination. Under the control of the instruction inputs, the desired shift function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The direction and shift linkage indicator defines the direction of the shift (up or down) as well as what will be shifted into the vacant bit. On a shift-up instruction, the LSB may be loaded with ZERO, ONE,

or the Link-Status bit (QLINK). The MSB is loaded into the Link-Status bit as shown in Figure 3. On a shift-down instruction, the MSB may be loaded with ZERO, ONE, the contents of the Status Carry flip-flop, (QC), the Exclusive-OR of the Negative-Status bit and the Overflow-Status bit (QN \oplus QOVR) or the Link-Status bit. The LSB is loaded into the Link-Status bit as shown in Figure 4. The N and Z bits of the Status register are affected but the OVR and C bits are forced to ZERO. The Shift-Down with QN \oplus QOVR is useful for Two's Complement multiplication.



SINGLE BIT SHIFT INSTRUCTIONS

SINGLE BIT SHIFT

Instruction	B/W	Quad		1.40348	U ¹	Dest ¹		Op	code	Ke Manager		RAM	Address
SHFTR	0 = B 1 = W	10	0110 0111	SHRR SHDR	RAM D	RAM RAM	0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000	R00 R31	RAM Reg 00 RAM Reg 31
Instruction	B/W	Quad		349300	U ¹			Оре	code	1000		Des	tination
SHFTNR	0 = B 1 = W	11	0110 0111	SHA SHD	ACC D		0000 0001 0010 0100 0101 0110 0111 1000	SHUPZ SHUP1 SHUPL SHDNZ SHDN1 SHDNL SHDNC SHDNOV	Up Up Up Down Down Down Down Down	0 1 QLINK 0 1 QLINK QC QN⊕QOVR	00000 00001	NRY NRA	Y Bus ACC

U = Source Dest = Destination Note 1.

Y BUS AND STATUS - SINGLE BIT SHIFT INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	C	z
	SHUPZ SHUP1	Up 0 Up 1	1 = W	$Y_i - SRC_{i-1}$, $i = 1$ to 15; $Y_0 - Shift Input$	NC	NC	NC	SRC ₁₅ •	0	SRC ₁₄	0	U
SHR SHNR	SHUPL	Up QLINK	0 = B	Y _i -SRC _{i-1} , i = 1 to 7; Y ₀ -Shift Input; Y _B -SRC ₇ , Y _i -SRC _{i-9} for i = 9 to 15	NC	NC	NC	SRC7+	0	SRC ₆	0	,
	SHDNZ SHDN1	Down 0 Down 1	1 = W	$Y_i - SRC_{i+1}$, $i = 0$ to 14; $Y_{15} - Shift Input$	NC	NC	NC	SRC ₀ •	0	Shift Input	0	ı
	SHDNL SHDNC SHCNOV	Down QLINK Down QC Down QN⊕QOVR	0 = B	$Y_i - SRC_{i+1}$, $i = 0$ to 6; $Y_i - SRC_{i-7}$, $i = 8$ to 14; $Y_{7,15} - Shift Input$	NC	NC	NC	SRC ₀ •	0	Shift Input	0	,

*Shifted Output is loaded into the QLINK.

SRC = Source U = Update NC = No Change 0 = Reset 1 = Set i = 0 to 15 when not specified

BIT ORIENTED INSTRUCTIONS

The Bit Oriented Instructions contain four indicators: byte or word mode, operation, source/destination, and the bit position of the bit to be operated on (Bit 0 is the least significant bit). They are further subdivided into two types. The first type uses the RAM as both source and destination and has two kinds of formats which differ only by quadrant. The second type does not use the RAM as a source or a destination. Under the control of the instruction inputs, the desired function is performed on the specified source and the result is stored in the specified destination or placed on the Y-bus or both. The operations which can be performed are: Set Bit n which forces the nth bit to a ONE leaving other bits unchanged; Reset Bit n

which forces the nth bit to ZERO leaving the other bits unchanged; Test Bit n, which sets the ZERO Status Bit depending on the state of bit n leaving all the bits unchanged; Load 2ⁿ, which loads ONE in Bit position n and ZERO in all other bit positions; Load 2ⁿ which loads ZERO in bit position n and ONE in all other bit positions; increment by 2ⁿ, which adds 2ⁿ to the operand; and decrement by 2ⁿ which subtracts 2ⁿ from the operand. For all the Load, Set, Reset and Test instructions, the N and Z bits are affected and OVR and C bit of the Status register are forced to ZERO. For all arithmetic instructions the LSH (OVR, C, N, Z bits) of the Status register is affected.

BIT ORIENTED FIELD DEFINITIONS

	15	14 13	12 9	8 5	4
BOR1	B/W	Quad	n	Opcode	RAM Address
BOR2	B/W	Quad	n	Opcode	RAM Address
BONR	B/W	Quad	n	1100	Opcode

BIT ORIENTED INSTRUCTIONS

Instruction	B/W	Quad	n		Opcode		RAM	Address
BOR1	0 = B 1 = W	11	0 to 15	1101 SETNR 1110 RSTNR 1111 TSTNR	Set RAM, bit n Reset RAM, bit n Test RAM, bit n	00000	R00 R31	RAM Reg 00 RAM Reg 31
Instruction	B/W	Quad	n		Opcode		RAM	Address
BOR2	0 = B 1 = W	10	0 to 15	1100 LD2NR 1101 LDC2NF 1110 A2NR 1111 S2NR	2 ⁿ - RAM 2 ⁿ - RAM RAM plus 2 ⁿ - RAM RAM minus 2 ⁿ - RAM	00000	R00 R31	RAM Reg 00 RAM Reg 31
Instruction	B/W	Quad	n				Op	code
BONR	0 = B 1 = W	11	0 to 15	1100		00000 00001 00010 00100 00101 00111 10000 10001 10010 10101 10101 10111	TSTNA RSTNA SETNA A2NA S2NA LD2NA LD2NA TSTND RSTND SETND A2NDY S2NDY LS2NY LDC2NY	Test ACC, bit n Reset ACC, bit n Set ACC, bit n ACC plus 2 ⁿ _ACC ACC minus 2 ⁿ _ACC 2 ⁿ _ACC Test D, bit n Reset D, bit n Set D, bi

BIT ORIENTED INSTRUCTIONS Y BUS AND STATUS - BIT ORIENTED INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	z
BOR1	SETNR RSTNR	Set RAM Bit n Reset RAM, Bit n	0 = B 1 = W	$Y_i - RAM_i$ for $i \neq n$; $Y_n - 1$ $Y_i - RAM_i$ for $i \neq n$; $Y_n - 0$	NC NC	NC NC	NC NC	NC NC	0	U	0	0
	TSTNR	Test Ram, Bit n		$Y_i - 0$ for $i \neq n$; $Y_n - SRC_n$	NC	NC	NC	NC	0	U	0	U
	LD2NR	2 ⁿ − RAM	1	$Y_i = 0$ for $i \neq n$; $Y_n = 1$	NC	NC	NC	NC	0	U	0	0
BOR2	LDC2NR	2 ⁿ → RAM	1	Y_i-1 for $i \neq n$; Y_n-0	NC	NC	NC	NC	0	U	0	0
BOHZ	A2NR	RAM + 2 ⁿ → RAM	1	Y ← RAM + 2 ⁿ	NC	NC	NC	NC	U	U	U	U
	S2NR	RAM - 2 ⁿ → RAM	1	Y-RAM-2 ⁿ	NC	NC	NC	NC	U	U	U	U
	TSTNA	Test ACC, Bit n	1	Y _i -0 for i≠n; Y _n -ACC _n	NC	NC	NC	NC	0	U	0	U
	RSTNA	Reset ACC, Bit n	1	$Y_i - ACC_i$ for $i \neq n$; $Y_n = 0$	NC	NC	NC	NC	0	U	0	U
	SETNA	Set ACC, Bit n	1	$Y_i - ACC_i$ for $i \neq n$; $Y_n - 1$	NC	NC	NC	NC	0	U	0	0
	A2NA	ACC + 2 ⁿ → ACC	ĺ	Y-ACC+2n	NC	NC	NC	NC	U	υ	U	ī
	S2NA	ACC - 2 ⁿ → ACC	1	Y-ACC-2 ⁿ	NC	NC	NC	NC	U	U	U	L
	LD2NA	2 ⁿ → ACC	1	$Y_i = 0$ for $i \neq n$; $Y_n = 1$	NC	NC	NC	NC	0	υ	0	0
BONR	LDC2NA	2 ^{TI} → ACC	1	Y_i-1 for $i \neq n$; Y_n-0	NC	NC	NC	NC	0	U	0	0
BONH	TSTND	Test D, Bit n	1	$Y_i - 0$ for $i \neq n$; $Y_n - D_n$	NC	NC	NC	NC	0	U	0	i
	RSTND	Reset D, Bit n*	1	$Y_i - D_i$ for $i \neq n$; $Y_n - 0$	NC	NC	NC	NC	0	U	0	U
	SETND	Set D, Bit n*	1	$Y_i - D_i$ for $i \neq n$; $Y_n - 1$	NC	NC	NC	NC	0	U	0	0
	A2NDY	D + 2 ⁿ → Y Bus	1	Y-D+2 ⁿ	NC	NC	NC	NC	U	U	U	ī
	S2NDY	D-2 ⁿ -Y Bus	1	Y-D-2 ⁿ	NC	NC	NC	NC	U	U	U	ī
	LD2NY	2 ⁿ → Y Bus	1	$Y_i = 0$ for $i \neq n$; $Y_n = 1$	NC	NC	NC	NC	0	U	0	0
	LDC2NY	2n - Y Bus	1	Y_i-1 for $i \neq n$; Y_n-0	NC	NC	NC	NC	0	U	0	0

SRC = Source
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*Destination is not D Latch but Y Bus.

ROTATE BY n BITS INSTRUCTIONS

The Rotate by n Bits Instructions contain four indicators: byte or word mode, source, destination and the number of places the source is to be rotated. They are further subdivided into two types. The first type uses RAM as a source and/or a destination and the second type does not use RAM as a source or destination. The first type has two different formats and the only difference is in the quadrant. The second type has only one format as shown in the table. Under the control of instruction inputs, the n indicator specifies the number of bit positions the source is to be rotated up (0 to 15), and the result is either stored in the specified destination or placed on the Y bus or both. An example of this instruction is given in Figure 5. In the Word mode, all 16-bits are rotated up; while in the Byte mode, only the lower 8-bits (0-7) are rotated up. In the Word mode, a rotate up by n bits is equivalent to a rotate down by (16-n) bits. Similarly, in the Byte mode a rotate up by n bits is equivalent to a rotate down by (8-n) bits. The N and Z bits of the Status Register are affected and OVR and C bits are forced to ZERO.

EXAMPLE: n = 4, Word Mode

Source 0001 0011 0111 1111 Destination 0011 0111 1111 0001

EXAMPLE: n = 4, Byte Mode

Source 0001 0011 0111 1111 Destination 0001 0011 1111 0111

ROTATE BY n BITS FIELD DEFINITIONS

15 14 13 12 9 8 ROTR1 B/W Quad n SRC-Dest RAM Address

ROTR2 B/W SRC-Dest Quad RAM Address п

Figure 5. Rotate by n Example

ROTNR B/W Quad 1100 SRC-Dest n

ROTATE BY n BITS INSTRUCTIONS

Instruction	B/W	Quad	n			U ¹	Dest ¹		RAM	Address	3
ROTR1	0 = B 1 = W	00	0 to 15	1100 1110 1111	RTRA RTRY RTRR	RAM RAM RAM	ACC Y Bus RAM	00000	R00 R31	RAM R	. · .
Instruction	B/W	Quad	n			U ¹	Dest ¹		RAM	Address	3
ROTR2	0 = B 1 = W	01	0 to 15	0000 0001	RTAR RTDR	ACC D	RAM RAM	00000	R00 R31	RAM R	
Instruction	B/W	Quad	n							U ¹	Dest ¹
ROTNR	0 = B 1 = W	11	0 to 15	1100				11000 11001 11100 11101	RTDY RTDA RTAY RTAA	D D ACC ACC	Y Bus ACC Y Bus ACC

Note 1: U = Source Dest = Destination

Y BUS AND STATUS - ROTATE BY n BITS INSTRUCTIONS

Instruction	Op- code	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	z
ROTR1		1 = W	Y _i ⊷ SRC _{(i-n)mod16}	NC	NC	NC	NC	0	SRC 15-n	0	U
ROTR2 ROTNR		0 = B	$Y_{i-}SRC_{i+8} = SRC_{(i-n)mod8}$ for $i = 0$ to 7	NC	NC	NC	NC	0	SRC _{8-n}	0	U

SRC = Source

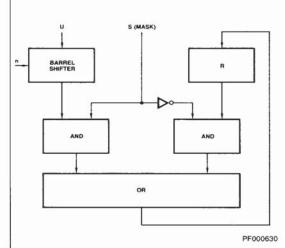
U = No Change 0 = Reset

1 = Set i = 0 to 15 when not specified

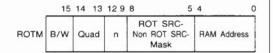
ROTATE AND MERGE INSTRUCTION

The Rotate and Merge Instructions contain five indicators: byte or word mode, rotated source, non-rotated source/ destination, mask and the number of bit positions a source is to be rotated. The function performed by the Rotate and Merge instruction is illustrated in Figure 6. The rotated source, U, is rotated up by the Barrel Shifter n places. The mask input then selects, on a bit by bit basis, the rotated U input or R

input. A ZERO in bit i of the mask will select the ith bit of the R input as the ith output bit, while ONE in bit i will select the ith rotated U input as the output bit. The output word is stored in the non-rotated operand location. The N and Z bits are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 7.



ROTATE AND MERGE FIELD DEFINITIONS:



EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
Rotated U	0001	0101	0110	0011
R	1010	1010	1010	1010
Mask (S)	0000	1111	0000	1111
Destination	1010	0101	1010	0011

Figure 7. Rotate and Merge Example

Figure 6. Rotate and Merge Function

ROTATE AND MERGE INSTRUCTION

Instruction	B/W	Quad	n			U ¹	R/Des	st ¹ S ¹		RAM A	ddress
ROTM	0 = B 1 = W	01	0 to 15	0111 1000 1001 1010 1100	MDAI MDAR MDRI MDRA MARI MBAI	D D D ACC BAM	ACC ACC RAM RAM RAM ACC	RAM I ACC	00000	R00 R31	RAM Reg 00 RAM Reg 31

Note 1.

U = Rotated Source R/Dest = Non-Rotated Source and Destination S = Mask

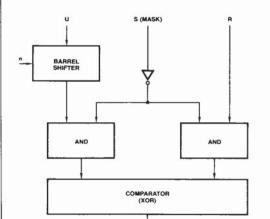
Y BUS AND STATUS - ROTATED MERGE

Instruction	Opcode	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	z
ROTM		1=W	Y _i ← (Non Rot Op) _i · (mask) _i + (Rot Op) _{(i - n)mod 16} · (mask) _i	NC	NC	NC	NC	0	U	0	U
HOIM		0 = B	Y _i ← (Non Rot Op) _i · (mask) _i + (Rot Op) _{(i - n)mod 8} · (mask) _i	NC	NC	NC	NC	0	U	0	U

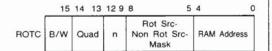
U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

ROTATE AND COMPARE INSTRUCTIONS

The Rotate and Compare Instructions contain five indicators: byte or word mode, rotated source, non-rotated source, mask, and the number of bit positions the rotated source is to be rotated up. Under the control of instruction inputs, the function performed by the Rotate and Compare instruction is illustrated in Figure 8. The rotated operand is rotated by the Barrel Shifter n places. The mask is inverted and ANDed on a bit-by-bit basis with the output of the Barrel Shifter and R input. Thus, a ONE in the mask input eliminates that bit from the comparison. A ZERO allows the comparison. If the comparison passes, the Zero flag is set. If it fails, the Zero flag is reset. The N and Z bit are affected. The OVR and C bits of the Status register are forced to ZERO. An example of this instruction is given in Figure 9.



ROTATE AND COMPARE FIELD DEFINITIONS



EXAMPLE: n = 4, Word Mode

U	0011	0001	0101	0110
	0001	0101	0110	0011
U Rotated				
R	0001	0101	1111	0000
Mask (S)	0000	0000	1111	1111
7 (etatue) = 1				

Figure 9. Rotate and Compare Examples

Figure 8. Rotate and Compare Function

ROTATE AND COMPARE INSTRUCTIONS

PF000650

Instruction	B/W	Quad	n			U ¹	R ¹	S ¹		RAM A	ddress
ROTC	0=B 1 = W	01	0 to 15	0010 0011 0100 0101	CDAI CDRI CDRA CRAI	D D D RAM	ACC RAM RAM ACC	ACC	00000	R00 R31	RAM Reg 00 RAM Reg 31

U = Rotated Source R = Non-Rotated Source S = Mask Note 1.

Y BUS AND STATUS - ROTATE AND COMPARE

Instruction	Opcode	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	Z
poro		1 = W	Y _i - (Non Rot Op) _i · (mask) _i ⊕ (Rot Op) _{(i - n)mod 16} · (mask) _i	NC	NC	NC	NC	0	U	0	U
ROTC		0 = B	Y _i (Non Rot Op) _i · (mask) _i ⊕ (Rot Op) _{(i - n)mod 8} · (mask) _i	NC	NC	NC	NC	0	U	0	U

U = Update NC = No Change 0 = Reset 1 = Set i = 0 to 15 when not specified

PRIORITIZE INSTRUCTION

The Prioritize Instructions contain four indicators: byte or word mode, operand source (R), mask source (S) and destination. They are further subdivided into two types. The function performed by the Prioritize instruction is shown in Figure 10. The R operand is ANDed with the complement of the Mask operand. A ZERO in the Mask operand allows the corresponding bit in the R operand to participate in the priority encoding function. A ONE in the Mask operand forces the corresponding bit in the R operand to a ZERO, eliminating it from participation in the priority encoding function.

The priority encoder accepts a 16-bit input and produces a 5-bit binary-weighted code indicating the bit position of the highest priority active bit. If none of the inputs are active, the output is ZERO. In the Word mode, if input bit 15 is active, the output is 1, etc. Figure 11 lists the output as a function of the highest-priority active-bit position in both the Word and Byte mode. The N and Z bits are affected and the OVR and C bits of the status register are forced to ZERO. The only limitation in this instruction is that the operand and the mask must be different sources.

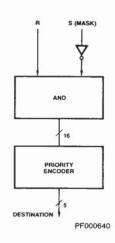


Figure 10. Prioritize Function

PRIORITIZE INSTRUCTION FIELD DEFINITIONS

15	14 13	12 9	8 5	4
B/W	Quad	Destination	Source (R)	RAM Address/ Mask (S)
B/W	Quad	Mask (S)	Destination	RAM Address/ Source (R)
B/W	Quad	Mask (S)	Source (R)	RAM Address/ Destination
B/W	Quad	Mask (S)	Source (R)	Destination

WORD	MODE	BYTE MODE*				
Highest Priority Active Bit	Encoder Output	Highest Priority Active Bit	Encoder Output			
None	0	None	0			
15	1	7	1			
14	2	6	2			
			22			
1	15	1	7			
0	16	0	8			

*Bits 8 through 15 do not participate.

Figure 11.

PRIORITIZE INSTRUCTION

Instruction	B/W	Quad		Destination	on		Source (F	?)	RAI	M Addre	ss/Mask (S)
PRT1	0 = B 1 = W	10	1000 1010 1011	PRIA PR1Y PR1R	ACC Y Bus RAM	0111 1001	RPT1A PR1D	ACC D	00000	R00 R31	RAM Reg 00 RAM Reg 31
Instruction	B/W	Quad		Mask (S)			Destinatio	n	RAM Address/Source (R		
PRT2	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	Acc 0 I	0000 0010	PR2A PR2Y	ACC Y Bus	00000	R00 R31	RAM Reg 00
Instruction	B/W	Quad		Mask (S	k (S) Source (R) RAM Addre		ress/Dest				
PRT3	0 = B 1 = W	10	1000 1010 1011	PRA PRZ PRI	ACC 0 I	0011 0100 0110	PR3R PR3A PR3D	RAM ACC D	00000	R00 R31	RAM Reg 00
Instruction	B/W	Quad	9	Mask (S	5)		Source (F	R)		Desti	nation
PRTNR	0 = B 1 = W	11	1000 1010 1011	PRA PRZ PRI	ACC 0	0100 0110	PRTA PRTD	ACC D	00000 00001	NRY NRA	Y Bus ACC

Y BUS AND STATUS - PRIORITIZE INSTRUCTION											
Instruction	Opcode	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	Z
PRT1 PRT2		1 = W	Y _i - CODE (SCR _n ·mask _n); Y _m - 0; i = 0 to 4 and n = 0 to 15 m = 5 to 15	NC	NC	NC	NC	0	U	0	U
PRT3 PRTNR		0 = B	Y _i -CODE (SCR _n ·mask _n); Y _m -0; i = 0 to 3 and n = 0 to 7 m = 4 to 15	NC	NC	NC	NC	0	υ	0	U

SRC = Source NC = No Change U = Update 0 = Reset

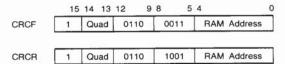
1 = Set i = 0 to 15 when not specified

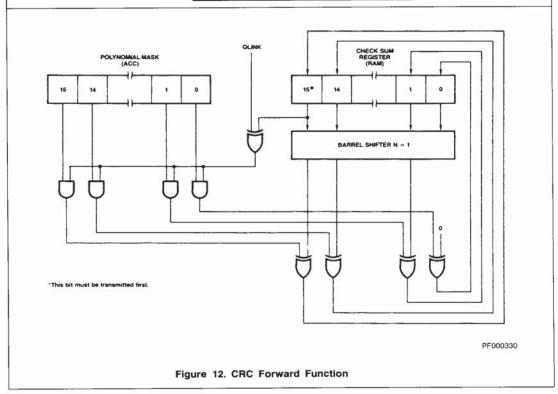
CRC INSTRUCTION

The CRC (Cyclic-Redundancy-Check) Instructions contain one indicator: address of a RAM register to use as the check sum register. The CRC instruction provides a method for generation of the check bits in a CRC calculation. Two CRC instructions are provided – CRC Forward and CRC Reverse. The reason for providing two instructions is that CRC standards do not specify which data bit is to be transmitted first, the LSB or the MSB, but they do specify which check bit must be transmitted first. Figure 12 illustrates the method used to generate these check bits for the CRC Forward function and

Figure 13 illustrates method used for the 2CRC Reverse function. The ACC serves as a polynomial mask to define the generating polynomial while the RAM register holds the partial result and eventually the calculated check sum. The LINK-bit is used as the serial input. The serial input combines with the MSB of the check-sum register, according to the polynomial defined by the polynomial mask register. When the last input bit has been processed, the check-sum register contains the CRC check bits. The LINK, N and Z bits are affected and the OVR and C bits of the Status register are forced to ZERO.

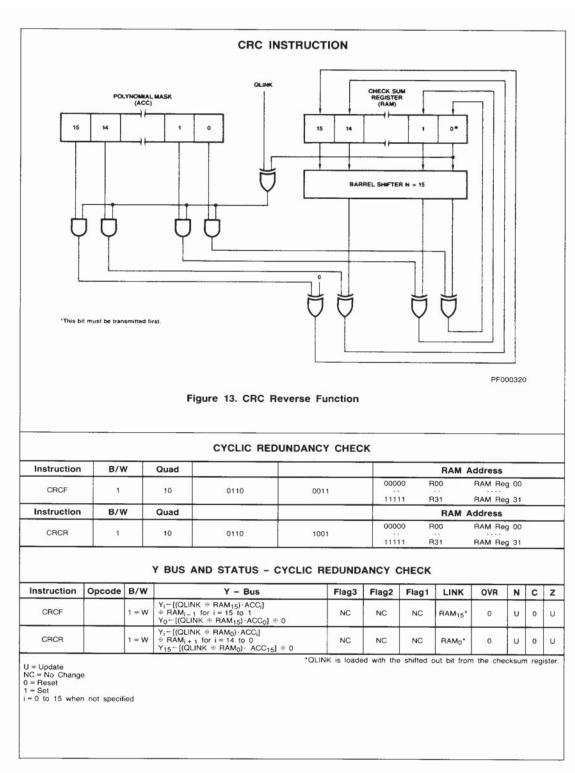
CYCLIC-REDUNDANCY-CHECK DEFINITIONS:





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STATUS INSTRUCTIONS

Status Instructions - The Set Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register (Figure 14), are to be set (forced to a ONE).

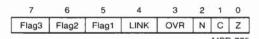


Figure 14. Status Byte

The Reset Status Instruction contains a single indicator. This indicator specifies which bit or group of bits, contained in the status register, are to be reset (forced to ZERO).

The Store Status Instruction contains two indicators; byte/word and a second indicator that specifies the destination of the status register. The Store Status Instruction allows the status of the processor to be saved and restored later, which is an especially useful function for interrupt handling.

The status register is always stored in the lower byte of the RAM or the ACC register. Depending upon byte or word mode the upper byte is unchanged or loaded with all ZEROs respectively.

The Load Status instructions are included in the single operand and two operand instruction types.

The Test Status Instructions contain a single indicator which specifies which one of the 12 possible test conditions are to be placed on the Conditional-Test output. Besides the eight bits in the Status register (OZ, QC, QN, QOVR, QLINK, QFlag1, QFlag 2, and QFlag3), four logical functions (QN \oplus QOVR), (QN \oplus QOVR) + QZ, QZ + $\overline{\rm QC}$ and LOW may also be selected. These functions are useful in testing results of Two's Complement and unsigned number arithmetic operations. The status register may also be tested via the bidirectional T bus. The code to test the status register via T bus is similar to the code used by instruction lines $\rm I_1$ to $\rm I_4$ as shown below. Instruction lines $\rm I_0$ – 4 have priority over T bus for testing the

status register on CT output. See the discussion on the status register for a full description.

T ₄	T ₃	T ₂	T ₁	ст
0	0	0	0	(N ⊕ OVR) + Z
0	0	0	1	N ⊕ OVR
0	0	1	0	Z
0	0	1	1	OVR
0	1	0	0	rom.
0	1	0	1	С
0	1	1	0	Z + C
0	1	1	1	N
1	0	0	0	LINK
1	0	0	1	Flag1
1	0	1	0	Flag2
1	0	1	1	Flag3

*LOW = CT is forced LOW

STATUS

	15	14 13	12 9	8 5	4
SETST	0	Quad	1011	1010	Opcode
RSTST	0	Quad	1010	1010	Opcode
SVSTR	B/W	Quad	0111	1010	RAM Address/Dest
SVSTNR	B/W	Quad	0111	1010	Destination

STATUS INSTRUCTIONS

Instruction	B/W	Quad				C	pcode
SETST	0	11	1011	1010	00011 00101 00110 01001 01010	SONCZ SL SF1 SF2 SF3	Set OVR, N, C, Z Set LINK Set Flag1 Set Flag2 Set Flag3
Instruction	B/W	Quad		Life			pcode
RSTST	0	11	1010	1010	00011 00101 00110 01001 01010	RONCZ RL RF1 RF2 RF3	Reset OVR, N, C, Z Reset LINK Reset Flag1 Reset Flag2 Reset Flag3
Instruction	B/W	Quad				RAM A	ddress/Dest
SVSTR	0 = B 1 = W	10	0111	1010	00000 11111	R00 R31	RAM Reg 00 RAM Reg 31
412.						De	stination
SVSTNR	0 = B 1 = W	11	0111	1010	00000 00001	NRY NRA	Y Bus ACC

STATUS INSTRUCTIONS Instruction B/W Quad Opcode (CT) Test (N⊕OVR) + Z Test N⊕OVR Test Z Test OVR Test LOW Test C Test C Test X + C Test NK Test LINK Test Flag1 Test Flag3 TNOZ TNO TZ TOVR TLOW TC TZC TN TL TF1 TF1 TF2 TF3 00000 00010 00100 00110 01000 01010 01110 10000 10110 10100 10110 Test 1001 1010

Note: IEN • test status instruction has priority over T₁₋₄ instruction.

Y BUS AND STATUS - FOR STATUS INSTRUCTIONS

Instruction	Opcode	Description	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	Z
	SONCZ	Set OVR, N, C, Z	0 = B	Y _i -1 for i = 0 to 15	NC	NC	NC	NC	1	1	1	1
	SL	Set LINK	1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	NC	NC	NC	1	NC	NC	NC	NO
SETST	SF1	Set Flag1			NC	NC	1	NC	NC	NC	NC	N
	SF2	Set Flag2			NC	1	NC	NC	NC	NC	NC	N
	SF3	Set Flag3			1	NC	NC	NC	NC	NC	NC	N
C-12-12-12	RONCZ	Reset OVR, N, C, Z	0 = B	Y _i -0 for i = 0 to 15	NC	NC	NC	NC	0	0	0	(
	RL	Reset LINK	1		NC	NC	NC	0	NC	NC	NC	N
RSTST	RF1	Reset Flag1			NC	NC	0	NC	NC	NC	NC	N
	RF2	Reset Flag2			NC	0	NC	NC	NC	NC	NC	N
	RF3	Reset Flag3			0	NC	NC	NC	NC	NC	NC	N
SVSTR SVSTNR		Save Status*	0 = B 1 = W	Y _i -Status for i - 0 to 7; Y _i -0 for i = 8 to 15	NC	NC	NC	NC	NC	NC	NC	N
	TNOZ	Test (N⊕OVR) + Z	0 = B	••	NC	NC	NC	NC	NC	NC	NC	N
	TNO	Test N⊕OVR	1		NC	NC	NC	NC	NC	NC	NC	N
	TZ	Test Z	1		NC	NC	NC	NC	NC	NC	NC	N
	TOVR	Test OVR	7		NC	NC	NC	NC	NC	NC	NC	N
	TLOW	Test LOW	1		NC	NC	NC	NC	NC	NC	NC	N
Test	TC	Test C	1		NC	NC	NC	NC	NC	NC	NC	N
	TZC	Test Z + C	1		NC	NC	NC	NC	NC	NC	NC	N
	TN	Test N	1		NC	NC	NC	NC	NC	NC	NC	N
	TL	Test LINK	\dashv		NC	NC	NC	NC	NC	NC	NC	N
	TF1	Test Flag1	1		NC	NC	NC	NC	NC	NC	NC	N
	TF2	Test Flag2	1		NC	NC	NC	NC	NC	NC	NC	N
	TF3	Test Flag3	-		NC	NC	NC	NC	NC	NC	-	N

U = Update
NC = No Change
0 = Reset
1 = Set
i = 0 to 15 when not specified

*In byte mode only the lower byte from the Y bus is loaded into the RAM or ACC and in word mode all 16-bits from the Y bus are loaded into the RAM or ACC.

**Y-Bus is Undefined.

NO-OP INSTRUCTION

The NO-OP Instruction has a fixed 16-bit code. This instruction does not change any internal registers in the Am29C116. It preserves the status register, RAM register and the ACC register.

NO OPERATION FIELD DEFINITION

NOOP

15 14 13 12 9 8 5 4 0 0 11 1000 1010 00000

NO-OP INSTRUCTION

Instruction	B/W	Quad			
NOOP	0	11	1000	1010	00000

Y BUS AND STATUS - NO-OP INSTRUCTION

Instruction	Opcode	B/W	Y - Bus	Flag3	Flag2	Flag1	LINK	OVR	N	С	Z
NOOP		0 = B	•	NC	NC	NC	NC	NC	NC	NC	NC

SRC = Source U = Update NC = No Change

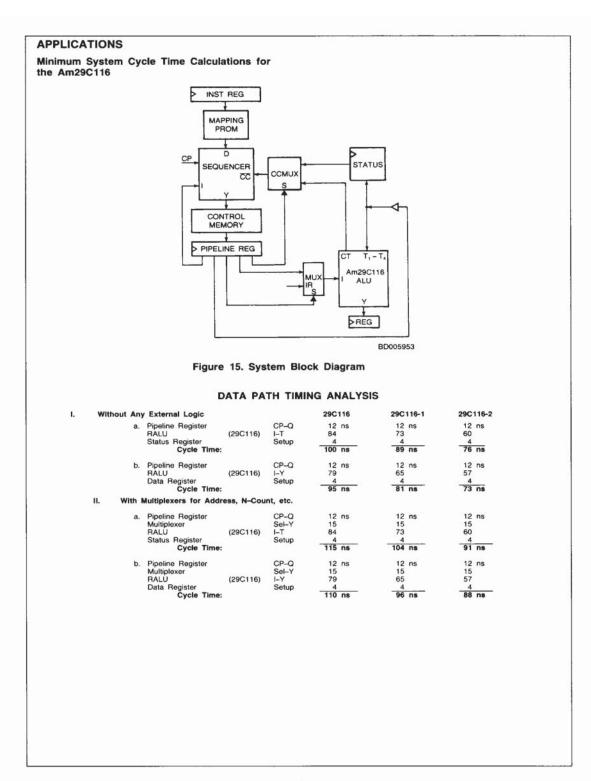
0 = Reset

1 = Seti = 0 to 15 when not specified

*Y-Bus is undefined.

	SUMMARY OF	- MNEMONIC	5
Instruction	Туре	Two Opera	ind
SOR	Single Operand RAM	TORAA	Two Operand RAM, ACC to ACC
SONR	Single Operand Non-RAM	TORIA	Two Operand RAM, I to ACC
TOR1	Two Operand RAM (Quad 0)	TODRA	Two Operand D, RAM to ACC
TOR2	Two Operand RAM (Quad 2)	TORAY	Two Operand RAM, ACC to Y Bus
TONR	Two Operand Non-RAM	TORIY	Two Operand RAM, I to Y Bus
SHFTR	Single Bit Shift RAM	TODRY	Two Operand D, RAM to Y Bus
SHFTNR		TORAR	Two Operand RAM, ACC to RAM
ROTR1	Rotate n Bits RAM (Quad 0)	TORIR	Two Operand RAM, I to RAM
ROTR2	Rotate n Bits RAM (Quad 1)	TODRR	Two Operand D, RAM to RAM
ROTNR	Rotate n Bits Non-RAM	TODAR	Two Operand D, ACC to RAM
BOR1	Bit Oriented RAM (Quad 3)	TOAIR	Two Operand ACC, I to RAM
BOR2	Bit Oriented RAM (Quad 2)	TODIR	Two Operand D, I to RAM
BONR	Bit Oriented Non-RAM	TODA	Two Operand D, ACC
ROTM	Rotate and Merge	TOAL	Two Operand ACC, I
ROTC	Rotate and Compare	TODI	Two Operand D, I
PRT1	Prioritize RAM; Type 1		
PRT2	Prioritize RAM; Type 2	Single Bit 5	Shift
PRT3		SHRR	Shift RAM, Store in RAM
	Prioritize RAM; Type 3	SHDR	Shift D, Store in RAM
PRTNR	Prioritize Non-RAM	SHA	Shift ACC
CRCF	Cyclic Redundancy Check Forward	SHD	Shift D
CRCR	Cyclic Redundancy Check Reverse		
NOOP	No Operation	Rotate n B	its
SETST	Set Status	RTRA	Rotate RAM, Store in ACC
RSTST	Reset Status	RTRY	Rotate RAM, Place on Y Bus
SVSTR	Save Status RAM	RTRR	Rotate RAM, Store in RAM
	Save Status Non-RAM	RTAR	Rotate ACC, Store in RAM
TEST	Test Status	RTDR	Rotate D, Store in RAM
SOURCE A	ND DESTINATION	RTDY	Rotate D, Place on Y Bus
Single Oper		RTDA	Rotate D, Store in ACC
		RTAY	Rotate ACC, Place on Y Bus
SORA	Single Operand RAM to ACC	RTAA	Rotate ACC, Store in ACC
SORY	Single Operand RAM to Y Bus		
SORS	Single Operand RAM to Status	Rotate and	Merge
SOAR	Single Operand ACC to RAM	MDAI	Merge Disjoint Bits of D and ACC Using
SODR	Single Operand D to RAM		I as Mask and Store in ACC
SOIR	Single Operand I to RAM	MDAR	Merge Disjoint Bits of D and ACC Using
SOZR	Single Operand 0 to RAM		RAM as Mask and Store in ACC
SOZER	Single Operand D(0E) to RAM	MDRI	Merge Disjoint Bits of D and RAM Usin
SOSER	Single Operand D(SE) to RAM		I as Mask and Store in RAM
SORR	Single Operand RAM to RAM	MDRA	Merge Disjoint Bits of D and RAM Usin
SOA	Single Operand ACC		ACC as Mask and Store in RAM
SOD	Single Operand D	MARI	Merge Disjoint Bits of ACC and RAM
SOI	Single Operand I		Using I as Mask and Store in RAM
SOZ	Single Operand 0	MRAI	Merge Disjoint Bits of RAM and ACC
SOZE	Single Operand D(0E)		Using I as Mask and Store in ACC
SOSE	Single Operand D(SE)	D-4-4-	0
NRY	Non-RAM Y Bus	Rotate and	Compare
NRA	Non-RAM ACC	CDAI	Compare Unmasked Bits of D and ACC
NRS	Non-RAM Status		Using I as Mask
NRAS	Non-RAM ACC, Status		

CDRA CRAI Prioritize PR1A PR1Y PR1B PRT1A PR1D PR2A PR2Y PR3B PR3A PR3D PRTA	Compare Unmasked Bits of D and RAM Using ACC as Mask Compare Unmasked Bits of RAM and ACC Using I as Mask ACC as Destination for Prioritize Type 1 Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3 D as Source for Prioritize Type 3	SHDN1 SHDNL SHDNC SHDNOV Loads LD2NR LDC2NR LDC2NA LDC2NA LDC2NA LDC2NY LDC2NY	Shift Down Towards LSB with 1 Insert Shift Down Towards LSB with LINK Insert Shift Down Towards LSB with Carry Insert Shift Down Towards LSB with Sign EXCOVERSION Insert Load 2 ⁿ into RAM Load 2 ⁿ into RAM Load 2 ⁿ into ACC Load 2 ⁿ into ACC Place 2 ⁿ on Y Bus Place 2 ⁿ on Y Bus
Prioritize PR1A PR1Y PR1R PR11A PR1D PR2A PR2Y PR3R PR3A PR3D	Using ACC as Mask Compare Unmasked Bits of RAM and ACC Using I as Mask ACC as Destination for Prioritize Type 1 Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	SHDNC SHDNOV Loads LD2NR LDC2NR LD2NA LDC2NA LDC2NA LD2NY LDC2NY	Shift Down Towards LSB with Carry Inset Shift Down Towards LSB with Sign EXO Overflow Insert
Prioritize PR1A PR1Y PR1B PRT1A PR1D PR2A PR2Y PR3R PR3A PR3D	Compare Unmasked Bits of RAM and ACC Using I as Mask ACC as Destination for Prioritize Type 1 Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	SHDNOV Loads LD2NR LDC2NR LD2NA LDC2NA LDC2NY	Shift Down Towards LSB with Sign EXO Overflow Insert
Prioritize PR1A PR1Y PR1B PRT1A PR1D PR2A PR2Y PR3R PR3A PR3D	ACC Using I as Mask ACC as Destination for Prioritize Type 1 Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	Loads LD2NR LDC2NR LD2NA LDC2NA LDC2NA LD2NY	Overflow Insert Load 2^n into RAM Load 2^n into RAM Load 2^n into ACC Load 2^n into ACC Place 2^n on Y Bus
PR1A PR1Y PR1R PR11A PR1D PR2A PR2Y PR3R PR3A PR3D	Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LD2NR LDC2NR LD2NA LDC2NA LD2NY LDC2NY	Load $\overline{2}^n$ into RAM Load 2^n into ACC Load $\overline{2}^n$ into ACC Place 2^n on Y Bus
PR1Y PR1R PRT1A PR1D PR2A PR2Y PR3R PR3A PR3D	Y Bus as Destination for Prioritize Type 1 RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LDC2NR LD2NA LDC2NA LD2NY LDC2NY	Load $\overline{2}^n$ into RAM Load 2^n into ACC Load $\overline{2}^n$ into ACC Place 2^n on Y Bus
PR1R PR11A PR1D PR2A PR2Y PR3R PR3A PR3D	RAM as Destination for Prioritize Type 1 ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LD2NA LDC2NA LD2NY LDC2NY	Load 2 ⁿ into ACC Load 2 ⁿ into ACC Place 2 ⁿ on Y Bus
PRT1A PR1D PR2A PR2Y PR3R PR3A PR3D	ACC as Source for Prioritize Type 1 D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LDC2NA LD2NY LDC2NY	Load $\overline{2}^n$ into ACC Place 2^n on Y Bus
PR1D PR2A PR2Y PR3R PR3A PR3D	D as Source for Prioritize Type 1 ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LD2NY LDC2NY	Load $\overline{2}^n$ into ACC Place 2^n on Y Bus
PR2A PR2Y PR3R PR3A PR3D	ACC as Destination for Prioritize Type 2 Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3	LDC2NY	Place 2 ⁿ on Y Bus
PR2Y PR3R PR3A PR3D	Y Bus as Destination for Prioritize Type 2 RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3		
PR3R PR3A PR3D	RAM as Source for Prioritize Type 3 ACC as Source for Prioritize Type 3		
PR3A PR3D	ACC as Source for Prioritize Type 3	Bit Oriente	
PR3D			d
	D as Source for Prioritize Type 3	SETNR	Set RAM, Bit n
PRTA		SETNA	Set ACC, Bit n
	ACC as source for Prioritize Type	SETND	Set D, Bit n
	Non-RAM	SONCZ	Set OVR, N, C, Z, in Status Register
PRTD	D as Source for Prioritize Type Non-RAM	SL	Set LINK Bit in Status Register
PRA	ACC as Mask for Prioritize Type 2, 3,	SF1	
	and Non-RAM		Set Flag Bit in Status Register
PRZ	Mask Equal to Zero for Prioritize Type	SF2	Set Flag2 Bit in Status Register
	2, 3, and Non-RAM	SF3	Set Flag3 Bit in Status Register
PRI	I as Mask for Prioritize Type 2, 3, and	RSTNR	Reset RAM, Bit n
	Non-RAM	RSTNA	Reset ACC, Bit n
OPCODE		RSTND	Reset D, Bit n
Addition		RONCZ	Reset OVR, N, C, Z, in Status Register
		RL	Reset LINK Bit in Status Register
ADD	Add without Carry	RF1	Reset Flag1 Bit in Status Register
ADDC	Add with Carry	RF2	Reset Flag2 Bit in Status Register
A2NA	Add 2 ⁿ to ACC	RF3	Reset Flag3 Bit in Status Register
A2NR	Add 2 ⁿ to RAM	TSTNR	Test RAM, Bit n
A2NDY	Add 2 ⁿ to D, Place on Y Bus	TSTNA TSTND	Test ACC, Bit n Test D, Bit n
Subtraction			
SUBR	Subtract R from S without Carry	Arithmetic	
SUBRC	Subtract R from S with Carry	MOVE	Move and Update Status
SUBS	Subtract S from R without Carry	COMP	Complement (1's Complement)
SUBSC	Subtract S from R with Carry	INC	Increment
S2NR	Subtract 2 ⁿ from RAM	NEG	Two's Complement
S2NA	Subtract 2 ⁿ from ACC	Conditional	Test
S2NDY	Subtract 2 ⁿ from D, Place on Y Bus		
Logical Ope	erations	TNOZ	Test (N ⊕ OVR) + Z
		TNO	Test N ⊕ OVR
AND	Boolean AND	TZ	Test Zero Bit
NAND	Boolean NAND	TOVR	Test Overflow Bit
EXOR	Boolean EXOR	TLOW	Test for LOW
NOR	Boolean NOR	TC	Test Carry Bit
OR	Boolean OR	TZC	Test Z + C
EXNOR	Boolean EXNOR	TN	Test Negative Bit
SHIFTS		TL	Test LINK Bit
	12.00 PO NE	TF1	Test Flag1 Bit
SHUPZ	Shift Up Towards MSB with 0 Insert	TF2	Test Flag2 Bit
SHUP1	Shift Up Towards MSB with 1 Insert	TF3	Test Flag3 Bit
SHUPL	Shift Up Towards MSB with LINK Insert		opyright © 1980 tro Devices, Inc.



The Use of an External Status Register in Reducing Microcycle Length

The standard connection of the CT pin of the Am29C116 and microcycle length calculation arising from that connection are shown below:

CRITICAL PATH TIMING (FIGURE 16-1)

Part Number	Path	Maximum Commercial Delay (ns)
Pipeline Register	CP-Q	12
Am29C116-2	I, T-CT	25
CC-MUX	D-W	7
Am29C10A-1	CC-Y	26
Control Memory	taa	40
Pipeline Register	taa Setup	4
		114

While 114-ns cycle time is quite fast, it can be improved by using an external register for status testing.

CRITICAL PATH TIMING (FIGURE 16-2)

Part Number	Path	Maximum Commercial Delay (ns)
Status Reg	CP-Y	12
CC-MUX	Sel-W	15
Am29C10A-1	CC-Y	26
Control Memory	taa	40
Pipeline Register	t _{AA} Setup	4
		97

The cycle time has been reduced from 114 ns to 97 ns.

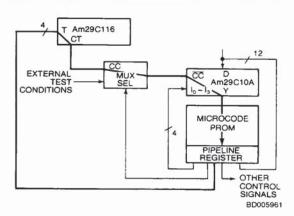


Figure 16-1.

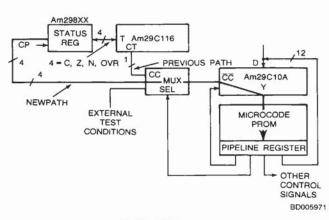


Figure 16-2.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature-65 to +150°C (Case) Temperature Under Bias -55 to +125°C Supply Voltage to Ground Potential Continuous-0.3 V to +7.0 V DC Voltage Applied to Outputs For

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

(T _A) 0 to +70°C +4.5 V to +5.5 V
(T _A)55 to +125°C +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

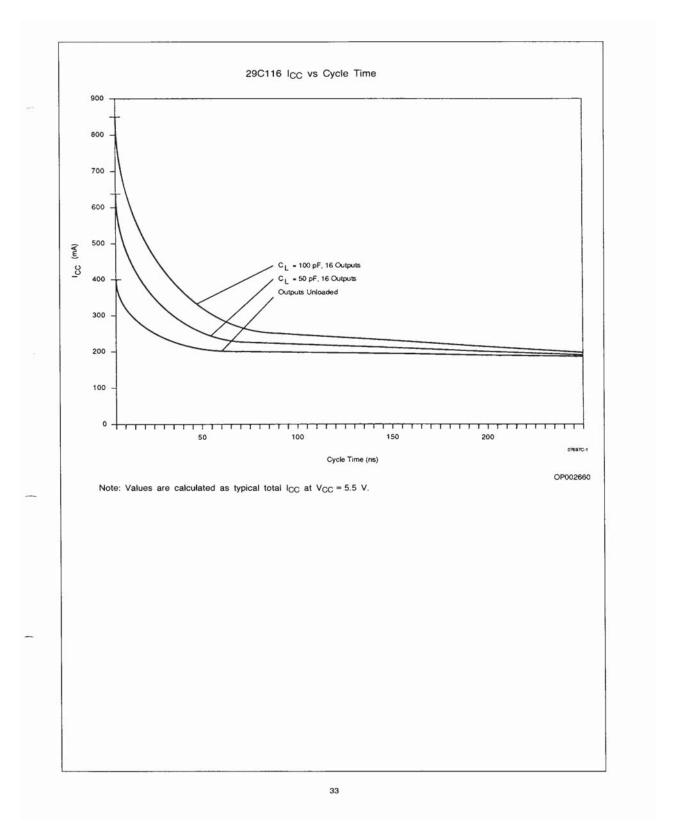
*Military Product 100% tested at TA = +25°C, +125°C, and -55°C.

DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Min.	Max.	Unit													
VoH	Output HIGH Voltage	$V_{CC} = Min.$ $V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -1.6 \text{ mA}/-1.2 \text{ mA}$ (COM^*L/MIL)					٧											
VOL	Output LOW Voltage	V _{CC} = Min. I _{OL} = 16 mA/12 mA (COM'L/MIL)				0.5	٧											
V _{IH}	Guaranteed Input Logical HIGH Voltage (Note 2)		2.0		v													
VIL	Guaranteed Input Logical LOW Voltage (Note 2)			0.8	٧													
lıL.	Input LOW Current	V _{CC} = Max. V _{IN} = 0.5 Volts		-10	μΑ													
l _{IH}	Input HIGH Current	V _{CC} = Max. V _{IN} = V _{CC} - 0.5		10	μΑ													
lozh	Off State (HIGH Impedance) Output Current	V _{CC} = Max. V _O = 2.4 Volts		10	μА													
lozL	Off State (HIGH Impedance) Output Current	V _{CC} = Max. V _O = 0.5 Volts		- 10	μА													
-		COM'L		(Note 4) CMOS V _{IN} = V _{CC} or GND		120												
ig.	Static Power Supply Current	V _{CC} = Max. I _O = 0 μA		The state of the s		The state of the s			CONTRACTOR OF THE SECTION OF THE SEC	***************************************				T _A = 0 to +70°C	(Note 4) TTL V _{IN} = 0.5 V or 2.4 V		170	
Icc	(Note 3)								MIL	(Note 4) CMOS V _{IN} = V _{CC} or GND		145	mA					
			T _A = -55 to + 125°C	(Note 4) TTL V _{IN} = 0.5 V or 2.4 V		200												
C _{PD}	Power Dissipation Capacitance (Note 5)	V _{CC} = 5.0 V T _A = 25°C No Load	8	350 pF Typic	cal													

Notes: 1. V_{CC} conditions shown as Min. or Max. refer to ±10% V_{CC} limits.
2. These input levels provide zero-noise immunity and should only be statically tested in a noise-free environment (not functionally tested).
3. Worst-case I_{CC} is measured at the lowest temperature in the specified operating range.
4. Use CMOS I_{CC} when the device is driven by CMOS circuits and TTL I_{CC} when the device is driven by TTL circuits.
5. C_{PD} determines the dynamic current consumption:

 I_{CC} (Total) = I_{CC} (Static) + (C_{PD} + nCL) $\frac{1}{2}$, where f is the clock frequency, CL output load capacitance, and n number of loads.



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SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified $(T_A = 0 \text{ to } +70^{\circ}\text{C}, \ V_{CC} = 4.5 \text{ to } 5.5 \text{ V}, \ C_L = 50 \text{ pF})$

Am29C116

A. Combinational Delays (nsec)

	Outputs							
Input	Y ₀₋₁₅	T ₁₋₄	СТ					
I ₀₋₄ (ADDR)	79	84	-					
I ₀₋₁₅ (DATA)	79	84	-					
I ₀₋₁₅ (INSTR)	79	84	48					
DLE	58*	60	.					
T ₁₋₄	-	-	39					
CP	63	66	40					
Y0 - 15	62*	64	-					
IEN	-	-	43					

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

		Ena	ble	Dis	able
From Input	To Output	tpzH tpzL		tpHZ	tpLZ
ŌĒY	Y0 - 15	22	22	22	22
OET	T1-4	25	25	25	25

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	20	30
DLE	-	15
IEN	22	_

D. Setup and Hold Times (nsec)

Input	With Respect to	HIGH-to-LOW Trans Ition Setup Hold			LOW-to-HIGH Transition Setup Hold				Comment					
IO-4 (RAM ADDR)	CP	CP (t _{S1}) 24 (t _{h1}) 0 -		CP (t _{s1}) 24 (t _{h1}) 0 -		CP (t _{S1}) 24		(t _{s1}) 24 (t _{h1}) 0			-		Single Al (Source)	DDR
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(1	(t _{s2}) 5		-	-		(th7) 2		Two ADDR (Destination)				
IO-15 (DATA)	CP	i Hindi	-		(t _{st}		(t _{s8})	65	(th8) 0					
I ₀₋₁₅ (INSTR)	CP	(t _{s3}) 38		(t _{s3}) 38		(th:	3) 17	(t _{s9})	65	(th9) 2				
IEN HIGH	CP	(t ₁	(t _{s4}) 10 -		- (t _{h10}) 2		2	Disable						
IEN LOW	СР	-	(t _{\$5}) 20	_	(t _{h5}) 1	(l _{s11}) 22	-	(th11) 1**	(t _{h11}) 1** -		Immediate first cycle			
SRE	CP						-	(t _{s12}) 17		(th12) 0			-	
Υ	CP			(t _{s13}) 44		(th13) 0								
Y	DLE	(t _{s6}) 10 (t _{h6}) 6		-		_								
DLE	CP		-	77.00	_	(t _{s14}) 45 (t _{h14}) 0		0						

^{**} Status register and accumulator destination only.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Cont'd.)

Am29C116-1

A. Combinational Delays (nsec)

	Outputs							
Input	Y0-15	T1-4	СТ					
I ₀₋₄ (ADDR)	65	73	_					
I _{0 - 15} (DATA)	65	73	-					
10 - 15 (INSTR)	65	73	30					
DLE	55*	55	-					
T ₁₋₄	-	-	27					
CP	60	66	37					
Y _{0 - 15}	53*	53	-					
IEN	-	-	25					

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

		Ena	able	Disable			
From Input	m Input To Output		om Input To Output tpzH t				tpLZ
ŌĒY	Yo - 15	22	22	22	22		
OET	T ₁₋₄	22	22	22	22		

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	20	30
DLE	-	15
IEN	20	-

D. Setup and Hold Times (nsec)

Input	With Respect to						LOW-to-HIGH Transition Setup Hold			d	Comment								
I ₀₋₄ (RAM ADDR)	СР	(t _s	(t _{s1}) 13				-		-		Single Al (Source)	DDR							
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(t	(t _{s2}) 5		-	-		(t _{h7}) 0		Two ADDR (Destination)									
I ₀₋₁₅ (DATA)	CP		-				(t _{s8}) (g) 60 (th8) 0		0									
10-15 (INSTR)	CP	(ts	(t _{s3}) 24		(t _{s3}) 24		(t _{s3}) 24		(t _{s3}) 24 ((t _{s3}) 24 (t _{h3}) 12		3) 12	(t _{s9}) (60	(th9) 0		1	
IEN HIGH	CP	(t	s4) 5			(th10) 2		Disable											
IEN LOW	СР	-	(t _{s5}) 5	-	(t _{h5}) 1	(t _{s11}) 10	(t _{s11}) 10 -		-	Enable	Immediate first cycle								
SRE	CP		-	-				-		(t _{s12})	12	(th12)	0	1					
Y	CP				(t _{s13}) 42 (t _{h13}) 0		0												
Y	DLE	(t	(t _{s6}) 6 (t _{h6}) 5																
DLE	CP		-	-		(t _{S14})	43	(th14)	0										

** Status register and accumulator destination only.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range

Am29C116-2

A. Combinational Delays (nsec)

	Outputs							
Input	Y0-15	T1-4	СТ					
lo-4 (ADDR)	57	60						
I _{0 - 15} (DATA)	57	60	-					
I ₀₋₁₅ (INSTR)	57	60	25					
DLE	45*	45	-					
T ₁₋₄	-	-	25					
CP	50	55	29					
Yo - 15	45*	45	-					
ĪĒN	-	-	25					

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

		Enabl		Dis	able
From Input	To Output	tpzH	tpzL	tpHZ	tPLZ
ŌĒY	Y0-15	22	22	22	22
OET	T ₁₋₄	22	22	22	22

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	20	30
DLE	-	15
IEN	20	-

D. Setup and Hold Times (nsec)

Input	With Respect to		HIGH-t Trans Setup	sition	old	Setu	Tra	to-HIGH sition Hold		nsition		Co	mment
I ₀₋₄ (RAM ADDR)	СР	(t	s1) 13	(t _{h1}) 0		-		-		Single Al (Source)	DDR		
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(1	l _{s2}) 5		-	-		(t _{h7}) 0		Two ADD			
I _{0 - 15} (DATA)	CP		-		-	(t _{s8})	50	(th8) 0					
I _{0 - 15} (INSTR)	CP	(t	s3) 22	(tha) 10	(t _{s9}) 50		(th9) 0					
IEN HIGH	CP	(1	s ₄) 5		-	-	- (1) 2	Disable			
IEN LOW	CP	-	(t _{S5}) 5	-	(t _{h5}) 1	(t _{s11}) 10	-	(t _{h11}) 1**	-	Enable	Immediate first cycle		
SRE	CP	į.	-		-	(t _{s12})	12	(th12	0		10000000		
Y	CP		-		-	(t _{s13})	39	(th13	0 (12.5		
Y	DLE	(1	l _{s6}) 6	(th	6) 5	-		-					
DLE	CP				-	(t _{s14})	43	(th14	0				

^{**} Status register and accumulator destination only.

SWITCHING CHARACTERISTICS over MILITARY operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) ($T_A = -55$ to +125°C, $V_{CC} = 4.5$ to 5.5 V, $C_L = 50$ pF).

Am29C116

A. Combinational Delays (nsec)

		Outputs	
Input	Y ₀₋₁₅	T1-4	СТ
I ₀₋₄ (ADDR)	100	103	- 8
I _{0 - 15} (DATA)	100	103	-
10-15 (INSTR)	100	103	50
DLE	68*†	70	-
T ₁₋₄	-	-	46
CP	76	83	48
Y ₀₋₁₅	70°†	72	-
IEN	-	-	50

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

		Ena	able	Dis	able
From Input	To Output	tpzH	tpzL	tpHZ	tpLZ
ŌĒŸ	Y0 - 15	25	25	25	25
OET	T1-4	30	30	30	30

C. Clock and Pulse Requirements (nsec)

	Input	Min. LOW Time	Min. HIGH Time
1	CP	33	50
1	DLE	-	20
1	IEN	33	-

D. Setup and Hold Times (nsec)

Input	With Respect to	,	HIGH-to Trans Setup	ition	old	Setu	Trai			/-to-HIGH ansition Hold		insition		Co	mment
I ₀₋₄ (RAM ADDR)	СР	(t	(t _{s1}) 24		(t _{h1}) 1		-			Single Al (Source)	ODR				
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(t	_{S2}) 10		-	-		(t _{h7})	(t _{h7}) 3		OR on)				
10-15 (DATA)	CP		(t ₈₈) 78 (t _{h8}) 3		3										
I ₀₋₁₅ (INSTR)	CP	(t	(t _{s3}) 57 (t _{h3}) 1		(t _{s3}) 57	3) 17	(t _{s9})	(t _{s9}) 78 (t _{h9}) 3		3					
IEN HIGH	CP	(t	s4) 10		-	-	-		2	Disable	5(2) 1815; 4 1925;				
IEN LOW	CP	-	(t _{s5}) 20	-	(th5) 3	(t _{S11}) 28	-	(th11) 3**	-	Enable	Immediate first cycle				
SRE	CP					(t _{s12})	19	(th12) 1						
Y	СР	-				(t _{s13})	53	(th13) 2						
Y	DLE	(t	(t _{s6}) 11 (t _{h6}) 7		-		-								
DLE	CP		-				(t _{s14})	54	(th14	0 (

**Status register and accumulator destination only.

[†] Not included in Group A tests.

SWITCHING CHARACTERISTICS over MILITARY operating range (Cont'd.)

Am29C116-1

A. Combinational Delays (nsec)

	Outputs							
Input	Y0 - 15	T1-4	СТ					
I ₀₋₄ (ADDR)	75	75						
I _{0 - 15} (DATA)	75	75	-					
I ₀₋₁₅ (INSTR)	75	75	29					
DLE	62*†	62						
T ₁₋₄	-	-	29					
CP	67	75	39					
Y _{0 - 15}	60*†	60	-					
IEN	-	-	29					

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

		Enable		Dis	able
From Input	To Output	tpzH	tpzL	tpHZ	tpLZ
ŌĒY	Y0 - 15	25	25	20	20
OET	T1-4	25	25	16	16

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	25	15
DLE	-	15
ĪĒN	15	_

D. Setup and Hold Times (nsec)

Input	With Respect to			o-LOW sition H	old	Setu	Tra	to-HIGH nsition Hol	d	Co	mment
I ₀₋₄ (RAM ADDR)	СР	(t,	(t _{s1}) 12		(t _{h1}) 1		-			Single Al (Source)	DDR
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(1	t _{s2}) 7		-	-	Fig. 11	(t _{h7}) 0		Two ADD	
I ₀₋₁₅ (DATA)	CP				- (t _{s8}) 65 (t _{h8}) 0		(th8) 0				
I ₀₋₁₅ (INSTR)	CP	(t	s3) 27	(th	3) 12	(t _{s9}) 65		(t _{h9})	2		
IEN HIGH	CP	(1	t _{s4}) 5	Marketon years of the Land	-	-	ye.	(th10)	2	Disable	
IEN LOW	CP	_	(t _{s5}) 7	_	(t _{h5}) 3	(t _{s11}) 12	12	(t _{h11}) 3**	2	Enable	Immediate first cycle
SRE	CP	(t _{s12}) 12 (t _{h12}) 1		3							
Y	CP	770		-		(t _{s13}) 53		(th13)	0		
Υ	DLE	(1	t _{s6}) 7	(t _h	6) 3	-	207	-			
DLE	CP		-		-	(t _{s14})	54	(th14)	0		

^{**}Status register and accumulator destination only.

[†] Not included in Group A tests.

SWITCHING CHARACTERISTICS over MILITARY operating range (Cont'd.)

Am29C116-2

A. Combinational Delays (nsec)

	Outputs					
Input	Y ₀₋₁₅	T1-4	СТ			
I ₀₋₄ (ADDR)	65	65	_			
I ₀₋₁₅ (DATA)	65	65	-			
lo-15 (INSTR)	65	65	26			
DLE	52*†	52	-			
T ₁₋₄	-	-	26			
CP	57	65	33			
Y _{0 - 15}	52*†	52	-			
IEN	_		26			

 Y_{0-15} must be stored in the Data Latch and its source disabled before the delay to Y_{0-15} as an output can be measured. *Guaranteed indirectly by other tests.

B. Enable/Disable Times (nsec) (Disable: C_L = 5 pF, 0.5-V Change on Outputs)

From Input		Ena	able	Disable		
	To Output	tpzH	tpZL	tpHZ	tpLZ	
ŌĒY	Y ₀₋₁₅	22	22	18	18	
OET	T ₁₋₄	22	22	15	15	

C. Clock and Pulse Requirements (nsec)

Input	Min. LOW Time	Min. HIGH Time
CP	20	15
DLE	-	15
IEN	15	-

D. Setup and Hold Times (nsec)

Input With Respec		8	HIGH-t Trans Setup	0.377(276)257(1)		LOW-to-H Transiti Setup		nsition			Comment				
I ₀₋₄ (RAM ADDR)	CP	(t _{s1}) 12		(t _{s1}) 12		CP (t _{s1}) 12		CP (t _{s1}) 12 (t _{h1})	1) 1	-		-		Single ADDR (Source)	
I ₀₋₄ (RAM ADDR)	CP and IEN both LOW	(t _{s2}) 7		<u>=</u>		- (t _h		(t _{h7})	(th7) 0 Two ADDR (Destination)						
I ₀₋₁₅ (DATA)	CP					(t _{s8}) 56		(th8) 0							
I ₀₋₁₅ (INSTR)	CP	(t _{s3}) 25		(t _{s3}) 25 (t _{h3}) 12		(t _{s9}) 56 (t _{h9}) 2		2							
IEN HIGH	CP	(t _{S4}) 5		(t _{s4}) 5 -		-		(th10) 2		Disable					
IEN LOW	CP		(t _{s5}) 7	-	(t _{h5}) 3	(t _{s11}) 10	-	(th11) 3**	-	Enable	Immediate first cycle				
SRE	CP	- '-				(t _{s12}) 10		(th12) 1							
Y	СР	-		-		(t _{s13}) 45		(th13	0		20162				
Y	DLE	(1	(t _{s6}) 7 (t _{h6}) 3					10							
DLE	CP				(t _{s14}) 46 (t _{h14}) 0			23.7							

**Status register and accumulator destination only.

[†] Not included in Group A tests.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown in the data sheet.

- Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
- Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
- 3. Do not attempt to perform threshold tests at high speed. Following an output transition, ground current may change by as much as 400 mA in 5-8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily. Current level may vary from product to product.
- 4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins that may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.
- To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests
- 6. Capacitive Loading for AC Testing

Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench set up are used to predict the result at the lower capacitance.

Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at <u>both</u> capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within specification. In some cases, special DC tests are performed in order to facilitate this correlation.

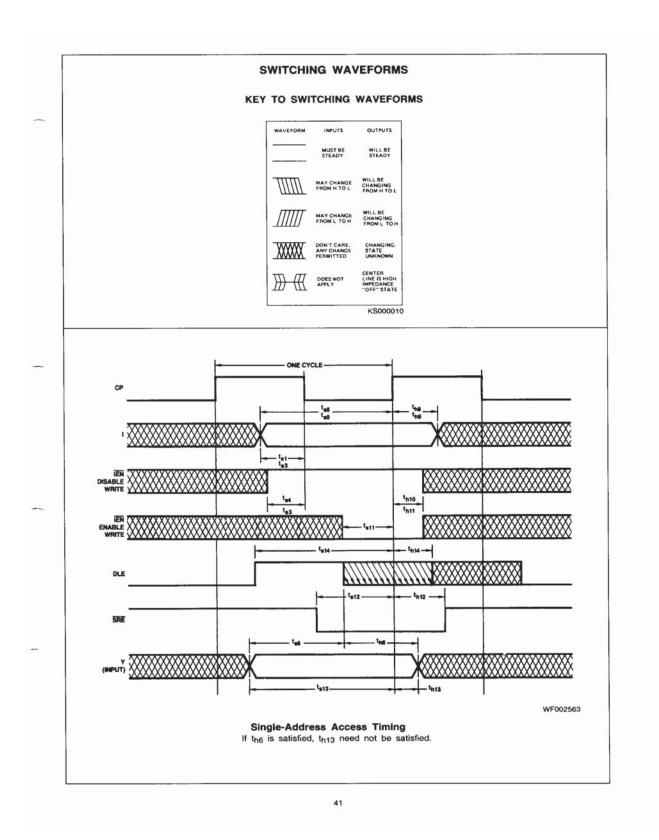
7. Threshold Testing

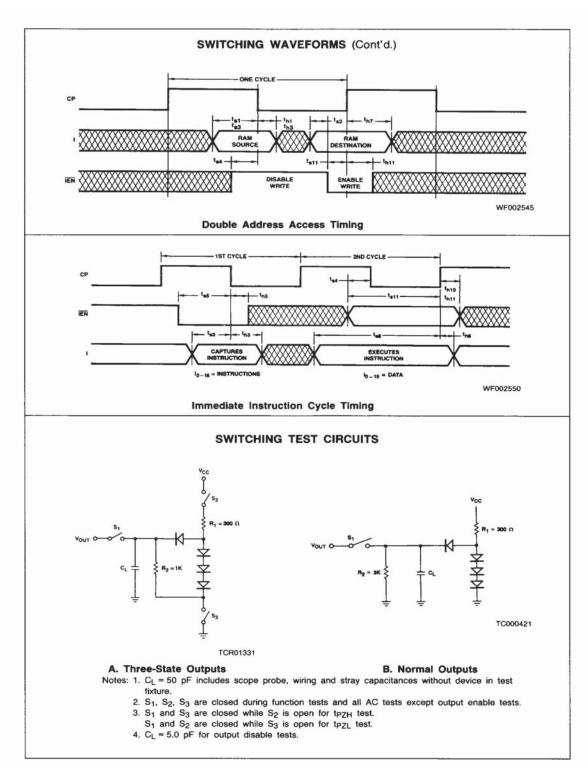
The noise associated with automatic testing (due to the long inductive cables), and the high gain of the tested device when in the vicinity of the actual device threshold, frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for $\underline{\text{each}}$ input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at $V_{\rm IL}$ Max. and $V_{\rm IH}$ Min.

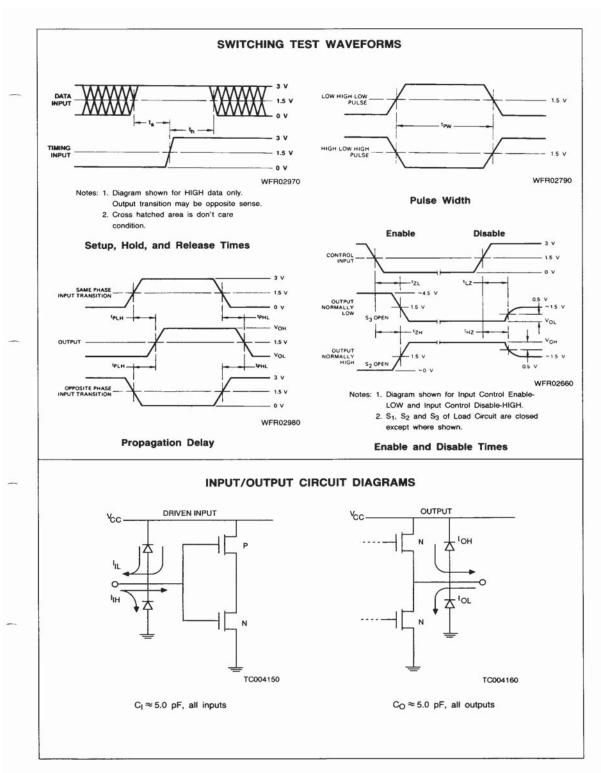
8. AC Testing

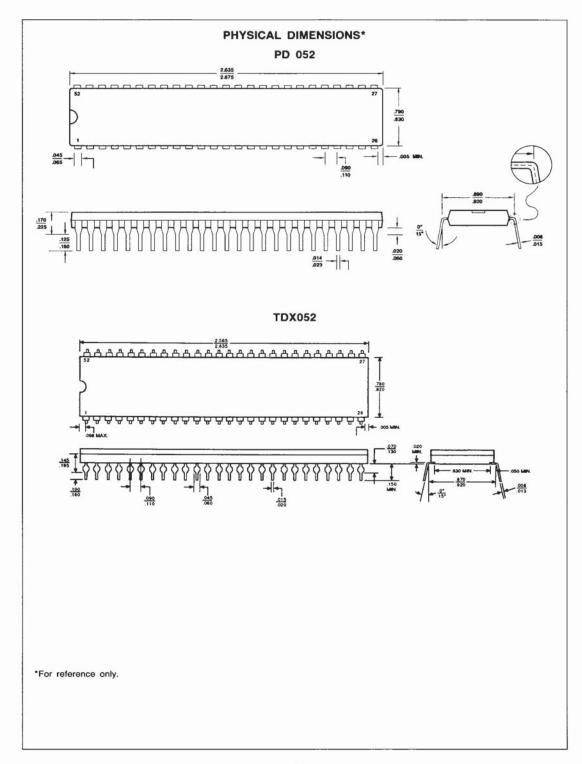
Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

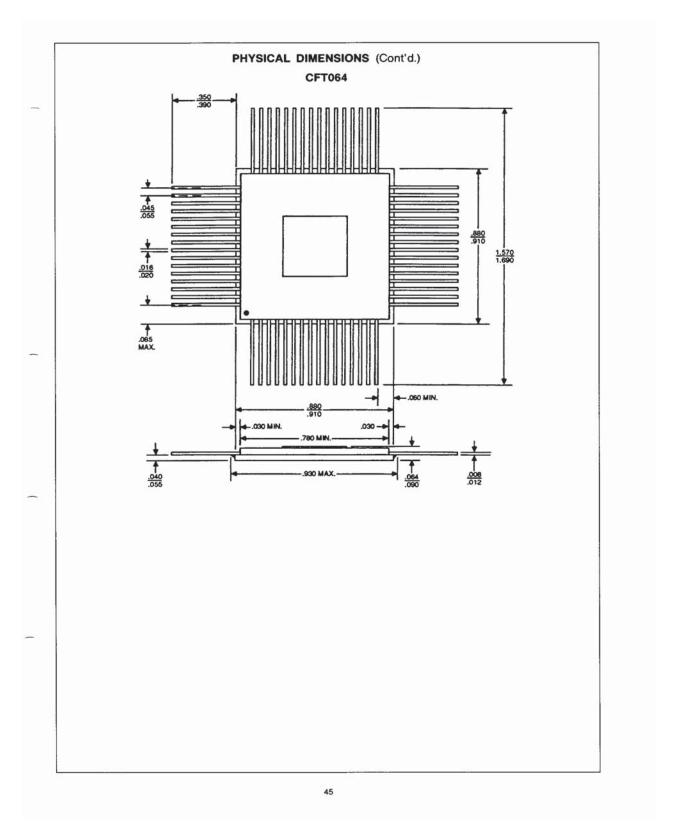
In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.



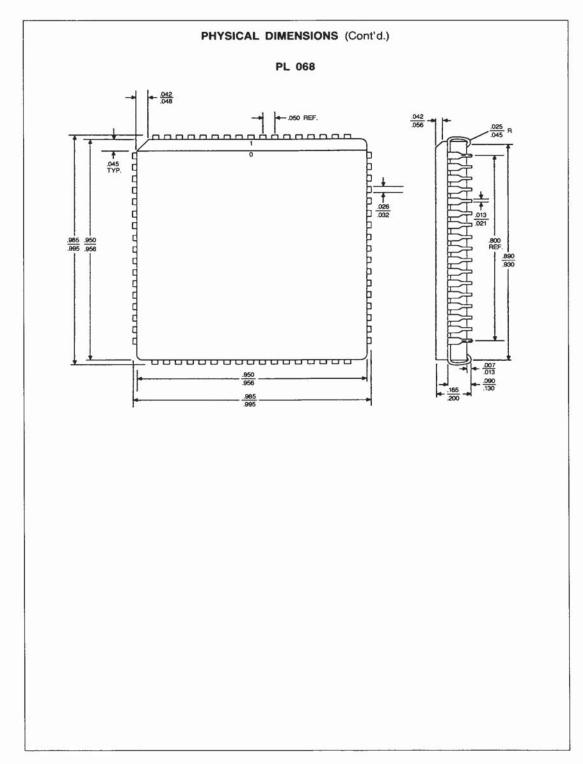


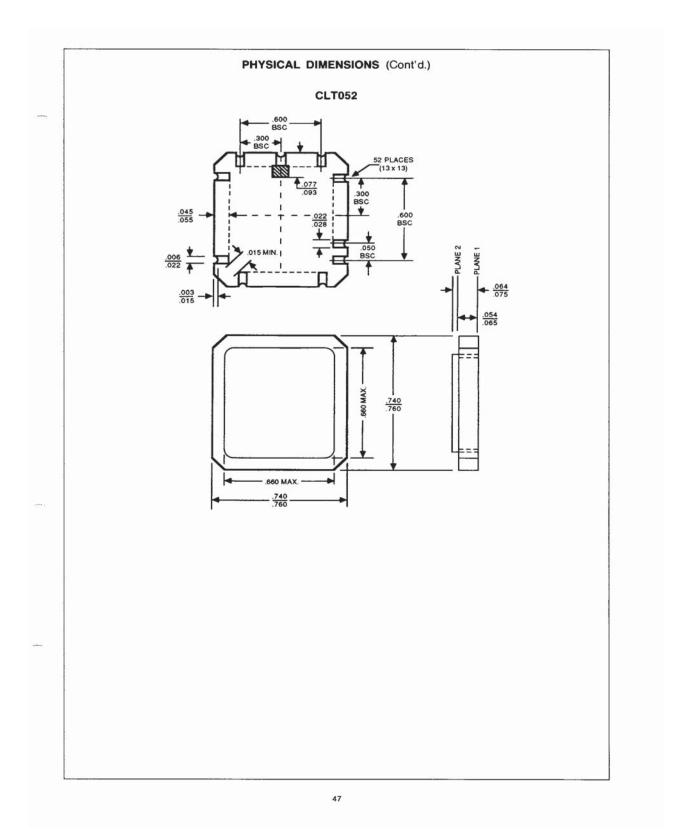






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