Rochester Electronics

Datasheet

PART NUMBER

5493ADM-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

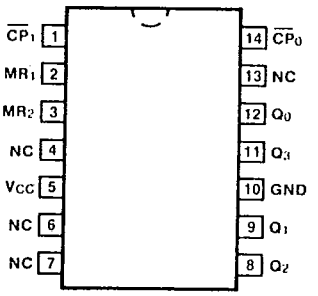
- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

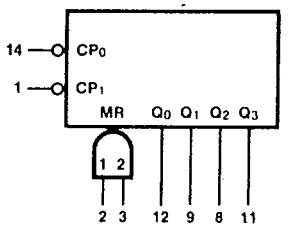
54/7493A
54LS/74LS93
DIVIDE-BY-SIXTEEN COUNTER

CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '93 is a 4-stage ripple counter containing a high speed flip-flop acting as a divide-by-two and three flip-flops connected as a divide-by-eight. HIGH signals on the Master Reset (MR) inputs override the clocks and force all outputs to the LOW state.

LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7493APC, 74LS93PC		9A
Ceramic DIP (D)	A	7493ADC, 74LS93DC	5493ADM, 54LS93DM	6A
Flatpak (F)	A	7493AFC, 74LS93FC	5493AFM, 54LS93FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{CP}_0$	÷2 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.5
$\overline{CP}_1$	÷5 Section Clock Input (Active Falling Edge)	2.0/2.0	1.0/1.0
MR_1, MR_2	Asynchronous Master Reset Inputs (Active HIGH)	1.0/1.0	0.5/0.25
Q_0	÷2 Section Output*	20/10	10/5.0 (2.5)
Q_1 — Q_3	÷8 Section Outputs	20/10	10/5.0 (2.5)

*The Q_0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP}_1$ input.

FUNCTIONAL DESCRIPTION — The '93 is a 4-bit ripple type binary counter. It consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device. A gated AND asynchronous Master Reset (MR_1, MR_2) is provided which overrides the clocks and resets (clears) all the flip-flops. Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the Truth Table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

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MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

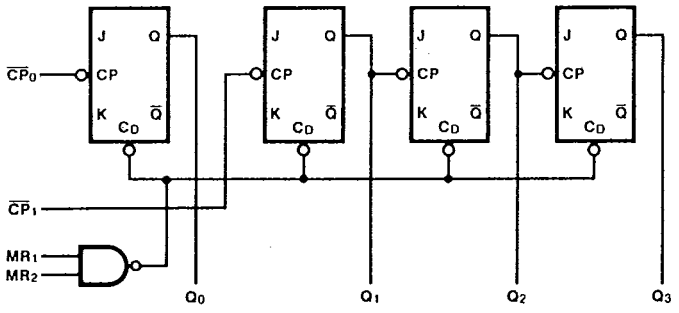
H = HIGH Voltage Level
L = LOW Voltage Level

TRUTH TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 connected to $\overline{CP}_1$.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
I_{IH}	Input HIGH Current $\overline{CP_0}$ or $\overline{CP_1}$		1.0		0.2	mA	V_{CC} = Max, V_{IN} = 5.5 V
I_{CC}	Power Supply Current		39		15	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74 C_L = 15 pF, R_L = 400 Ω		54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max	Min	Max		
f_{max}	Maximum Count Frequency $\overline{CP_0}$ Input	32		32		MHz	Figs. 3-1, 3-9
f_{max}	Maximum Count Frequency $\overline{CP_1}$ Input	16		16		MHz	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_0		16 18		16 18	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_0}$ to Q_3		70 70		70 70	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_1		16 21		16 21	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_2		32 35		32 35	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP_1}$ to Q_3		51 51		51 51	ns	Figs. 3-1, 3-9
t_{PHL}	Propagation Delay MR to Q_n		40		40	ns	Figs. 3-1, 3-17

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
t_w (H)	$\overline{CP_0}$ Pulse Width HIGH	15		15		ns	Fig. 3-9
t_w (H)	$\overline{CP_1}$ Pulse Width HIGH	30		30		ns	Fig. 3-9
t_w (H)	MR Pulse Width HIGH	15		15		ns	Fig. 3-17
t_{rec}	Recovery Time, MR to $\overline{CP}$	25		25		ns	Fig. 3-17