Latch/Flip-Flops

54F573, 54F574

FEATURES

- 54F573 is broadside pinout version of 54F373
- 54F574 is broadside pinout version of 54F374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing
- Common Output Enable

DESCRIPTION

The 54F573 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The 54F573 is functionally identical to the 54F373 but has broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs is transferred to the latch outputs when the Enable (E) input is High. The latch remains transparent to the data input while E is High and stores the data that is present one set-up time before the High-to-Low enable transition.

The 54F574 is functionally identical to the 54F374 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

It is a 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is full edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Ouput Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54F573/BRA, 54F574/BRA	GDIP1-T20
20-Pin Ceramic FlatPack	54F573/BSA, 54F574/BSA	DGFP2-F20
20-Pin Ceramic LLCC	54F573/B2A, 54F574/B2A	CQCC2-N20

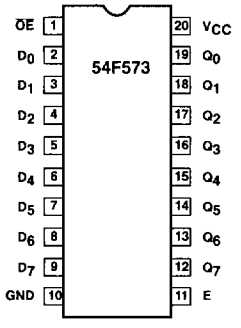
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

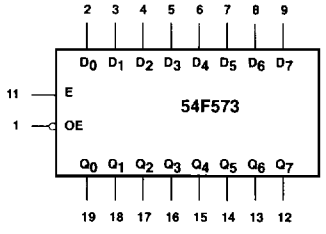
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_7	Data inputs	1.0/1.0	20μA/0.6mA
E (54F573)	Latch enable input (active High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
CP (54F574)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q_0 - Q_7	3-State outputs	50/33.3	3.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

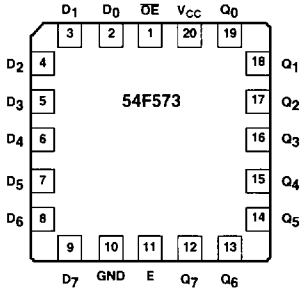
PIN CONFIGURATION



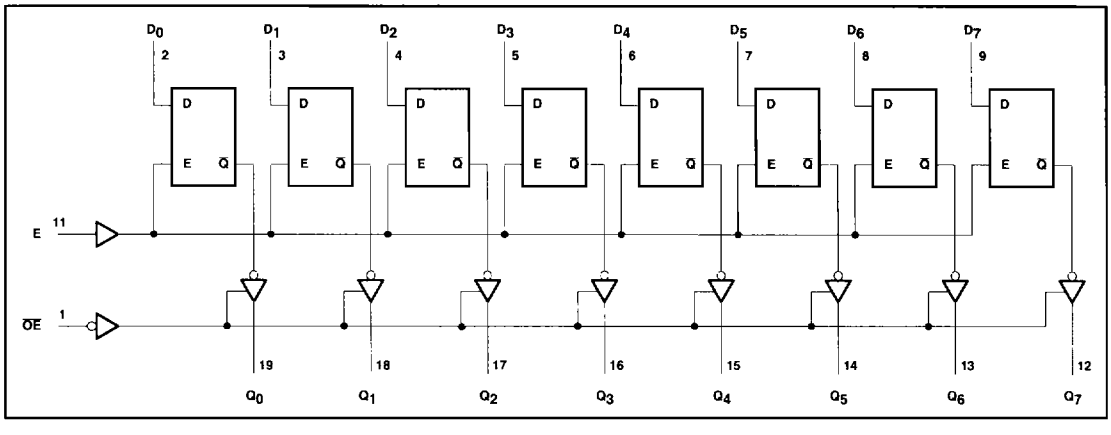
LOGIC SYMBOL



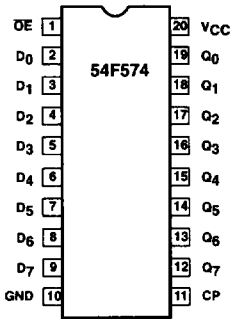
LLCC LEAD CONFIGURATION



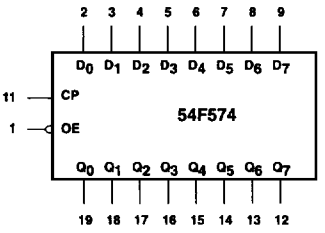
LOGIC DIAGRAM, 54F573



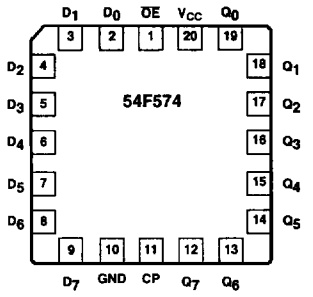
PIN CONFIGURATION



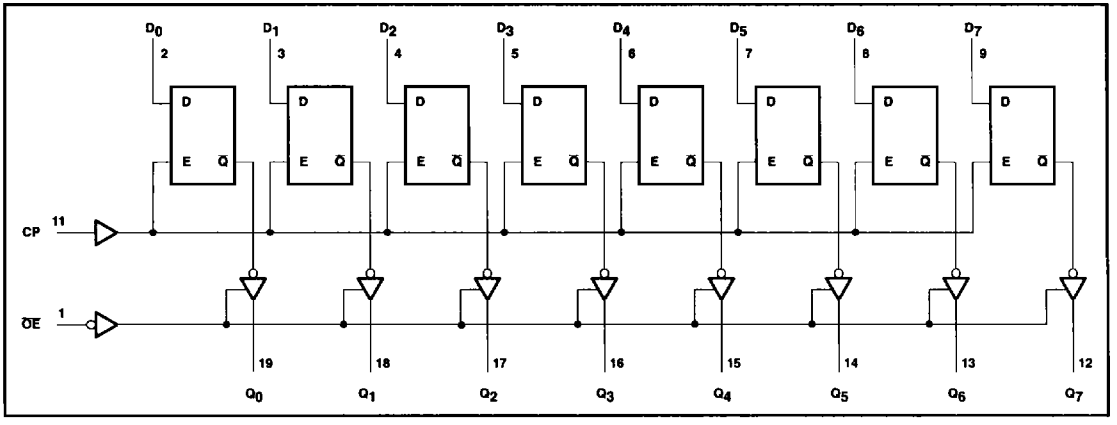
LOGIC SYMBOL



LLCC LEAD CONFIGURATION



LOGIC DIAGRAM, 54F574



FUNCTION TABLE, 54F573

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D	REGISTER	Q_0 - Q_7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D_n	D_n	Z	

H = High voltage level
h = High voltage one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

FUNCTION TABLE, 54F574

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↥	X	NC	NC	Hold
H	↑	D_n	D_n	Z	Disable outputs
H	X	X	X	Z	

H = High voltage level
h = High voltage one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↥ = Not a Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-3	mA
I_{OH2}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS[1]		LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage			V_{CC} = Min, V_{IL} = Max,	I_{OH1}	2.4			V
				V_{IH} = Min	I_{OH2}	2.5	3.4		V
V_{OL}	Low-level output voltage			V_{CC} = Min, V_{IL} = Max , V_{IH} = Min, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage			V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage			V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current			V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current			V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OZH}	Off-state output current, High-level voltage applied			V_{CC} = Max, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, High-level voltage applied			V_{CC} = Max, V_O = 0.5V				-50	µA
I_{OS}	Short-circuit output current[3]			V_{CC} = Max		-60		-150	mA
I_{CC}	Supply current (total)	I_{CCH}	'F573	V_{CC} = Max			30	40	mA
		I_{CCL}					35	50	mA
		I_{CCZ}					40	60	mA
		I_{CCH}	'F574	V_{CC} = Max			45	65	mA
		I_{CCL}					50	70	mA
		I_{CCZ}					55	90	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	'F573	Waveform 2	3.0 1.2	5.5 3.5	8.0 6.0	2.5 1.0	9.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	'F573	Waveform 1	4.5 3.0	8.5 5.0	11.5 7.0	6.0 2.5	13.5 8.0	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F573	Waveform 4 Waveform 5	2.5 2.5	5.5 5.5	9.5 8.0	2.0 2.0	11.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	'F573	Waveform 4 Waveform 5	1.2 1.2	3.0 2.5	6.0 5.5	1.0 1.0	7.0 5.5	ns ns
f_{MAX}	Maximum Clock frequency	'F574	Waveform 1	110	125		100[4]		ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	'F574	Waveform 1	4.0 4.0	5.5 6.0	8.5 8.5	3.0 3.0	9.5 9.5	ns ns
t_{PZH} t_{PZL}	Output Enable time to High or Low level	'F574	Waveform 4 Waveform 5	2.5 3.0	4.5 6.0	8.0 8.5	2.0 3.0	9.0 9.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time to High or Low level	'F574	Waveform 4 Waveform 5	1.0 1.0	3.0 2.5	6.0 5.5	1.0 1.0	7.0 6.0	ns ns

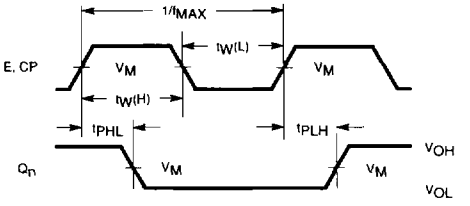
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Set-up time D_n to E	'F573	Waveform 3	0.0 0.0			0.0 1.0		ns ns
t_h(H) t_h(L)	Hold time D_n to E	'F573	Waveform 3	2.5 4.0			3.0 5.0		ns ns
t_w(H) t_w(L)	E Pulse width, High or Low	'F573	Waveform 1	4.0 4.0			4.0 4.0		ns ns
t_s(H) t_s(L)	Set-up time D_n to CP	'F574	Waveform 3	2.0 2.0			2.5 2.5		ns ns
t_h(H) t_h(L)	Hold time D_n to CP	'F574	Waveform 3	1.5 1.5			2.0 2.0		ns ns
t_w(H) t_w(L)	CP Pulse width, High or Low	'F574	Waveform 1	3.0 4.5			3.0 4.5		ns ns

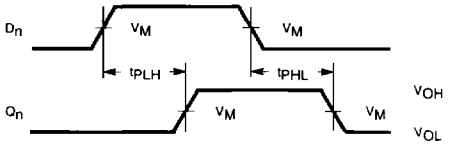
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. This parameter is guaranteed, but not tested.

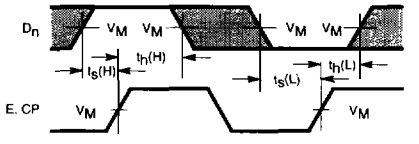
AC WAVEFORMS



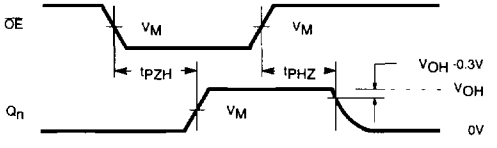
Waveform 1. Propagation Delay, Clock and Enable Inputs to Output, Enable and Clock Pulse Widths and Maximum Clock Frequency



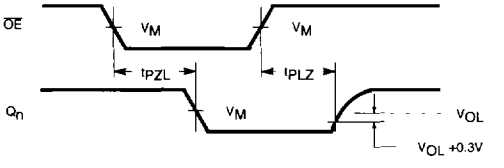
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



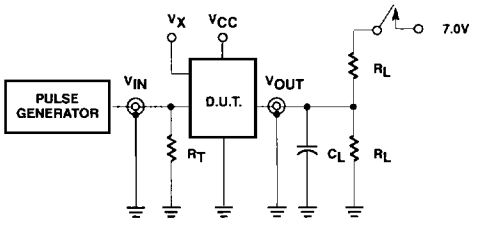
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



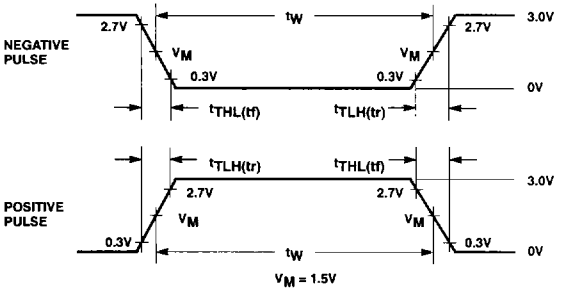
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE For all waveforms, V_M = 1.5V
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**t_W**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per Function Table.