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**PART NUMBER****54H72JB-ROCV**

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**Rochester Electronics  
Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

**Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

**Qualified Suppliers List of Distributors (QSLD)**

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

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*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

## **SN5472, 54L72, 54H72, 7472**

### ***AND-Gated J-K Master-Slave Flip-Flops with Preset and Clear***

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave

Logical state of J and K inputs must not be allowed to change when the clock pulse is in a high state. The SN5472, SN54H72, and the SN54L72 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7472 is characterized for operation from 0°C to 70°C.

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#### **FOR REFERENCE ONLY**

# TYPES SN5472, SN54H72, SN54L72, SN7472, SN74H72 AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

REVISED DECEMBER 1983

- Package Options Include Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

## description

These J-K flip-flops are based on the master-slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

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The SN5472, SN54H72, and the SN54L72 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN7472 and the SN74H72 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

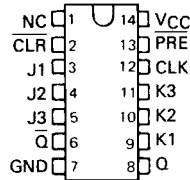
FUNCTION TABLE

| INPUTS |     |              |   |   | OUTPUTS        |                |
|--------|-----|--------------|---|---|----------------|----------------|
| PRE    | CLR | CLK          | J | K | Q              | $\bar{Q}$      |
| L      | H   | X            | X | X | H              | L              |
| H      | L   | X            | X | X | L              | H              |
| L      | L   | X            | X | X | H <sup>†</sup> | H <sup>†</sup> |
| H      | H   | $\downarrow$ | L | L | Q <sub>0</sub> | $\bar{Q}_0$    |
| H      | H   | $\downarrow$ | H | L | H              | L              |
| H      | H   | $\downarrow$ | L | H | L              | H              |
| H      | H   | $\downarrow$ | H | H | TOGGLE         |                |

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

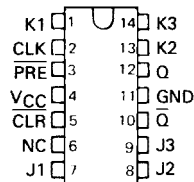
SN5472, SN54H72, SN54L72 ... J PACKAGE  
SN7472, SN74H72 ... J OR N PACKAGE

(TOP VIEW)



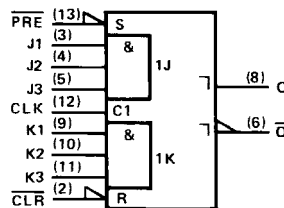
SN5472, SN54H72 ... W PACKAGE

(TOP VIEW)



NC - No internal connection

## logic symbol



Pin numbers shown are for J and N packages.

## positive logic

$$J = J1 \cdot J2 \cdot J3$$

$$K = K1 \cdot K2 \cdot K3$$

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## PRODUCTION DATA

This document contains information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

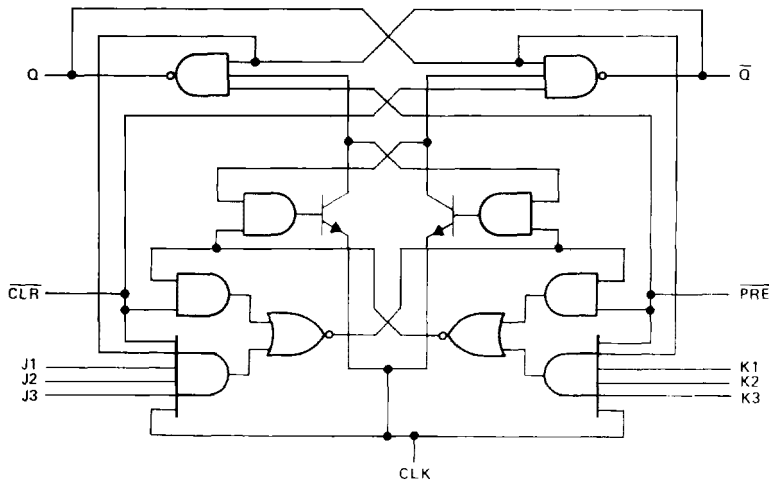
TEXAS  
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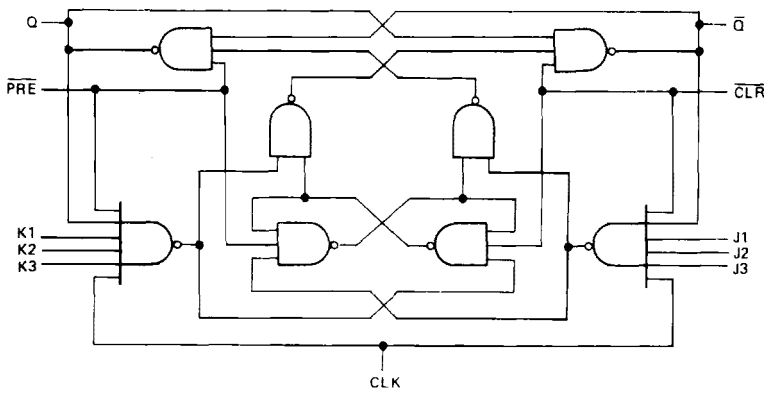
3-279

**TYPES SN5472, SN54H72, SN54L72,  
SN7472, SN74H72  
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR**

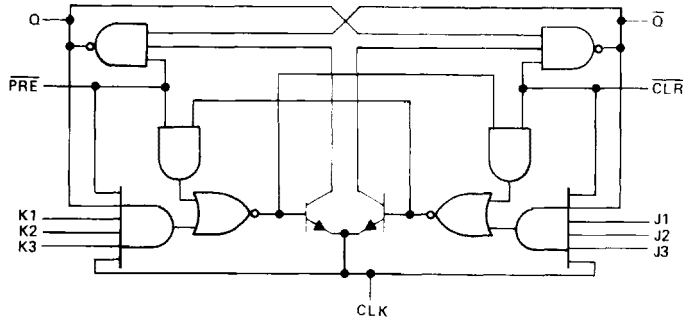
logic diagrams  
'72



'H72

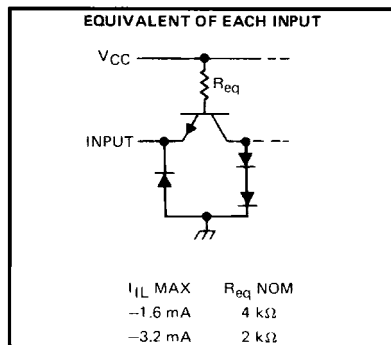


'L72

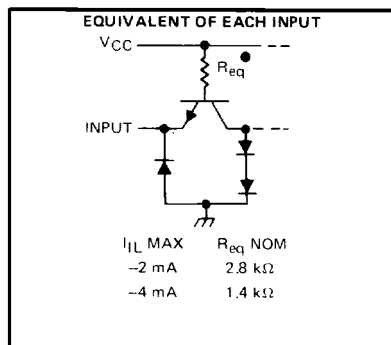
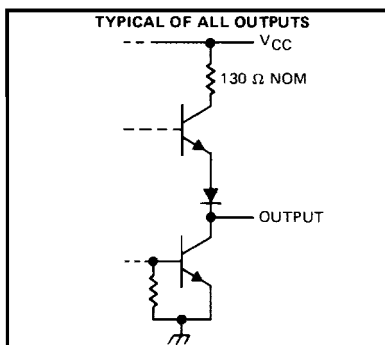


TYPES SN5472, SN54H72, SN54L72,  
SN7472, SN74H72  
**AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR**

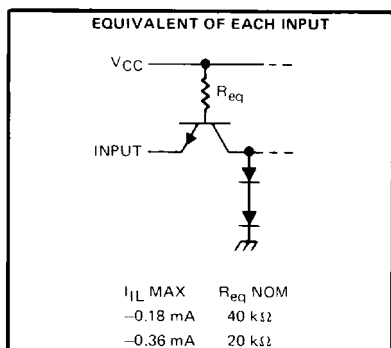
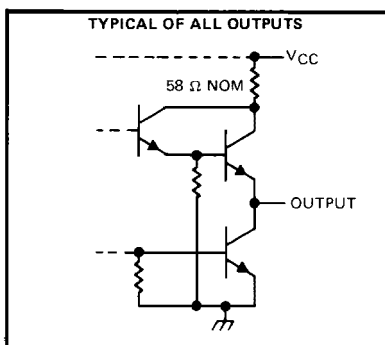
schematics of inputs and outputs



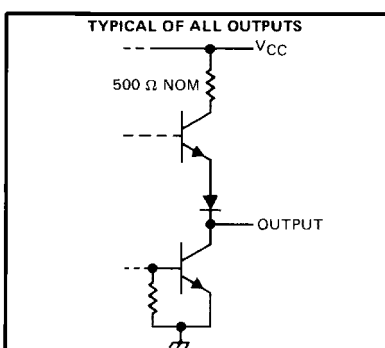
'72



'H72



'L72



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TTL DEVICES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|                                       |                |
|---------------------------------------|----------------|
| Supply voltage, $V_{CC}$ (see Note 1) | 7 V            |
| Input voltage                         | 5.5 V          |
| Operating free-air temperature: SN54' | -55°C to 125°C |
| SN74'                                 | 0°C to 70°C    |
| Storage temperature range             | -65°C to 150°C |

NOTE 1: Voltage values are with respect to network ground terminal.

# TYPES SN5472, SN7472

## AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

### recommended operating conditions

|                 |                                  | SN5472     |     |       | SN7472 |     |       | UNIT |    |    |
|-----------------|----------------------------------|------------|-----|-------|--------|-----|-------|------|----|----|
|                 |                                  | MIN        | NOM | MAX   | MIN    | NOM | MAX   |      |    |    |
| V <sub>CC</sub> | Supply voltage                   | 4.5        | 5   | 5.5   | 4.75   | 5   | 5.25  | V    |    |    |
| V <sub>IH</sub> | High-level input voltage         | 2          |     |       | 2      |     |       | V    |    |    |
| V <sub>IL</sub> | Low-level input voltage          |            |     | 0.8   |        |     | 0.8   | V    |    |    |
| I <sub>OH</sub> | High-level output current        |            |     | − 0.4 |        |     | − 0.4 | mA   |    |    |
| I <sub>OL</sub> | Low-level output current         |            |     | 16    |        |     | 16    | mA   |    |    |
| t <sub>w</sub>  | Pulse duration                   | CLK high   |     |       | 20     |     |       | ns   |    |    |
|                 |                                  | CLK low    |     |       | 47     |     |       |      |    |    |
|                 |                                  | PRE or CLR |     |       | 25     |     |       |      |    |    |
| t <sub>su</sub> | Input setup time before CLK †    | 0          |     |       | 0      |     |       | ns   |    |    |
| t <sub>h</sub>  | Input hold time-data after CLK † | 0          |     |       | 0      |     |       | ns   |    |    |
| T <sub>A</sub>  | Operating free-air temperature   | − 55       |     |       | 125    |     |       | 0    | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |           | TEST CONDITIONS †                                                                             |  |  | SN5472 |      |      | SN7472 |      |      | UNIT          |
|-----------|-----------|-----------------------------------------------------------------------------------------------|--|--|--------|------|------|--------|------|------|---------------|
|           |           |                                                                                               |  |  | MIN    | TYP‡ | MAX  | MIN    | TYP‡ | MAX  |               |
| $V_{IK}$  |           | $V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$                                                   |  |  | -1.5   |      |      | -1.5   |      |      | V             |
| $V_{OH}$  |           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$ |  |  | 2.4    | 3.4  |      | 2.4    | 3.4  |      | V             |
| $V_{OL}$  |           | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$   |  |  |        | 0.2  | 0.4  |        | 0.2  | 0.4  | V             |
| $I_I$     |           | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                    |  |  |        |      | 1    |        |      | 1    | mA            |
| $I_{IH}$  | J or K    | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$                                                    |  |  |        |      | 40   |        |      | 40   | $\mu\text{A}$ |
|           | All other |                                                                                               |  |  |        |      | 80   |        |      | 80   |               |
| $I_{IL}$  | J or K    | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$                                                    |  |  |        |      | -1.6 |        |      | -1.6 | mA            |
|           | All other |                                                                                               |  |  |        |      | -3.2 |        |      | -3.2 |               |
| $I_{OS}§$ |           | $V_{CC} = \text{MAX}$                                                                         |  |  | 20     |      | -57  | -18    |      | -57  | mA            |
| $I_{CC}$  |           | $V_{CC} = \text{MAX}, \text{ See Note 2}$                                                     |  |  | 10     | 20   |      | 10     | 20   |      | mA            |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

§ Not more than one output should be shorted at a time.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER        | FROM<br>(INPUT)                                    | TO<br>(OUTPUT)             | TEST CONDITIONS                                |  | MIN | TYP | MAX | UNIT |
|------------------|----------------------------------------------------|----------------------------|------------------------------------------------|--|-----|-----|-----|------|
| $f_{\max}$       |                                                    |                            | $R_L = 400\ \Omega, \quad C_L = 15\ \text{pF}$ |  | 15  | 20  |     | MHz  |
| $t_{\text{PLH}}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ | Q or $\overline{\text{Q}}$ |                                                |  |     | 16  | 25  | ns   |
| $t_{\text{PHL}}$ |                                                    |                            |                                                |  |     | 25  | 40  | ns   |
| $t_{\text{PLH}}$ | CLK                                                | Q or $\overline{\text{Q}}$ |                                                |  |     | 16  | 25  | ns   |
| $t_{\text{PHL}}$ |                                                    |                            |                                                |  |     | 25  | 40  | ns   |

NOTE 3: See General Information Section for load circuits and voltage waveforms.

# TYPES SN54H72, SN74H72

## AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

### recommended operating conditions

|                 |                                |            | SN54H72          |     |       | SN74H72 |     |       | UNIT |    |    |
|-----------------|--------------------------------|------------|------------------|-----|-------|---------|-----|-------|------|----|----|
|                 |                                |            | MIN              | NOM | MAX   | MIN     | NOM | MAX   |      |    |    |
| V <sub>CC</sub> | Supply voltage                 |            | 4.5              | 5   | 5.5   | 4.75    | 5   | 5.25  | V    |    |    |
| V <sub>IH</sub> | High-level input voltage       |            | 2                |     |       | 2       |     |       | V    |    |    |
| V <sub>IL</sub> | Low-level input voltage        |            |                  |     | 0.8   |         |     | 0.8   | V    |    |    |
| I <sub>OH</sub> | High-level output current      |            |                  |     | − 0.5 |         |     | − 0.5 | mA   |    |    |
| I <sub>OL</sub> | Low-level output current       |            |                  |     | 20    |         |     | 20    | mA   |    |    |
| t <sub>w</sub>  | Pulse duration                 | CLK high   | 12               |     |       | 12      |     |       | ns   |    |    |
|                 |                                | CLK low    | 28               |     |       | 28      |     |       |      |    |    |
|                 |                                | CLR or PRE | 16               |     |       | 16      |     |       |      |    |    |
| t <sub>su</sub> | Setup time, before CLK ↑       |            | data high or low |     |       | 0       |     |       | ns   |    |    |
| t <sub>h</sub>  | Hold time-data after CLK ↓     |            | 0                |     |       | 0       |     |       | ns   |    |    |
| T <sub>A</sub>  | Operating free-air temperature |            | − 55             |     |       | 125     |     |       | 0    | 70 | °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER     |                         | TEST CONDITIONS <sup>†</sup>                                                                              |  | SN54H72 |                  |      | SN74H72 |                  |      | UNIT          |
|---------------|-------------------------|-----------------------------------------------------------------------------------------------------------|--|---------|------------------|------|---------|------------------|------|---------------|
|               |                         |                                                                                                           |  | MIN     | TYP <sup>‡</sup> | MAX  | MIN     | TYP <sup>‡</sup> | MAX  |               |
| $V_{IK}$      |                         | $V_{CC} = \text{MIN.}$ , $I_I = -8 \text{ mA}$                                                            |  |         |                  | -1.5 |         |                  | -1.5 | V             |
| $V_{OH}$      |                         | $V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V.}$ , $V_{IL} = 0.8 \text{ V.}$ , $I_{OH} = -0.5 \text{ mA}$ |  | 2.4     | 3.4              |      | 2.4     | 3.4              |      | V             |
| $V_{OL}$      |                         | $V_{CC} = \text{MIN.}$ , $V_{IH} = 2 \text{ V.}$ , $V_{IL} = 0.8 \text{ V.}$ , $I_{OL} = 20 \text{ mA}$   |  |         | 0.2              | 0.4  |         | 0.2              | 0.4  | V             |
| $I_I$         |                         | $V_{CC} = \text{MAX.}$ , $V_I = 5.5 \text{ V}$                                                            |  |         | 1                |      |         | 1                |      | mA            |
| $I_{IH}$      | J, K or CLK             | $V_{CC} = \text{MAX.}$ , $V_I = 2.4 \text{ V}$                                                            |  |         | 50               |      |         | 50               |      | $\mu\text{A}$ |
|               | PRE or CLR <sup>*</sup> |                                                                                                           |  |         | 100              |      |         | 100              |      |               |
| $I_{IL}$      | J, K or CLR             | $V_{CC} = \text{MAX.}$ , $V_I = 0.4 \text{ V}$                                                            |  |         | -2               |      |         | -2               |      | mA            |
|               | PRE or CLR <sup>*</sup> |                                                                                                           |  |         | -4               |      |         | -4               |      |               |
| $I_{OS}^{\S}$ |                         | $V_{CC} = \text{MAX.}$                                                                                    |  | -40     | -100             |      | -40     | -100             |      | mA            |
| $I_{CC}$      |                         | $V_{CC} = \text{MAX.}$ , See Note 2                                                                       |  | 16      | 25               |      | 16      | 25               |      | mA            |

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

<sup>\S</sup> Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

<sup>\*</sup> Clear is tested with preset high and preset is tested with clear high.

NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$ (see note 3)

| PARAMETER | FROM<br>(INPUT)                      | TO<br>(OUTPUT)        | TEST CONDITIONS                               | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------------|-----------------------|-----------------------------------------------|-----|-----|-----|------|
| $f_{max}$ |                                      |                       | $R_L = 280 \Omega, \quad C_L = 25 \text{ pF}$ | 25  | 30  |     | MHz  |
| $t_{PLH}$ | $\overline{PRE}$ or $\overline{CLR}$ | $Q$ or $\overline{Q}$ |                                               |     | 6   | 13  | ns   |
| $t_{PHL}$ |                                      |                       |                                               |     | 12  | 24  | ns   |
| $t_{PLH}$ | CLK                                  | $Q$ or $\overline{Q}$ |                                               |     | 14  | 21  | ns   |
| $t_{PHL}$ |                                      |                       |                                               |     | 22  | 27  | ns   |

NOTE 3: See General Information Section for load circuits and voltage waveforms.

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# TYPE SN54L72

## AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

### recommended operating conditions

|          |                                | MIN              | NOM | MAX   | UNIT |
|----------|--------------------------------|------------------|-----|-------|------|
| $V_{CC}$ | Supply voltage                 | 4.5              | 5   | 5.5   | V    |
| $V_{IH}$ | High-level input voltage       | 2                |     |       | V    |
| $V_{IL}$ | Low-level input voltage        | Clock input      |     | 0.6   | V    |
|          |                                | All other inputs |     | 0.7   |      |
| $I_{OH}$ | High-level output current      |                  |     | − 0.1 | mA   |
| $I_{OL}$ | Low-level output current       |                  |     | 2     | mA   |
| $t_w$    | Pulse duration                 | CLK high or low  |     | 200   | ns   |
|          |                                | PRE or CLR low   |     | 100   |      |
| $t_{su}$ | Setup time before CLK ↑        |                  |     | 0     | ns   |
| $t_h$    | Hold time, data after CLK ↓    |                  |     | 0     | ns   |
| $T_A$    | Operating free-air temperature | − 55             |     | 125   | °C   |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |            | TEST CONDITIONS †                                                                          |  | MIN | TYP ‡ | MAX    | UNIT |
|-----------|------------|--------------------------------------------------------------------------------------------|--|-----|-------|--------|------|
| $V_{OH}$  |            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OH} = -0.1 \text{ mA}$ |  | 2.4 | 3.3   |        | V    |
| $V_{OL}$  |            | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, I_{OL} = 2 \text{ mA}$    |  |     | 0.15  | 0.3    | V    |
| $I_I$     | J or K     | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$                                                 |  |     |       | 0.1    | mA   |
|           | All other  |                                                                                            |  |     |       | 0.2    |      |
| $I_{IH}$  | J or K     | $V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$                                                 |  |     |       | 10     | µA   |
|           | PRE or CLR |                                                                                            |  |     |       | 20     |      |
|           | CLK        |                                                                                            |  |     |       | − 200  |      |
| $I_{IL}$  | J or K     | $V_{CC} = \text{MAX}, V_I = 0.3 \text{ V}$                                                 |  |     |       | − 0.18 | mA   |
|           | All other  |                                                                                            |  |     |       | − 0.36 |      |
| $I_{OS}$  |            | $V_{CC} = \text{MAX}$                                                                      |  | − 3 |       | − 15   | mA   |
| $I_{CC}$  |            | $V_{CC} = \text{MAX},$ See Note 2                                                          |  |     | 0.76  | 1.44   | mA   |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.  
‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .  
NOTE 2: With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the time of measurement, the clock input is grounded.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ (see note 3)

| PARAMETER        | FROM<br>(INPUT)                                               | TO<br>(OUTPUT)             | TEST CONDITIONS                                    | MIN | TYP | MAX | UNIT |    |
|------------------|---------------------------------------------------------------|----------------------------|----------------------------------------------------|-----|-----|-----|------|----|
| $t_{\max}$       |                                                               |                            | $R_L = 4\text{ k}\Omega, \quad C_L = 50\text{ pF}$ | 2.5 | 3   |     | MHz  |    |
| $t_{\text{PLH}}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$            | Q or $\overline{\text{Q}}$ |                                                    |     | 35  | 75  | ns   |    |
| $t_{\text{PHL}}$ | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK high) | $\overline{\text{Q}}$ or Q |                                                    |     | 60  | 150 | ns   |    |
|                  | $\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ (CLK low)  |                            |                                                    |     |     | 200 |      |    |
| $t_{\text{PLH}}$ | CLK                                                           | Q or $\overline{\text{Q}}$ |                                                    |     | 10  | 35  | 75   | ns |
| $t_{\text{PHL}}$ |                                                               |                            |                                                    |     | 10  | 60  | 150  | ns |

NOTE 3: See General information Section for load circuits and voltage waveforms.