

PART NUMBER**54L74SCA-ROCV****Rochester Electronics****Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

INCH-POUND

MIL-M-38510/21F
15 February 2006
SUPERSEDING
MIL-M-38510/21E
7 July 2005

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, TTL, LOW POWER, FLIP-FLOPS, MONOLITHIC SILICON

Inactive for new design after 7 September 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, TTL, low power, bistable logic microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535 and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>
01	R-S master slave flip-flop
02	J-K master slave flip-flop
03	Dual J-K master slave flip-flop
04	Dual J-K master slave flip-flop
05	Dual D-type edge triggered flip-flop

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
A	GDFP5-F14 or CDFP6-F14	14	Flat pack
B	GDFP4-F14	14	Flat pack
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage range	0 V dc to 8.0 V dc
Input voltage range	0 V dc to 6.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation in accordance	
with flip-flop (P_D) <u>1/</u>	11 mW dc
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	(See MIL-STD-1835)
Junction temperature (T_J) <u>2/</u>	175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.7 V dc, except clock input of types 01, 02, 03, and 04
Maximum low level input voltage (V_{IL})	0.6 V dc, (types 01, 02, 03, and 04)
Normalized fanout (each output) <u>3/</u>	10 maximum
Width of clock pulse	≥ 200 ns
Width of preset pulse	≥ 100 ns
Width of clear pulse	≥ 100 ns
Input setup time:	
Device types 02, 03, and 04	$\geq$ Clock pulse width minimum
Device type 01	100 ns minimum when R, S input data is complementary
Device type 01	$\geq$ Clock pulse width, minimum when R, S input data is not complementary
Device type 05	50 ns minimum
Input hold time	10 ns minimum
Case operating temperature range (T_C)	-55°C to 125°C

2.0 APPLICABLE DOCUMENT

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}) at one output for 5 seconds duration.

2/ Maximum junction temperature should not be exceeded except in accordance with allowable short duration burn-in screening condition in accordance with MIL-PRF-38535.

3/ Device will fanout in both high and low levels to the specified number of inputs of the same device type as that being tested.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Truth tables and logic diagrams. The truth tables and logic diagrams shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.4 Case outlines. Case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. Lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table 1 and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 17 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Device type					Limits		Unit
			01	02	03	04	05	Min	Max	
High level output voltage	V _{OH}	V _{IN} = 0.7 V V _{CC} = 4.5 V I _{OH} = -100μA						2.4		V
Low level input voltage	V _{OL}	I _{OL} = 2 mA V _{CC} = 4.5 V							0.3	V
Low level input current	I _{IL1}	V _{CC} = 5.5 V V _{IN} = 0.3 V	S R	J K	J K	J K		-43	-140	μA
Low level input current	I _{IL2}	V _{CC} = 5.5 V V _{IN} = 0.3 V	Clock	Clock	Clock			-105	-360	μA
			Preset Clear	Preset Clear	Clear	Preset		-86	-280	μA
Low level input current	I _{IL3}	V _{CC} = 5.5 V V _{IN} = 0.3 V				Clock Clear		-172	-560	μA
Low level input current	I _{IL4}	V _{CC} = 5.5 V V _{IN} = 0.3 V					D Preset	-50	-180	μA
Low level input current	I _{IL5}	V _{CC} = 5.5 V V _{IN} = 0.3 V					Clock Clear	-120	-360	μA
High level input current	I _{IH1}	V _{CC} = 5.5 V V _{IN} = 2.4 V	S R	J K	J K	J K	D		10	μA
High level input current	I _{IH2}	V _{CC} = 5.5 V V _{IN} = 5.5 V	S R	J K	J K	J K	D		100	μA
High level input current	I _{IH3}	V _{CC} = 5.5 V V _{IN} = 2.4 V	Clear Preset	Clear Preset	Clear	Preset	Clock Preset		200	μA
High level input current	I _{IH4}	V _{CC} = 5.5 V V _{IN} = 5.5 V	Clear Preset Clock	Clear Preset Clock	Clock Clear	Preset	Clock Clear		200	μA
High level input current	I _{IH5}	V _{CC} = 5.5 V V _{IN} = 2.4 V					Clear		30	μA
High level input current	I _{IH6}	V _{CC} = 5.5 V V _{IN} = 5.5 V					Clear		300	μA
High level input current	I _{IH7}	V _{CC} = 5.5 V V _{IN} = 2.4 V				Clear			40	μA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C	Device type					Limits		Unit
			01	02	03	04	05	Min	Max	
High level input current	I _{IH8}	V _{CC} = 5.5 V V _{IN} = 5.5 V				Clock Clear			400	μA
High level input current	I _{IH9}	V _{CC} = 5.5 V V _{IN} = 2.4 V				Clock		0	-400	μA
High level input current	I _{IH10}	V _{CC} = 5.5 V V _{IN} = 2.4 V	Clock	Clock	Clock			0	-200	μA
Short circuit output current	I _{OS}	V _{CC} = 5.5 V V _{IN} = 0 <u>1</u> /						-3	-15	mA
Supply current per flip-flop	I _{CC}	V _{CC} = 5.5 V V _{IN(clock)} = 0	Types 01, 02, 03, and 04						1.9	mA
			Type 05						1.5	mA
Maximum clock frequency	f _{MAX} <u>2</u> /	C _L = 50 pF R _L = 4 kΩ						2.5		MHz
Propagation delay to a high level (clear or pre-set to output)	t _{PLH}							10	125	ns
Propagation delay to a low level (clear or pre-set to output)	t _{PHL}		V _{IN(clock)} = 2.4 V					10	200	ns
			V _{IN(clock)} = 0 V, types 01, 02, 03, and 04					10	250	
Propagation delay to a high level (clock to output)	t _{PLH}							10	125	ns
Propagation delay to a low level (clock to output)	t _{PHL}							10	200	ns

1/ Not more than one output should be shorted at a time.

2/ f_{MAX} , minimum limit specified is the frequency of the input pulse. The output frequency shall be one half of the input frequency.

TABLE II. Electrical test requirements.

MIL-PRF-38535 Test requirement	Subgroups (see table III)	
	Class S Devices	Class B Devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3, 7, 8 9, 10, 11	N/A
Groups C end point electrical parameters	1, 2, 3, 7, 8 9, 10, 11	1, 2, 3
Group D end point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6, shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

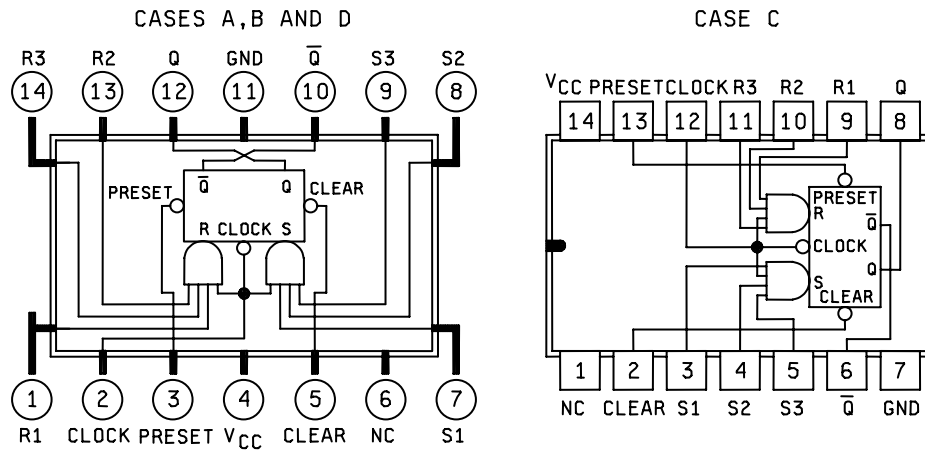
- a. End point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

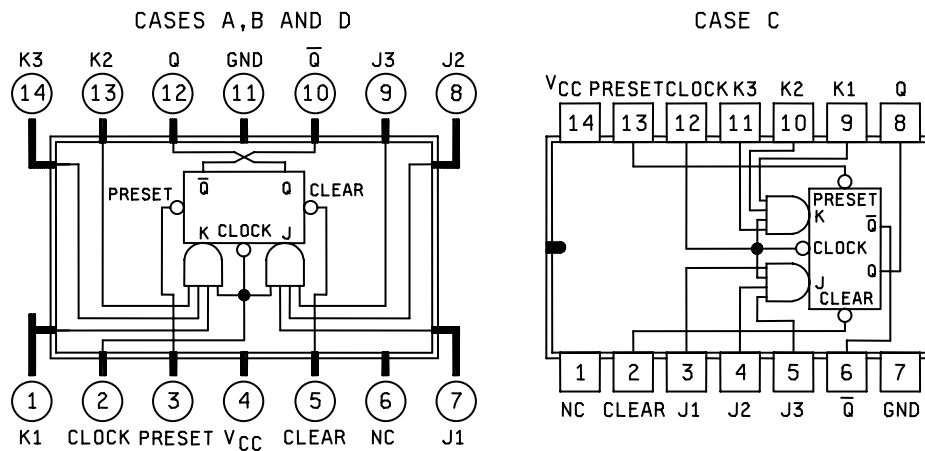
4.5 Methods inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

DEVICE TYPE 01



DEVICE TYPE 02



DEVICE TYPE 02

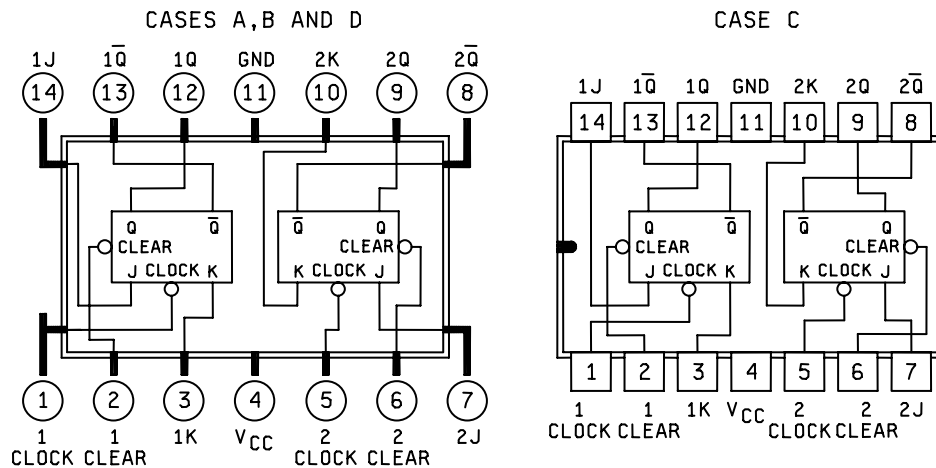
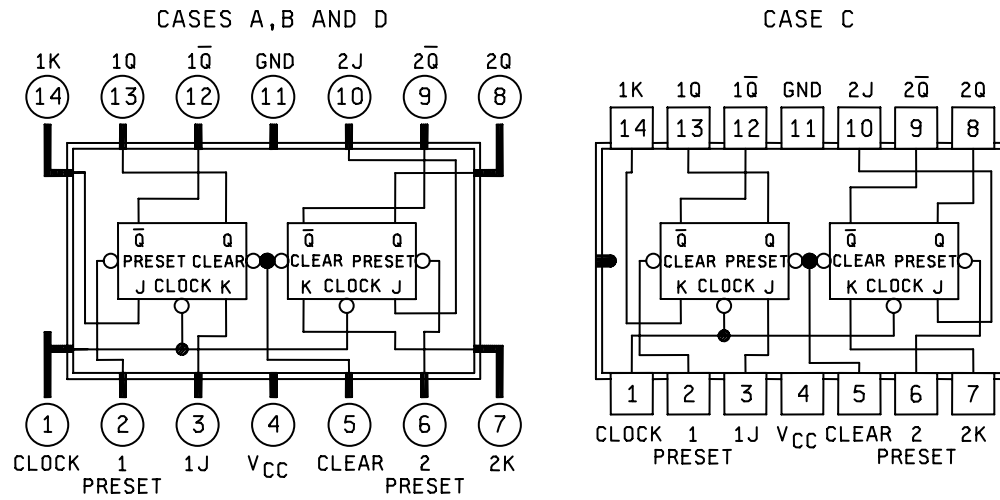


Figure 1. Terminal connections.

DEVICE TYPE 04



DEVICE TYPE 05

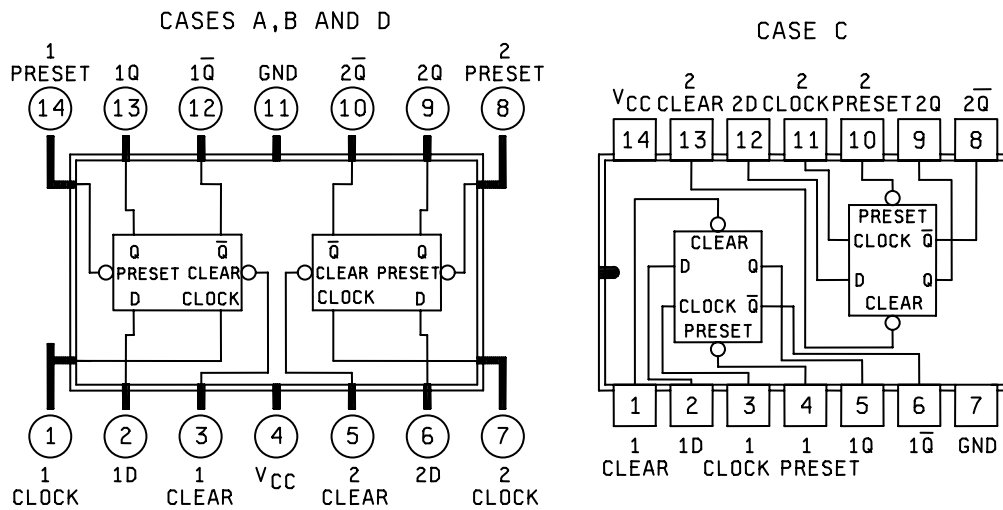


Figure 1. Terminal connections - Continued.

Device type 01

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Positive logic: Low input to preset sets Q to high level
 Low input to clear sets Q to low level
 Preset and clear are independent of clock

NOTES:

1. $J = J_1 J_2 J_3$
2. $K = K_1 K_2 K_3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

Device type 02

Truth table		
t_n		t_{n+1}
R	S	Q
L	L	Q_n
L	H	H
H	L	L
H	H	Indeterminate

Positive logic: Low input to preset sets Q to high level
 Low input to clear sets Q to low level
 Preset and clear are independent of clock

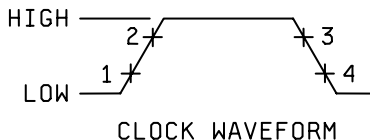
NOTES:

1. $R = R_1 R_2 R_3$
2. $S = S_1 S_2 S_3$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.

Description for device types 01 and 02

These flip-flops are based on the master slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation as controlled by the clock pulse is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.

Figure 2. Truth tables and device descriptions.

Device type 03

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Positive logic: Low input to clear sets Q to low level
Clear is independent of clock

NOTES:

1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

Device type 04

Truth table		
t_n		t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

Positive logic: Low input to preset sets Q to high level
Low input to clear sets Q to low level
Preset and clear are independent of clock

NOTES:

1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

Description for device types 03 and 04

These flip-flops are based on the master slave principle and each has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation as controlled by the clock pulse is as follows:

1. Isolate slave from master.
2. Enter information from AND gate inputs to master.
3. Disable AND gate inputs.
4. Transfer information from master to slave.

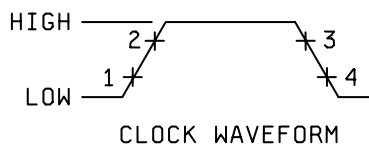


Figure 2. Truth tables and device descriptions- Continued.

Device type 05

Truth table each flip-flop		
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
L	L	Q_n
L	H	L

Positive logic: Low input to preset sets Q to high level
 Low input to clear sets Q to low level
 Preset and clear are independent of clock

NOTES:

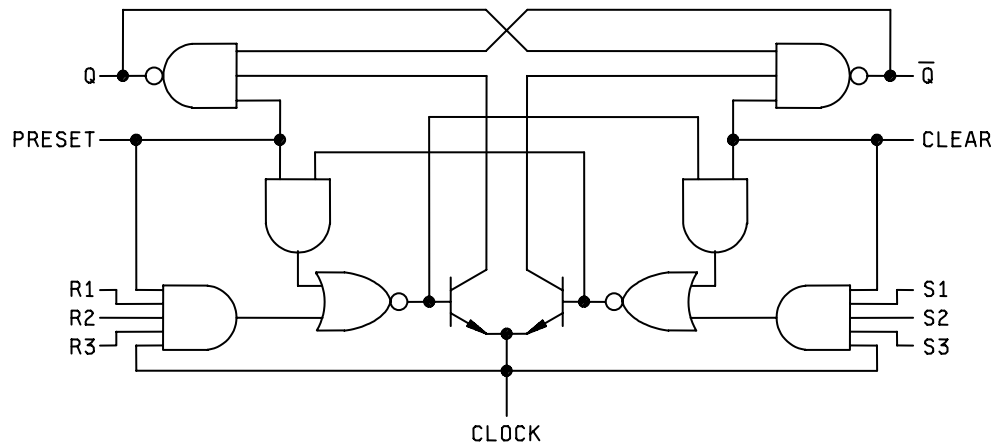
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

Description for device type 05

Input information is transferred to the output on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.

Figure 2. Truth tables and device descriptions - Continued.

DEVICE TYPE 01



DEVICE TYPE 02

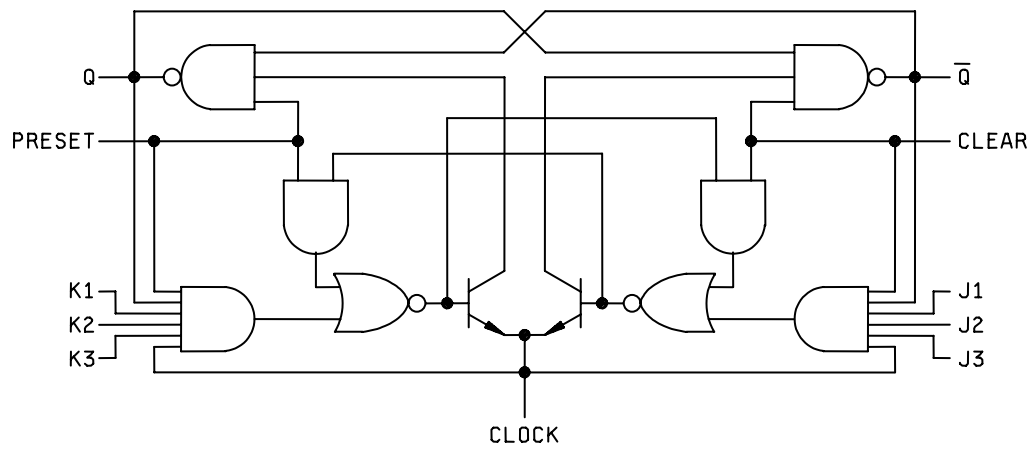
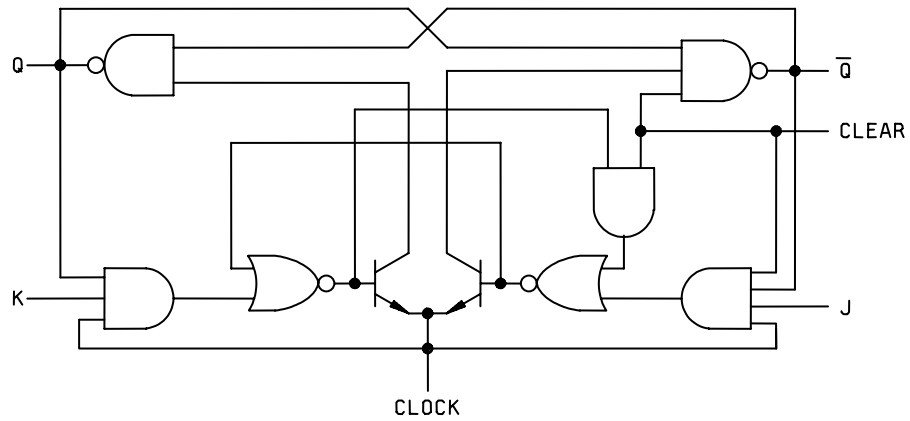


FIGURE 3. Logic diagram for device types 01, 02, 03, 04, and 05.

DEVICE TYPE 03



DEVICE TYPE 04

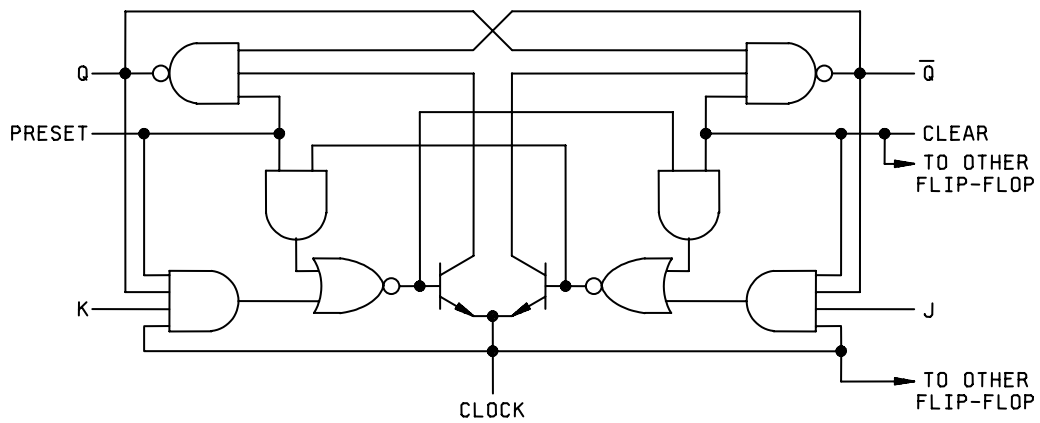


FIGURE 3. Logic diagram for device types 01, 02, 03, 04, and 05 - Continued.

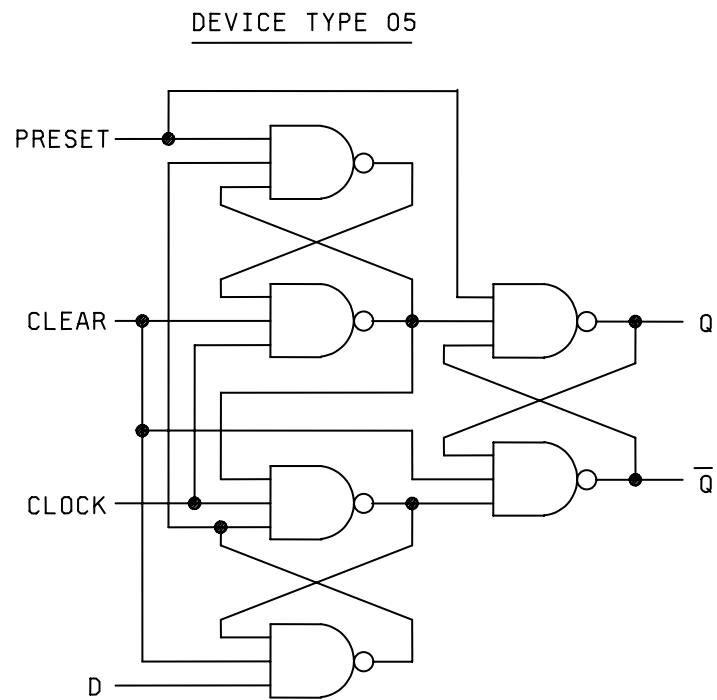
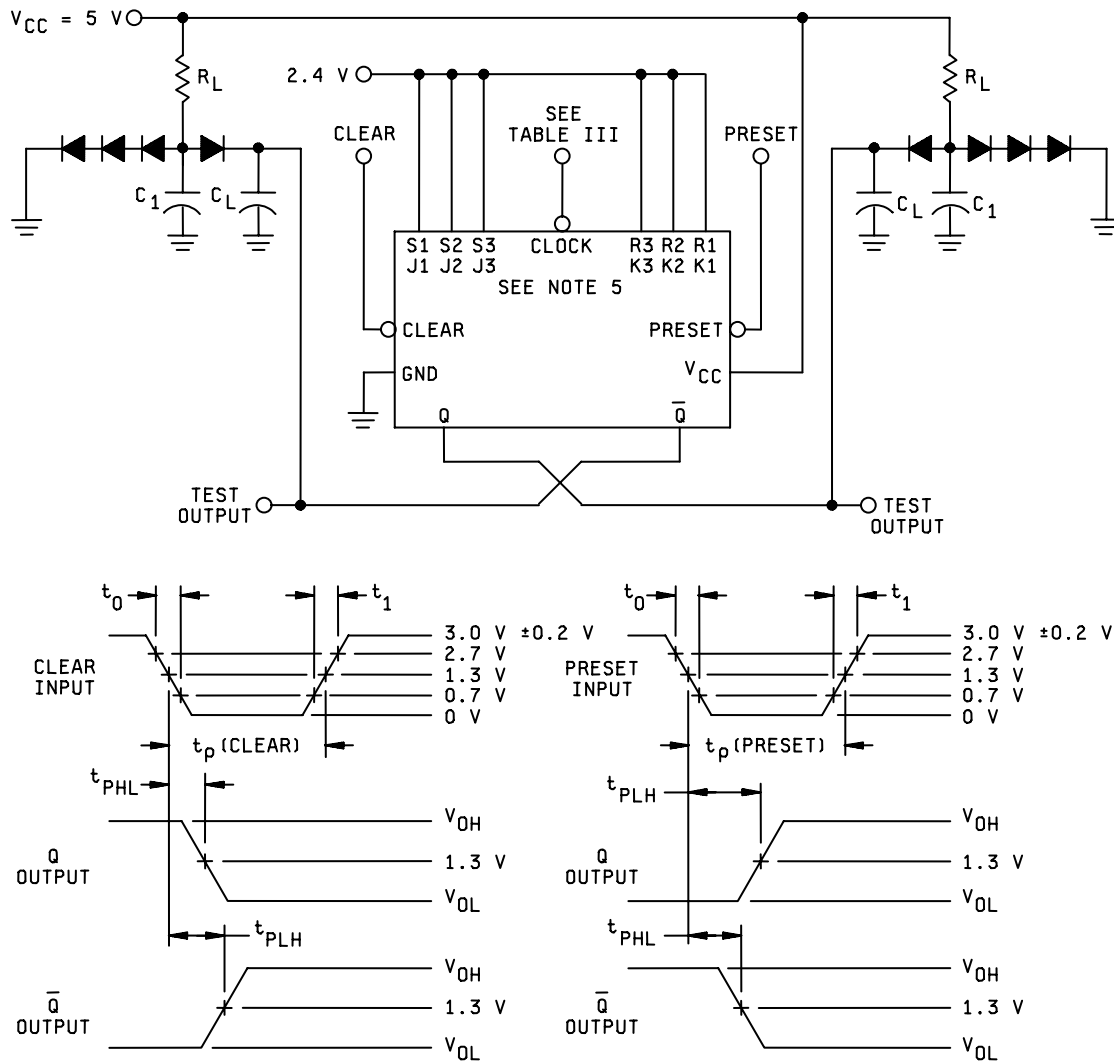


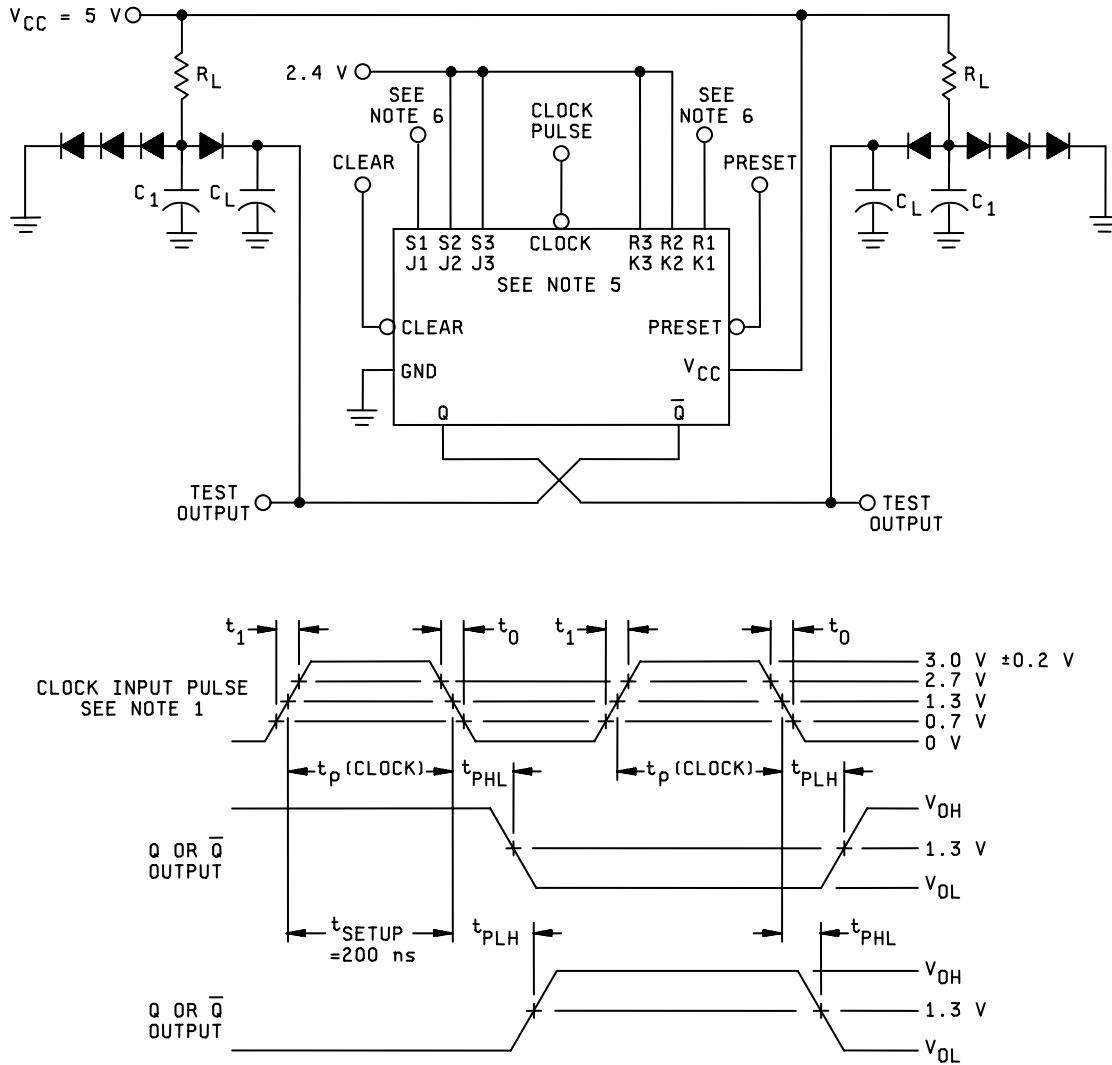
FIGURE 3. Logic diagram for device types 01, 02, 03, 04, and 05 - Continued.



NOTES:

- 1/ Clear or preset input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_{p(\text{CLEAR})} = t_{p(\text{PRESET})} = 100 \text{ ns}$, $\text{PRR} = 0.5 \text{ MHz}$ and $Z_{OUT} \approx 50 \Omega$.
- 2/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 3/ $R_L = 4 \text{ k}\Omega \pm 5\%$ and $C_1 = 30 \text{ pF}$ minimum.
- 4/ All diodes are 1N916 or equivalent.
- 5/ R and S inputs apply for device type 01, J and K inputs apply for device type 02.
- 6/ When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see table III).

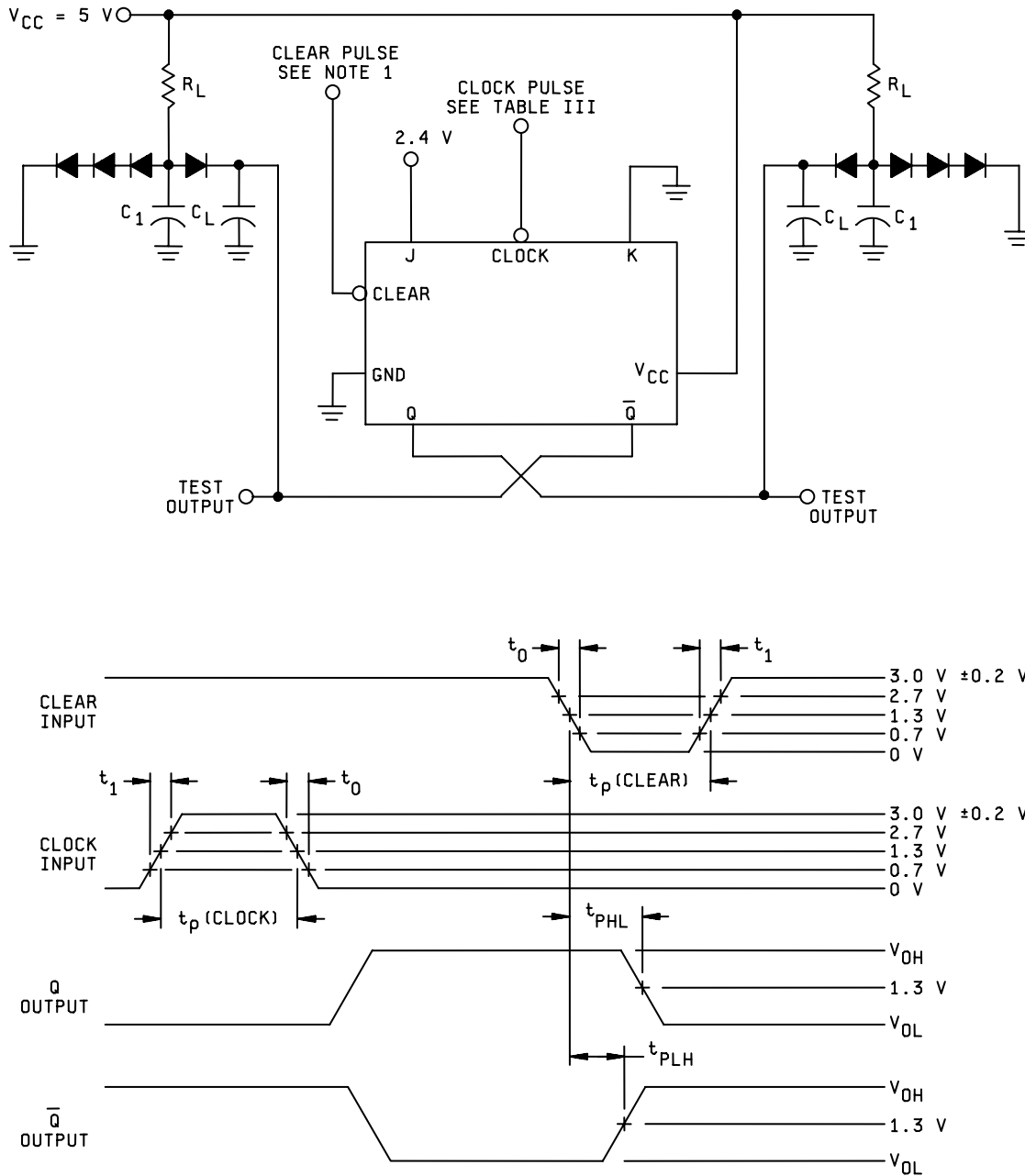
FIGURE 4. Clear and preset switching test circuit for device type 01 and 02.



NOTES:

- 1/ Clock input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_p = 200 \text{ ns}$, $\text{PRR} = 0.5 \text{ MHz}$, When testing f_{MAX} , $\text{PRR} = \text{see table III}$.
- 2/ All diodes are 1N916 or equivalent.
- 3/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 4/ $R_L = 4 \text{ k}\Omega \pm 5\%$ and $C_1 = 30 \text{ pF}$ minimum.
- 5/ R and S inputs apply for device type 01, J and K inputs apply for device type 02.
- 6/ R1 input is connected to Q output, S1 input is connected to $\bar{Q}$ output. J1 and K1 inputs are connected to 2.4 V.

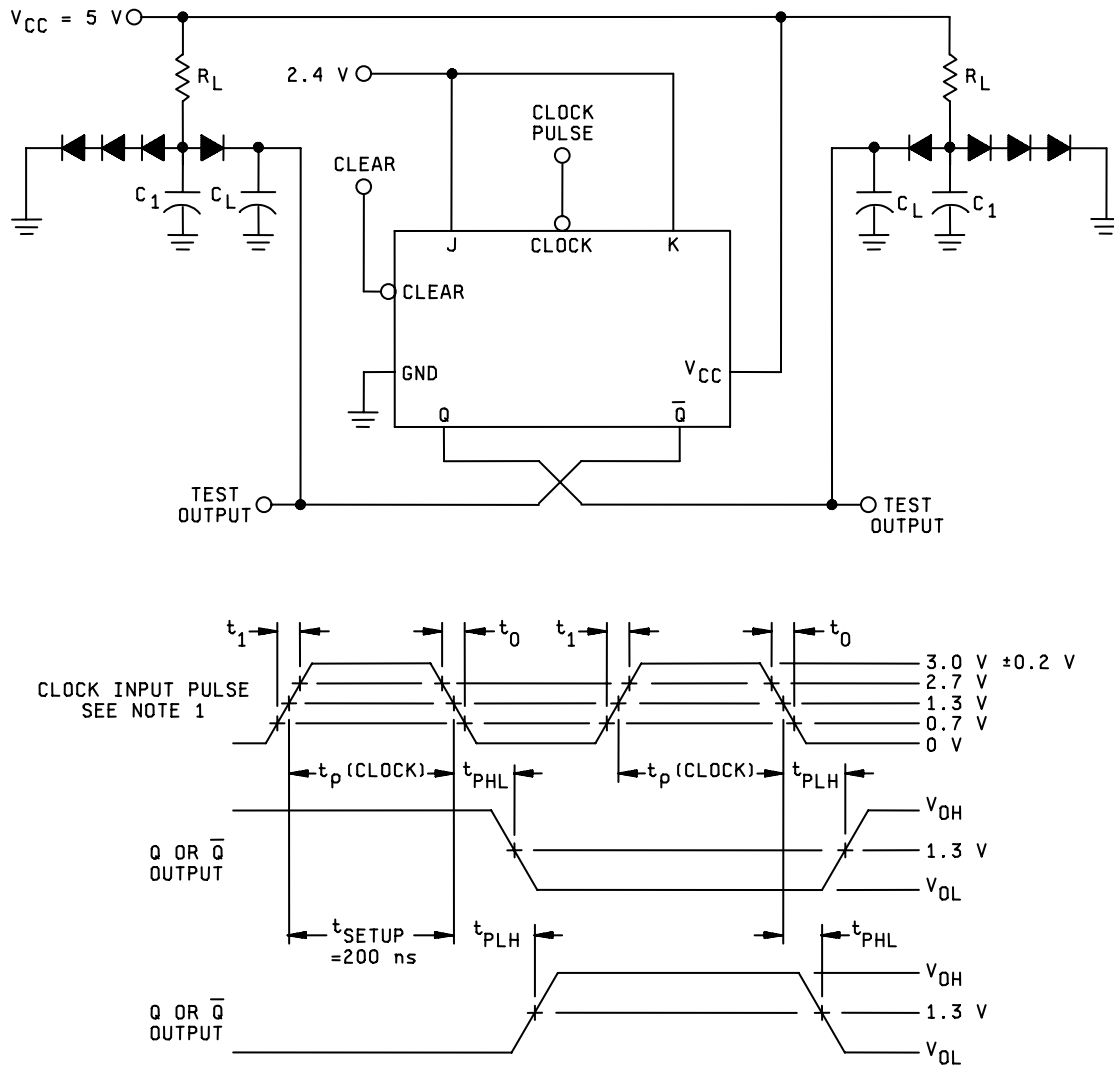
FIGURE 5. Synchronous switching test circuit for device types 01 and 02.



NOTES:

- 1/ Clear input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_{p(\text{CLEAR})} = 100 \text{ ns}$, $\text{PRR} = 0.5 \text{ MHz}$ and $Z_{OUT} = 50 \Omega$.
- 2/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 3/ $R_L = 4 \text{ k}\Omega \pm 5\%$ and $C_1 = 30 \text{ pF}$ minimum.
- 4/ All diodes are 1N916 or equivalent.
- 5/ Clock input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_{p(\text{CLOCK})} \geq 200 \text{ ns}$, $\text{PRR} = 0.5 \text{ MHz}$.

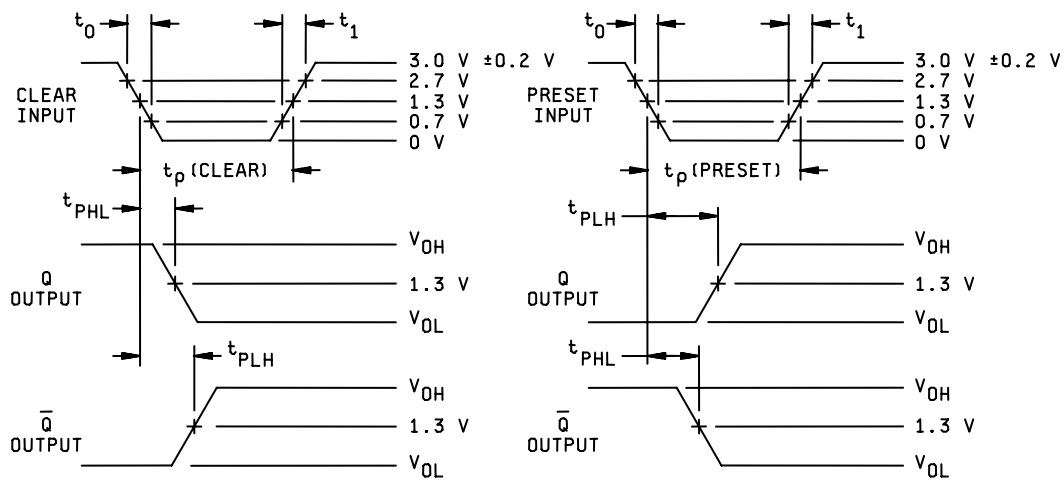
FIGURE 6. Clear switching test circuit for device types 03.



NOTES:

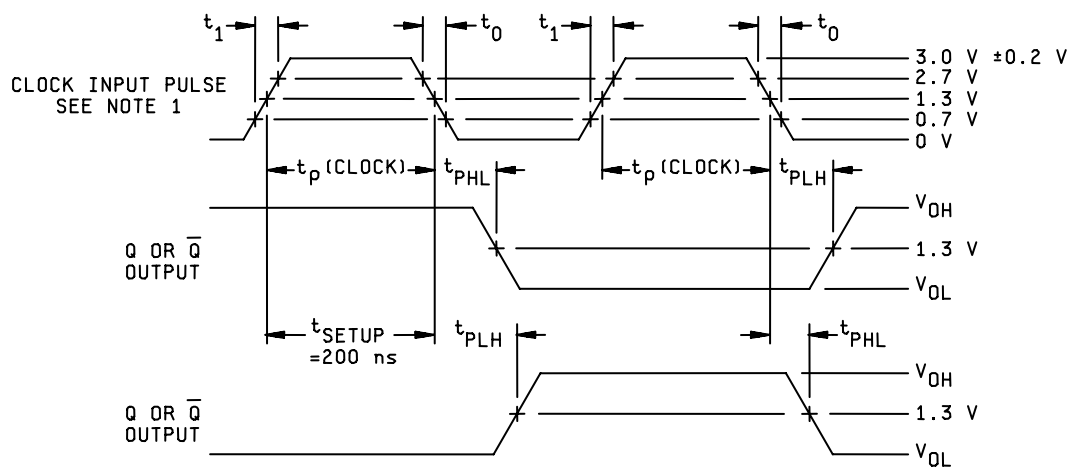
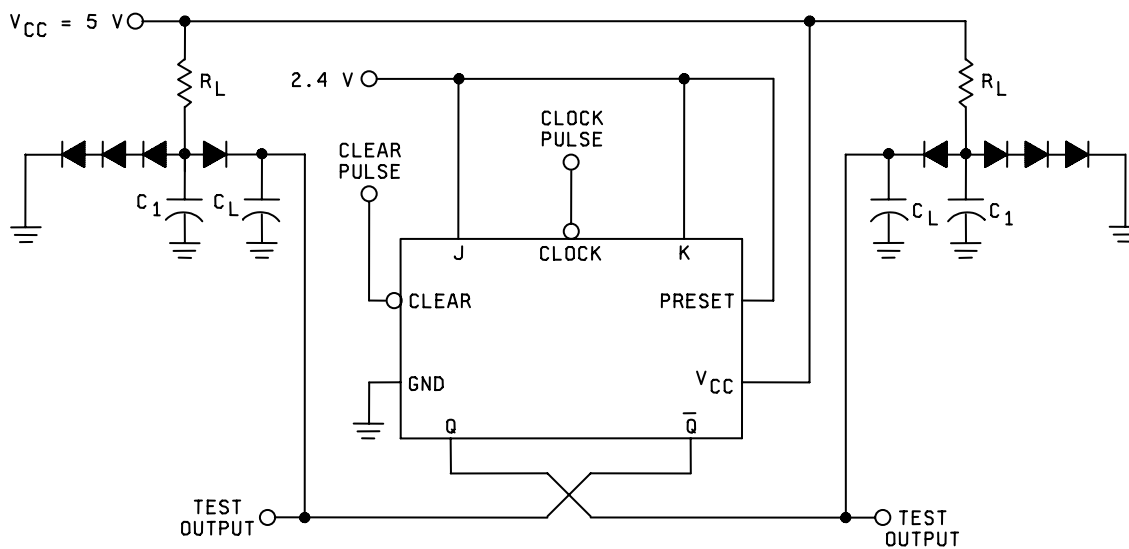
- 1/ Clock input pulse characteristics: $V_{gen} = 3.0\text{ V} \pm 0.2\text{ V}$, $t_0 = 15\text{ ns}$, $t_1 = 15\text{ ns}$, $t_p = 200\text{ ns}$, $PRR = 0.5\text{ MHz}$, when testing f_{MAX} , $PRR =$ see table III.
- 2/ All diodes are 1N916 or equivalent.
- 3/ $C_L = 50\text{ pF}$ minimum and includes probe and jig capacitance.
- 4/ $R_L = 4\text{ k}\Omega \pm 5\%$ and $C_1 = 30\text{ pF}$ minimum.

FIGURE 7. Synchronous switching test circuit for device types 03.



5/ When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see table III).

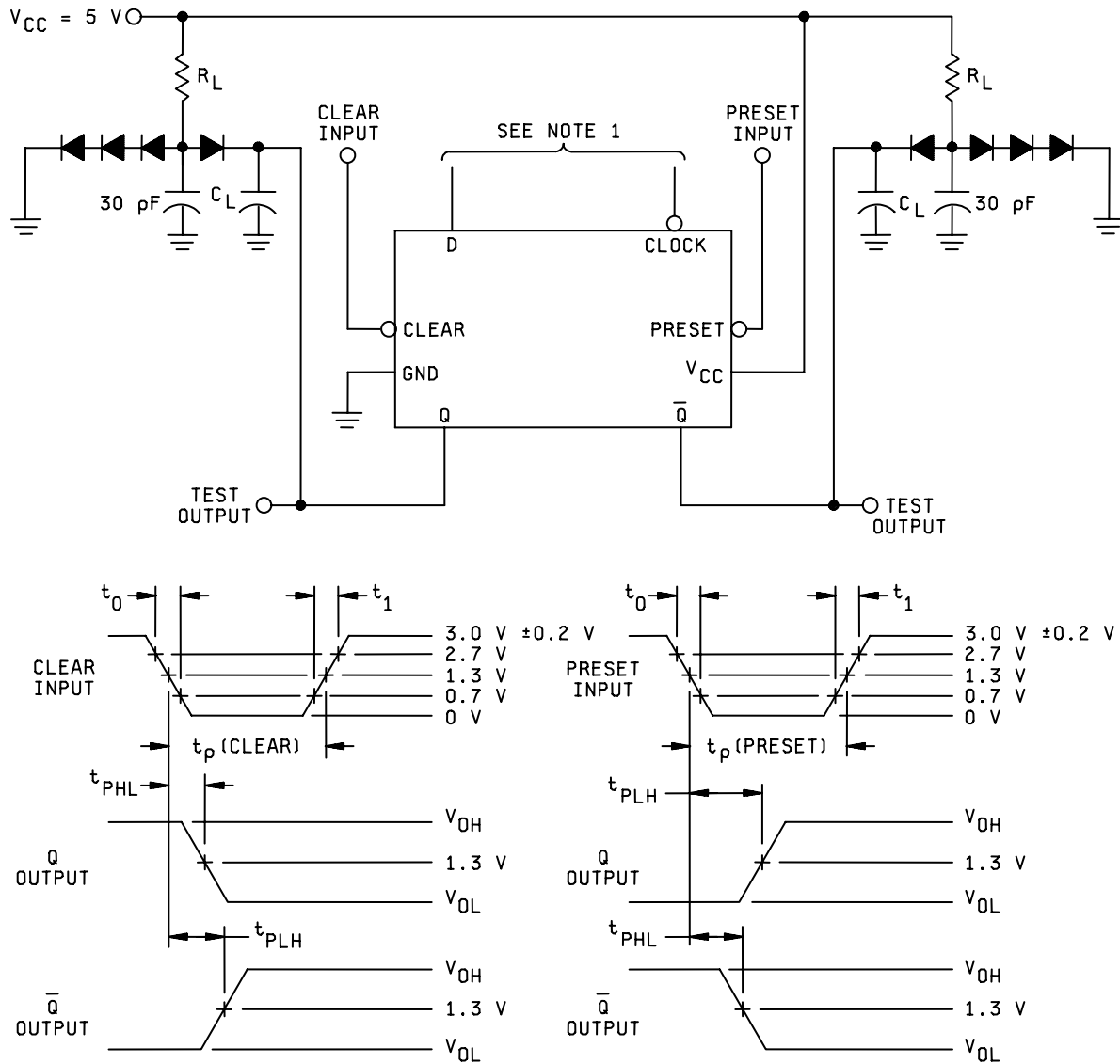
20



NOTES:

- 1/ Clock input pulse characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_p = 200 \text{ ns}$, $PRR = 0.5 \text{ MHz}$, when testing f_{MAX} , $PRR = \text{see table III}$.
- 2/ All diodes are 1N916 or equivalent.
- 3/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 4/ $R_L = 4 \text{ k}\Omega \pm 5\%$ and $C_1 = 30 \text{ pF}$ minimum.

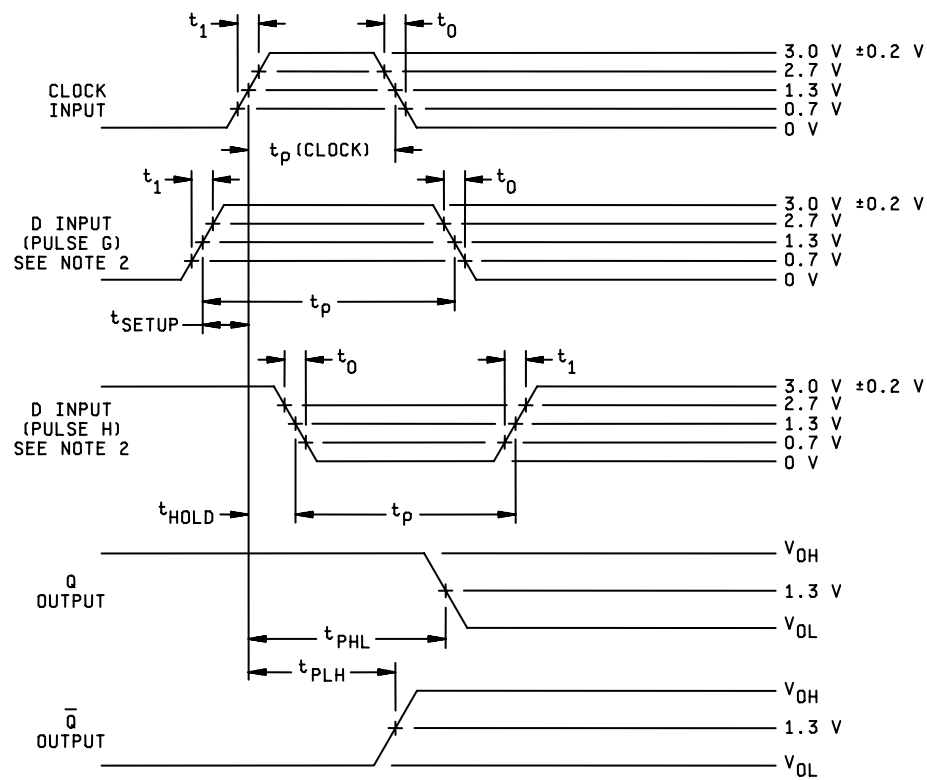
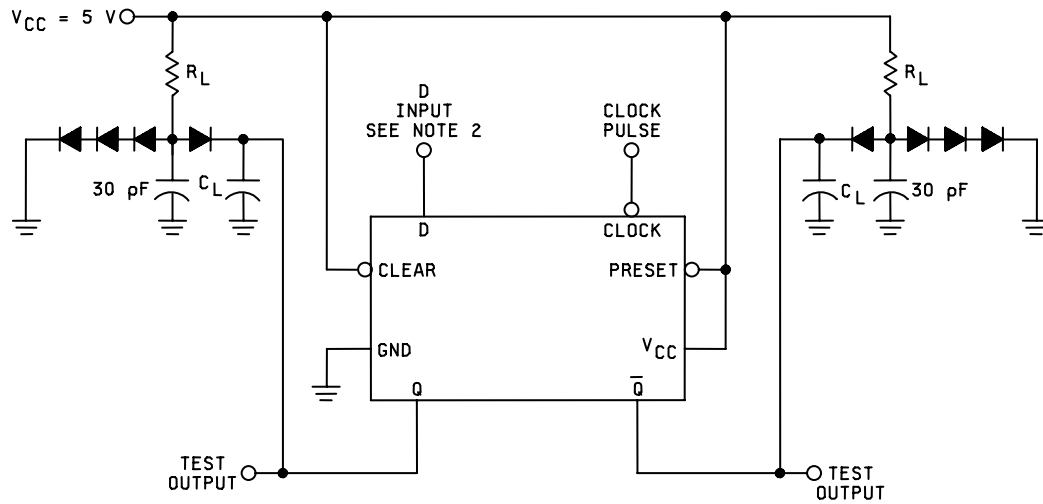
FIGURE 9. Synchronous switching test circuit for device type 04.



NOTES:

- 1/ Clear and preset inputs dominate regardless of the state of clock or D inputs.
- 2/ All diodes are 1N916 or equivalent.
- 3/ Clear or preset input pulse characteristics: $V_{gen} = 3.0\text{ V} \pm 0.2\text{ V}$, $t_0 = 15\text{ ns}$, $t_p = 100\text{ ns}$, $PRR = 0.5\text{ MHz}$.
- 4/ $C_L = 50\text{ pF}$ minimum and includes probe and jig capacitance.
- 5/ $R_L = 4\text{ k}\Omega \pm 5\%$.
- 6/ When testing clear to output switching, preset input shall have a negative pulse; when testing preset to output switching, clear input shall have a negative pulse (see table III).

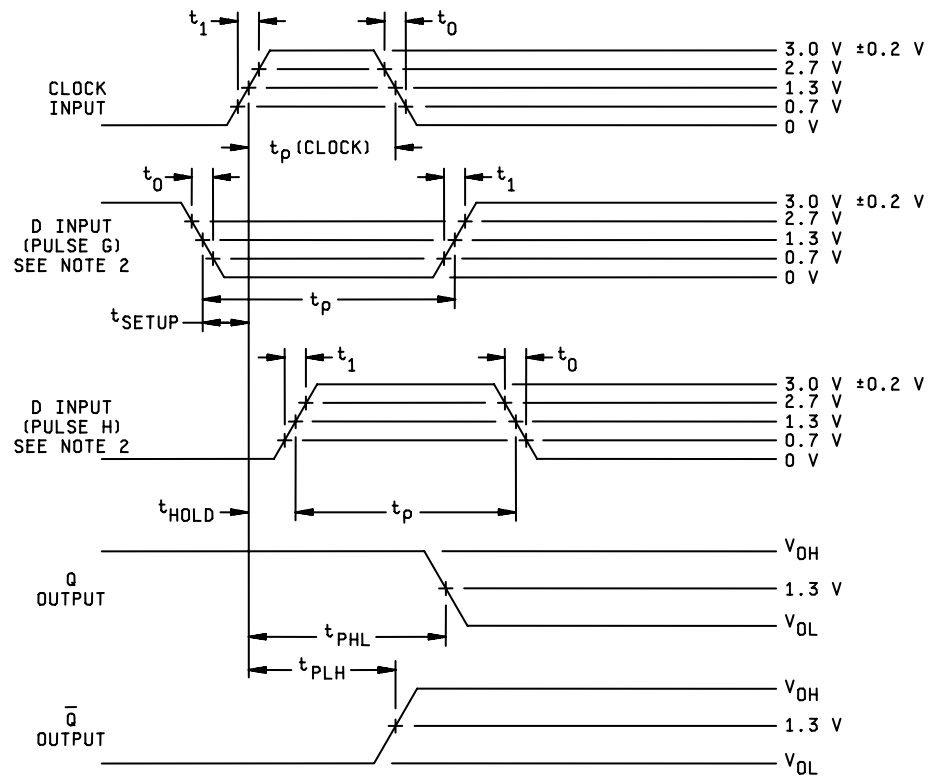
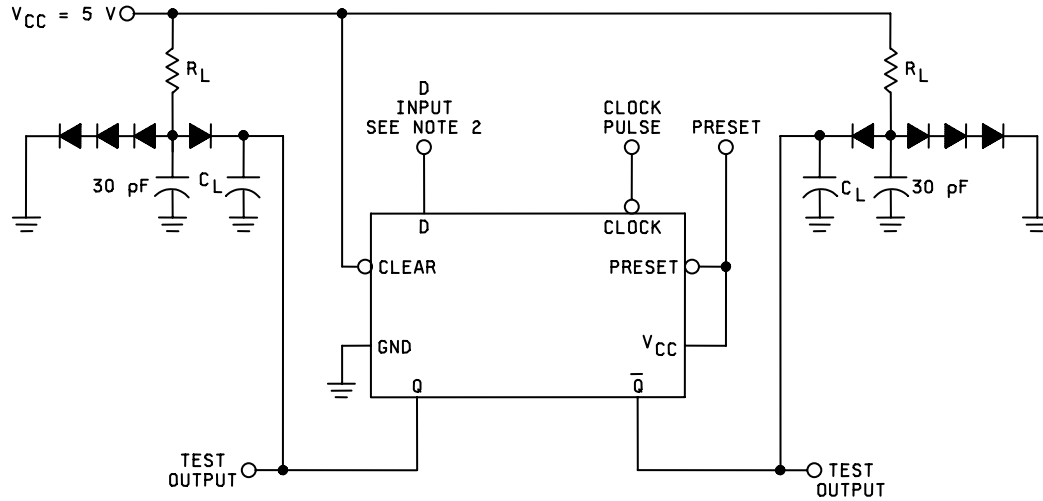
FIGURE 10. Clear and preset switching test circuit and waveforms for device type 05.



NOTES:

- 1/ Clock input pulse has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_p = 200 \text{ ns}$, $PRR = 0.5 \text{ MHz}$, when testing f_{MAX} , $PRR = \text{see table III}$.
- 2/ D input (pulse G and pulse H) has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_{SETUP} = 50 \text{ ns}$, $t_p = 100 \text{ ns}$ and PRR is 50% of the clock PRR .
- 3/ All diodes are 1N916 or equivalent.
- 4/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 5/ $R_L = 4 \text{ k}\Omega \pm 5\%$.

FIGURE 11. Synchronous switching test circuit for device type 05.



NOTES:

- 1/ Clock input pulse has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_p = 200 \text{ ns}$, $PRR = 0.5 \text{ MHz}$. When testing f_{MAX} , $PRR =$ see table III.
- 2/ D input (pulse G) has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_{SETUP} = 50 \text{ ns}$, $t_p = 100 \text{ ns}$ and PRR is 50% of the clock PRR . D input (pulse H) has the following characteristics: $V_{gen} = 3.0 \text{ V} \pm 0.2 \text{ V}$, $t_0 = 15 \text{ ns}$, $t_1 = 15 \text{ ns}$, $t_{HOLD} = 10 \text{ ns}$, $t_p = 80 \text{ ns}$ and PRR is 50% of the clock PRR .
- 3/ All diodes are 1N916 or equivalent.
- 4/ $C_L = 50 \text{ pF}$ minimum and includes probe and jig capacitance.
- 5/ $R_L = 4 \text{ k}\Omega \pm 5\%$.

FIGURE 12. Synchronous switching test circuit for device type 05.

TABLE III. Group A inspection for device type 01. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit		
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max			
			Test no.	R1	Clock	Preset	V _{CC}	Clear	NC	S1	S2	S3	$\bar{Q}$	GND	Q	R2	R3						
1 T _C =+25°C	V _{OH}	3006	1	0.7 V	A	4.5 V	4.5 V	4.5 V		2.0 V	2.0 V	2.0 V	-100μA	GND	-100μA	0.7 V	0.7 V	Q	2.4				
			2	2.0 V	A	4.5 V	"	4.5 V		0.7 V	0.7 V	0.7 V	"	"	2.0 V	2.0 V	Q	"		"			
			3	4.5 V	4.5 V	0.7 V	"	2.0 V		4.5 V	4.5 V	4.5 V	"	"	-100μA	4.5 V	4.5 V	Q	"		"		
			4	4.5 V	4.5 V	2.0 V	"	0.7 V		4.5 V	4.5 V	4.5 V	-100μA	"	"	4.5 V	4.5 V	Q	"	V	"		
	V _{OL}	3007	5	2.0 V	A	4.5 V	"	4.5 V		0.7 V	0.7 V	0.7 V		"	2 mA	2.0 V	2.0 V	Q					
			6	0.7 V	A	4.5 V	"	4.5 V		2.0 V	2.0 V	2.0 V	2 mA	"	"	0.7 V	0.7 V	Q			"		
			7	4.5 V	4.5 V	0.7 V	"	2.0 V		4.5 V	4.5 V	4.5 V	"	"	4.5 V	4.5 V	Q			"			
			8	4.5 V	"	2.0 V	"	0.7 V		4.5 V	"	"	"	"	2 mA	4.5 V	4.5 V	Q	0.3		"		
	I _{IL1}	3009	9		"		5.5 V	B		0.3 V		"		"				S1	-43	-140	μA		
			10		"		"	"		4.5 V	0.3 V	"		"				S2	"	"	"		
			11		"		"	"		4.5 V	4.5 V	0.3 V		"				S3	"	"	"		
			12	0.3 V	"	B	"	"		"	"	"	"	"		4.5 V	4.5 V	R1	"	"	"		
	I _{IL2}	3010	13	4.5 V	"	"	"	"		"	"	"	"	"		0.3 V	4.5 V	R2	"	"	"		
			14	"	"	"	"	"		"	"	"	"	"		4.5 V	0.3 V	R3	"	"	"		
			16	"	0.3 V	"	"	B		4.5 V	4.5 V	4.5 V		"		"	4.5 V	Clock	-120	-360	"		
			17	"	0.3 V	"	"	"		"	"	"	"	"		"	"	Clock	-120	-360	"		
	I _{IH1}	3011	18	"	0.3 V	"	"	0.3 V		"	"	"	"	"	"	"	"	Preset	-86	-280	"		
			19		GND		"	GND		2.4 V	GND	GND		"				Clear	-86	-280	"		
			20		"		"	"		GND	2.4 V	GND		"				S1			"		
			21		"		"	"		GND	GND	GND		"				S2			"		
	I _{IH2}	3012	22	2.4 V	"	GND	"	"		"	"	2.4 V	"	"		GND	GND	S3	10	"	"		
			23	GND	"	"	"	"		"	"	"	"	"		2.4 V	GND	R1	"	"	"		
			24	GND	"	"	"	"		"	"	"	"	"		GND	2.4 V	R2	"	"	"		
			25		"		"	GND		5.5 V	GND	GND		"				R3	"	"	"		
I _{IH3}	3013	26		"		"	"		GND	5.5 V	GND		"				S1			"			
		27		"		"	"		GND	GND	GND		"				S2			"			
		28	5.5 V	"	GND	"	"		"	"	5.5 V		"				S3			"			
		29	GND	"	"	"	"		"	"	"	"	"		GND	GND	R1	100	"	"			
I _{IH4}	3014	30	GND	"	"	"	"		"	"	"	"	"		5.5 V	5.5 V	R2	"	"	"			
		31		"		"	"		"	"	"	"	"		GND	GND	R3	"	"	"			
		32	GND	"	2.4 V	"	2.4 V		GND	GND	GND	GND	"	GND	GND	GND	Clear		20	"			
		33	GND	"	5.5 V	"	5.5 V		"	"	"	"	"	GND	GND	GND	Preset		20	"			
I _{IH10}	3015	34		"		"	"		GND	GND	GND	GND	"				Clear			"			
		35	GND	5.5 V	GND	"	GND		"	"	"	"	"		GND	GND	Preset			"			
		36	"	5.5 V	"	"	"		"	"	"	"	"		"	"	Clear			"			
		37	"	"	"	"	"		"	"	"	"	"		"	"	Clock	200		"			
I _{OS}	3016	38	"	2.4 V	GND	"	GND		"	"	"	"	"		"	"	Clock	0	-200	"			
		39	4.5 V	2.4 V	"	"	"		"	"	"	"	"		"	"	Clock	0	-200	"			
		40	4.5 V	"	GND	"	GND		4.5 V	4.5 V	4.5 V	GND	"	GND	4.5 V	4.5 V	Q	-3	-15	mA			
		41	4.5 V	"	"	"	"	"	4.5 V	4.5 V	4.5 V	"	"	"	4.5 V	4.5 V	Q	-3	-15	"			
I _{CC}	3005	42 CKT A	GND	"	GND	"	4.5 V		"	GND	GND		"		"	GND	V _{CC}			"			
		42 CKT B	"	"	GND	"	4.5 V		"	"	"		"		"	"	"			"			
		42 CKT A	"	"	4.5 V	"	"		"	"	"	"	"	GND	"	"	"			"			
		42 CKT B	"	"	4.5 V	"	GND	GND	"	"	"	"	"	GND	"	"	"	1.44		"			
																					1.90	1.44	"
2	Same tests, terminal conditions and limits as for subgroup 1, except T _C = +125°C.																						
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C = -55°C.																						

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit			
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max				
			Test no.	R1	Clock	Preset	V _{CC}	Clear	NC	S1	S2	S3	$\bar{Q}$	GND	Q	R2	R3							
7 T _C =+25°C 2/ 4/			43	A	A	A	4.5 V	B	A		A	A	H 3/ H	GND	L 3/ L	A	A	All outputs	H or L as shown 3/					
			44	B	A	"	"	A			"	"	"	"	"	"	"							
			45	B	B	"	"	"			"	"	"	"	"	"	"							
			46	A	A	"	"	"			"	"	"	"	"	"	"							
			47	"	B	"	"	"			"	B	"	"	"	"	"							
			48	"	A	"	"	"			"	A	"	"	"	"	"							
			49	"	B	"	"	"			"	"	"	"	"	B	"							
			50	"	A	"	"	"			"	"	"	"	"	A	"							
			51	"	B	"	"	"			"	B	"	"	"	"	"							
			52	"	A	"	"	"			"	A	"	"	"	"	B							
			53	"	B	"	"	"			"	"	"	"	"	"	B							
			54	"	A	"	"	"			"	"	"	"	"	"	A							
			55	"	B	"	"	"			"	"	"	"	"	"	A							
			56	B	A	"	"	"			"	B	B	B	"	"	B							
			57	B	B	"	"	"			"	"	"	"	"	"	B							
			58	A	A	B	"	"			"	"	"	"	"	"	A							
			59	A	B	B	"	"			"	"	"	"	"	"	A							
8 2/ 4/ Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and -55°C.																								
9 T _C =+25°C	f _{MAX} 5/ t _{MAX} 5/	(Fig. 6)	60 61	D "	IN IN	5.0 V 5.0 V	5.0 V B	B B		"	2.4 V "	2.4 V "	OUT "	GND "	OUT "	2.4 V "	2.4 V "	Q Q	3 3		MHz			
	t _{PLH} "	3003 (Fig. 4)	*62 CKT A	"	2.4 V	J	"	IN	C					OUT OUT		OUT			Clear/ $\bar{Q}$	10	75	ns		
			*62 CKT B	"	"	J	"	IN											"	"	Clear/Q	"	50	"
			*63 CKT A	"	"	IN	"	J											"	"	Preset/Q	"	75	"
			*63 CKT B	"	"	IN	"	J											"	"	Preset/Q	"	50	"
	t _{PHL} "		64 CKT A	"	GND	J	"	IN	"	"	"	"	"	"	"	"	"	Clear/Q	"	200	"			
			64 CKT B	"	"	J	"	IN	"	"	"	"	"	"	"	"	Clear/Q	"	90	"				
			65 CKT A	"	"	IN	"	J	"	"	"	"	"	"	"	"	Preset/ $\bar{Q}$	"	200	"				
			65 CKT B	"	"	IN	"	J	"	"	"	"	"	"	"	"	Preset/Q	"	90	"				
	t _{PLH} "	3003 (Fig. 5)	66 CKT A	"	IN	J	5.0 V	"	5.0 V	"	"	"	"	"	"	"	"	"	Clock/ $\bar{Q}$	"	75	"		
			66 CKT B	"	"	J	"	5.0 V	"	5.0 V	"	"	"	"	"	"	"	Clock/Q	"	50	"			
			67 CKT A	"	"	5.0 V	"	J	"	"	"	"	"	"	"	"	"	Clock/Q	"	75	"			
			67 CKT B	"	"	5.0 V	"	J	"	5.0 V	"	"	"	"	"	"	"	Clock/Q	"	50	"			
t _{PHL} "		68 CKT A	"	"	J	"	5.0 V	"	"	"	"	"	"	"	"	"	"	Clock/Q	"	150	"			
		68 CKT B	"	"	J	"	5.0 V	"	"	"	"	"	"	"	"	"	Clock/Q	"	70	"				
		69 CKT A	"	"	5.0 V	"	J	"	"	"	"	"	"	"	"	"	Clock/Q	"	150	"				
		69 CKT B	"	"	5.0 V	"	J	"	"	"	"	"	"	"	"	"	Clock/Q	"	70	"				

See footnotes at end of device type 01.

TABLE III. Group A inspection for device type 01 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit	
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max		
			Test no.	R1	Clock	Preset	V _{CC}	Clear	NC	S1	S2	S3	$\overline{Q}$	GND	Q	R2	R3					
10 T _C =+125°C	f _{MAX} 5/ f _{MAX} 5/	(Fig. 5)	70 71	D "	IN IN	5.0 V 5.0 V	5.0 V "	B B	 "	 "	2.4 V "	2.4 V "	 OUT	GND "	OUT "	2.4 V "	2.4 V "	$\frac{Q}{Q}$	3 3		MHz	
	t _{PLH} "	3003 (Fig. 4)	*72 CKT A *72 CKT B *73 CKT A *73 CKT B	" " " "	2.4 V " " "	J J IN IN	" " " "	IN IN J J	 C " "	 " " "	" " " "	" " " "	OUT OUT " "	" " " "	 OUT " "	" " " "	" " " "	Clear/Q Clear/Q Preset/Q Preset/Q	10 " " "	125 65 125 65	ns " " "	
	t _{PHL} "		74 CKT A 74 CKT B 75 CKT A 75 CKT B	" " " "	GND " " "	J J IN IN	" " " "	IN IN J J	 " " "	" " " "	" " " "	" " " "	" " " "	OUT " "	" " " "	" " " "	" " " "	Clear/Q Clear/Q Preset/Q Preset/Q	" " " "	250 100 250 100	" " " "	
	t _{PLH} "		3003 (Fig. 5)	76 CKT A 76 CKT B 77 CKT A 77 CKT B 78 CKT A 78 CKT B 79 CKT A 79 CKT B	" " " " " " " "	IN " " " " " " "	J J 5.0 V 5.0 V J J 5.0 V 5.0 V	" " " " " " " "	5.0 V 5.0 V J J 5.0 V 5.0 V J J	 " " " " " " " "	" " " " " " " "	" " " " " " " "	" " " " " " " "	" " " " " " " "	OUT " " " " " " "	" " " " " " " "	" " " " " " " "	" " " " " " " "	Clock/Q Clock/Q Clock/Q Clock/Q Clock/Q Clock/Q Clock/Q Clock/Q	" " " " " " " "	125 65 125 65 200 85 200 85	" " " " " " " "
	t _{PHL} "																					
	11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																				

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V.
 C = input connected to $\bar{Q}$, D = input connected to Q.
 J = input pulse t_p ≥ 100 ns, PRR = 0.5 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Tests shall be performed in sequence.

3/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.

4/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

* These tests are performed at device manufacturer's option.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max	
			Test no.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	$\bar{Q}$	GND	Q	K2	K3				
1 T _C = +25°C	V _{OH}	3006	1	0.7 V	A	4.5 V	4.5 V	4.5 V		2.0 V	2.0 V	2.0 V		GND	-100μA	0.7 V	0.7 V	$\bar{Q}$	2.4		"
			2	2.0 V	A	4.5 V	"	4.5 V		0.7 V	0.7 V	0.7 V		"	"	2.0 V	2.0 V	$\bar{Q}$	"		"
			3	4.5 V	4.5 V	0.7 V	"	2.0 V		4.5 V	4.5 V	4.5 V		"	-100μA	4.5 V	4.5 V	$\bar{Q}$	"	V	"
			4	4.5 V	4.5 V	2.0 V	"	0.7 V		4.5 V	4.5 V	4.5 V	-100μA	"	"	4.5 V	4.5 V	$\bar{Q}$	"		"
	V _{OL}	3007	5	2.0 V	A	4.5 V	"	4.5 V		0.7 V	0.7 V	0.7 V		"	2 mA	2.0 V	2.0 V	$\bar{Q}$			"
			6	0.7 V	A	4.5 V	"	4.5 V		2.0 V	2.0 V	2.0 V		"	"	0.7 V	0.7 V	$\bar{Q}$			"
			7	4.5 V	4.5 V	0.7 V	"	2.0 V		4.5 V	4.5 V	"		"	"	4.5 V	4.5 V	$\bar{Q}$	0.3	"	"
			8	4.5 V	"	2.0 V	"	0.7 V		4.5 V	"	"		"	2 mA	4.5 V	4.5 V	$\bar{Q}$	"		"
	I _{IL1}	3009	9				5.5 V	B		0.3 V	"	4.5 V		"				J1	-43	-140	μA
			10		"		"	"		4.5 V	0.3 V	4.5 V		"				J2	"	"	"
			11		"		"	"		4.5 V	4.5 V	0.3 V		"				J3	"	"	"
			12	0.3 V	"	B	"	"						"		4.5 V	4.5 V	K1	"	"	"
	I _{IL2}	3009	13	4.5 V	"	"	"	"						"		0.3 V	4.5 V	K2	"	"	"
			14	"	"	"	"	"						"		4.5 V	0.3 V	K3	"	"	"
			15	"	0.3 V	"	"	B		4.5 V	4.5 V	4.5 V		"		"	4.5 V	Clock	-105	-360	"
			16	"	0.3 V	"	"	"		"	"	"		"		"	"	Clock	-105	-360	"
	I _{IH1}	3010	17	"		0.3 V	"	0.3 V		"	"	"		"		"	"	Preset	-86	-280	"
			18	"		"	"	"		"	"	"		"		"	"	Clear	-86	-280	"
			19		GND		"	GND		2.4 V	GND	GND	"	"				J1			"
			20		"		"	"		GND	2.4 V	GND		"				J2			"
I _{IH2}	3010	21		"		"	"		GND	GND	GND		"				J3			"	
		22	2.4 V	"	GND	"	"						"		GND	GND	K1	10		"	
		23	GND	"	"	"	"						"		2.4 V	GND	K2			"	
		24	GND	"	"	"	"						"		GND	2.4 V	K3			"	
I _{IH3}	3010	25		"		"	GND		5.5 V	GND	GND		"				J1			"	
		26		"		"	"		GND	5.5 V	GND		"				J2			"	
		27		"		"	"		"	GND	5.5 V		"				J3			"	
		28	5.5 V	"	GND	"	"						"		GND	GND	K1	100		"	
I _{IH4}	3010	29	GND	"	"	"	"						"		5.5 V	GND	K2			"	
		30	GND	"	"	"	"						"		GND	5.5 V	K3			"	
		31		"		"	2.4 V		GND	GND	GND	GND	"				Clear		20	"	
		32	GND	"	2.4 V	"	"						"		GND	GND	Preset		20	"	
I _{IH10}	3011	33	GND	"	5.5 V	"	5.5 V		GND	GND	"	GND	"		GND	GND	Preset			"	
		34		"		"	"						"				Clear			"	
		35	GND	5.5 V	GND	"	GND		"	"	"	"	"		GND	GND	Clock	200		"	
		36	"	5.5 V	"	"	"		"	"	"	"	"		"	"	Clock			"	
I _{OS}	3011	37	"	2.4 V	GND	"	GND		"	"	"		"		"	"	Clock	0	-200	"	
		38	"	2.4 V	"	"	"		"	"	"		"		"	"	Clock	0	-200	"	
		39	4.5 V	GND	GND	"	GND	"	4.5 V	4.5 V	4.5 V		"	GND	4.5 V	4.5 V	$\bar{Q}$	-3	-15	mA	
		40	4.5 V	"	"	"	"		4.5 V	4.5 V	4.5 V	GND	"	"	4.5 V	4.5 V	$\bar{Q}$	-3	-15	"	
I _{CC}	3005	41 CKT A	GND	"	GND	"	4.5 V			GND	GND		"		"	GND	VCC			"	
		41 CKT B	"	"	GND	"	4.5 V			"	"		"		"	"	"			"	
		42 CKT A	"	"	4.5 V	"	"	GND	"	"	"		"		"	"	"	1.90	1.90	"	
		42 CKT B	"	"	4.5 V	"	GND		"	"	"		"	GND	"	"	"		1.44	"	
2	Same tests, terminal conditions and limits as for subgroup 1, except T _C = +125°C.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C = -55°C.																				

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit		
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max			
			Test no.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3						
7 T _C = +25°C 2/ 4/			43	B	B	A	4.5 V	B	B	B	B	B	H 3/	GND	L 3/	B	B	All outputs	H or L as shown 3/				
			44	"	"	B	"	A	"	"	"	"	"	"	"	B	B						
			45	"	"	A	"	"	"	"	"	"	"	"	"	A	A						
			46	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	
			47	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	
			48	A	"	"	"	"	"	"	"	"	"	"	"	"	"					"	
			49	"	A	"	"	"	"	"	"	"	"	"	"	"	B					"	
			50	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	
			51	"	B	"	"	"	"	"	"	"	"	"	"	"	A					B	
			52	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	
			53	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	
			54	"	"	"	"	"	"	"	"	"	"	"	"	"	"					"	
			55	B	"	"	"	"	"	B	"	"	"	"	H	"	L					B	"
			56	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			57	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			58	"	B	"	"	"	"	"	"	A	B	"	"	"	"					"	"
			59	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			60	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			61	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			62	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			63	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			64	A	B	"	"	"	"	"	"	"	"	"	"	"	"					A	A
			65	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			66	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			67	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			68	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			69	"	B	"	"	"	"	"	B	"	"	"	"	"	"					"	"
			70	"	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			71	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			72	"	B	"	"	B	"	"	"	"	"	"	"	"	"					"	"
			73	A	A	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			74	"	B	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			75	"	A	"	"	"	"	"	A	"	"	"	"	"	"					"	"
			76	"	"	"	"	A	"	"	"	"	"	"	"	"	"					"	"
			77	B	"	"	"	"	"	"	"	"	"	"	"	"	"					"	"
			78	"	"	"	"	"	"	"	"	"	B	"	"	"	"					"	"
			79	"	B	"	"	"	"	"	"	"	B	"	"	"	"					"	"
			80	A	A	"	"	"	"	"	"	"	B	"	"	"	"					"	"
			81	A	A	"	"	"	"	"	"	"	A	"	"	"	"					"	"
8 2/ 3/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T _C =+125°C and -55°C.																						

See footnotes at end of device type 02.

TABLE III. Group A inspection for device type 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit	
			Case C	9	12	13	14	2	1	3	4	5	6	7	8	10	11		Min	Max		
			Test no.	K1	Clock	Preset	V _{CC}	Clear	NC	J1	J2	J3	$\overline{Q}$	GND	Q	K2	K3					
9 T _C =+25°C	f _{MAX} 5/ f _{MAX} 5/	(Fig. 5)	82 83	2.4 V "	IN IN	B B	5.0 V 5.0 V	5.0 V 5.0 V		2.4 V "	2.4 V "	2.4 V "	OUT "	GND "	OUT "	2.4 V "	2.4 V "	$\overline{Q}$ Q	3 3		MHz	
	t _{PLH}	3003 (Fig. 4)	*84 CKT A	"	2.4 V	J	"	IN			"	"	OUT	"	"	"	"	Clear/ $\overline{Q}$	10	75	ns	
	"		*84 CKT B	"	"	J	"	IN		"	"	"	OUT	"	"	"	"	Clear/Q	"	50	"	
	"		*85 CKT A	"	"	IN	"	J		"	"	"	"	"	OUT	"	"	"	Preset/Q	"	75	"
	"		*85 CKT B	"	"	IN	"	J		"	"	"	"	"	"	"	"	"	Preset/Q	"	50	"
	t _{PHL}		86 CKT A	"	GND	J	"	IN		"	"	"	"	"	"	"	"	"	Clear/Q	"	200	"
	"		86 CKT B	"	"	J	"	IN		"	"	"	"	"	"	"	"	"	Clear/Q	"	90	"
	"		87 CKT A	"	"	IN	"	J		"	"	"	OUT	"	"	"	"	"	Preset/ $\overline{Q}$	"	200	"
	"		87 CKT B	"	"	IN	"	J		"	"	"	"	"	"	"	"	"	Preset/Q	"	90	"
	t _{PLH}	3003 (Fig. 5)	88 CKT A	"	IN	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/ $\overline{Q}$	"	75	"
	"		88 CKT B	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	50	"
	"		89 CKT A	"	"	5.0 V	"	J		"	"	"	"	"	OUT	"	"	"	Clock/Q	"	75	"
	"		89 CKT B	"	"	5.0 V	"	J		"	"	"	"	"	"	"	"	"	Clock/Q	"	50	"
	t _{PHL}		90 CKT A	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	150	"
	"		90 CKT B	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	70	"
	"		91 CKT A	"	"	5.0 V	"	J		"	"	"	"	OUT	"	"	"	"	Clock/ $\overline{Q}$	"	150	"
"	91 CKT B		"	"	5.0 V	"	J		"	"	"	"	OUT	"	"	"	"	Clock/Q	"	70	"	
10 T _C =+125°C	f _{MAX} 5/ f _{MAX} 5/	(Fig. 5)	92 93	" "	" "	B B	" "	5.0 V 5.0 V		" "	" "	" "	OUT "	" "	OUT "	" "	" "	$\overline{Q}$ Q	2.5 2.5		MHz	
	t _{PLH}	3003 (Fig. 4)	*94 CKT A	"	2.4 V	J	"	IN		"	"	"	OUT	"	"	"	"	Clear/ $\overline{Q}$	10	125	ns	
	"		*94 CKT B	"	"	J	"	IN		"	"	"	OUT	"	"	"	"	Clear/Q	"	65	"	
	"		*95 CKT A	"	"	IN	"	J		"	"	"	"	"	OUT	"	"	"	Preset/Q	"	125	"
	"		*95 CKT B	"	"	IN	"	J		"	"	"	"	"	"	"	"	"	Preset/Q	"	65	"
	t _{PHL}		96 CKT A	"	GND	J	"	IN		"	"	"	"	"	"	"	"	"	Clear/Q	"	250	"
	"		96 CKT B	"	"	J	"	IN		"	"	"	"	"	"	"	"	"	Clear/Q	"	100	"
	"		97 CKT A	"	"	IN	"	J		"	"	"	OUT	"	"	"	"	"	Preset/ $\overline{Q}$	"	250	"
	"		97 CKT B	"	"	IN	"	J		"	"	"	"	"	"	"	"	"	Preset/Q	"	100	"
	t _{PLH}	3003 (Fig. 5)	98 CKT A	"	IN	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/ $\overline{Q}$	"	125	"
	"		98 CKT B	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	65	"
	"		99 CKT A	"	"	5.0 V	"	J		"	"	"	"	"	"	OUT	"	"	Clock/Q	"	125	"
	"		99 CKT B	"	"	5.0 V	"	J		"	"	"	"	"	"	"	"	"	Clock/Q	"	65	"
	t _{PHL}		100 CKT A	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	200	"
	"		100 CKT B	"	"	J	"	5.0 V		"	"	"	"	"	"	"	"	"	Clock/Q	"	85	"
	"		101 CKT A	"	"	5.0 V	"	J		"	"	"	"	OUT	"	"	"	"	Clock/ $\overline{Q}$	"	200	"
"	101 CKT B		"	"	5.0 V	"	J		"	"	"	"	OUT	"	"	"	"	Clock/Q	"	85	"	
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C =-55°C																					

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V.

J = input pulse, t_p ≥ 100 ns, PRR = 0.5 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Tests shall be performed in sequence.

3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

4/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.

5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

* These tests are performed at device manufacturer's option.

TABLE III. Group A inspection for device type 03. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Test no.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	$\overline{Q}$ 2	Q2	K2	GND	Q1	$\overline{Q}$ 1	J1		Min	Max	
1 T _C =+25°C	V _{OH}	3006	1 2 3 4 5 6	A A 4.5 V	4.5 V 4.5 V 0.7 V	0.7 V 2.0 V 4.5 V	4.5 V " " "	A A 4.5 V	4.5 V 4.5 V 0.7 V	2.0 V 0.7 V 4.5 V	- 100µA - 100µA	-100µA	0.7 V 2.0 V 4.5 V	GND " " "	-100µA	-100µA -100µA	2.0 V 0.7 V 4.5 V	Q1 Q1 Q1 Q2 Q2 Q2	2.4 " " " " "	V	" " " " "
	V _{OL}	3007	7 8 9 10 11 12	A A 4.5 V	4.5 V 4.5 V 0.7 V	2.0 V 0.7 V 4.5 V	" " " "	A A 4.5 V	4.5 V 4.5 V 0.7 V	0.7V 2.0V 4.5 V	2 mA 2 mA	2 mA 2 mA	2.0 V 0.7 V 4.5 V	" " " "	2 mA 2 mA	2 mA	0.7 V 2.0 V 4.5 V	Q1 Q1 Q1 Q2 Q2 Q2	0.3 " " " " "	" " " " " "	
	I _{IL1}	3009	13 14 15 16	4.5 V 4.5 V	4.5 V 4.5 V	0.3 V	5.5V " "	4.5 V 4.5 V	4.5 V 4.5 V	0.3 V	E E	E	0.3 V	" " "	E	E	0.3 V	J1 K1 J2 K2	-43 " " "	-140 " " "	µA " " "
	I _{IL2}		17 18 19 20	4.5 V 0.3 V	0.3 V B	4.5 V	" " "	4.5 V 0.3 V	0.3 V B	4.5 V 4.5 V	" "	" "	4.5 V	" " "	" "	" "	4.5 V 4.5 V	Clear 1 Clock 1 Clear 2 Clock 2	-86 -120 -86 -120	-280 -360 -280 -360	" " " "
	I _{IH1}	3010	21 22 23 24	GND GND	GND B	2.4 V	" " "	GND GND	GND B	2.4 V	" "	" "	2.4 V	" " "	" "	" "	2.4 V	J1 K1 J2 K2	10 " " "	" " " "	" " " "
	I _{IH2}		25 26 27 28	GND GND	GND B	5.5 V	" " "	GND GND	GND B	5.5 V	" "	" "	5.5 V	" " "	" "	" "	5.5 V	J1 K1 J2 K2	100 " " "	" " " "	" " " "
	I _{IH3}		29 30	GND	2.4 V	"	" "	GND	2.4 V	GND	GND	" "	" "	" "	" "	" "	GND	Clear 1 Clear 2	" 20	" "	" "
	I _{IH4}		31 32 33 34	5.5 V GND	GND 5.5 V	GND	" "	5.5 V GND	GND 5.5 V	GND GND	GND	" "	GND	" "	GND GND	GND	GND	Clock 1 Clear 1 Clock 2 Clear 2	20 " 200 "	" " " "	" " " "
	I _{IH10}		35 36	2.4 V	GND	GND	" "	2.4 V	GND	GND	" "	" "	GND	" "	" "	" "	GND	Clock 1 Clock 2	0 0	-200 -200	" "
	I _{OS}	3011 3011** 3011** 3011	37 38 39 40	2.4 V A	GND 2.4 V	2.4 V GND	" "	A 2.4 V	2.4 V GND	2.4 V 2.4 V	GND GND	GND	GND 2.4 V	" "	GND	GND	2.4 V 2.4 V	Q1 Q1 Q2 Q2	-3 " " "	-15 " " "	mA " " "
	I _{CC}	3005	41 CKT A 41 CKT B 42 CKT A 42 CKT B	F F GND GND	4.5 V 4.5 V GND GND	GND " "	" " "	F F GND GND	4.5 V 4.5 V GND GND	4.5 V 4.5 V GND GND	" "	" "	GND " "	" "	" "	" "	4.5 V 4.5 V GND GND	V _{CC} " " "	3.8 2.88 3.8 2.88	" " " "	" " " "
2	Same tests, terminal conditions and limits as for subgroup 1, except T _C =+125°C and I _{IL2} = -50 µA min/-360 µA max for Clock 1 and Clock 2.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C =-55°C.																				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03. Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Test no.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	$\overline{Q}$ 2	Q2	K2	GND	Q1	$\overline{Q}$ 1	J1		Min	Max	
7 T _C =+25°C 2/ 4/			43	B	B	B	4.5 V	B	B	A	H 3/	L 3/	B	GND	L 3/	H 3/	A	All outputs	H or L as shown 3/		
			44	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			45	B	"	"	"	B	"	"	"	"	"	"	"	"	"				"
			46	B	"	"	A	"	B	"	"	"	A	"	"	"	"				"
			47	A	"	"	"	"	B	"	"	"	"	"	"	"	"				"
			48	B	"	"	"	"	B	"	"	"	"	"	"	"	"				"
			49	B	A	"	"	B	A	"	"	"	"	"	"	"	"				"
			50	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			51	B	"	"	"	B	"	"	"	"	"	"	"	"	"				"
			52	A	"	"	"	A	"	"	L	H	"	"	H	L	"				"
			53	B	"	"	"	B	"	"	L	H	"	"	H	L	"				"
			54	A	"	"	"	A	"	"	H	L	"	"	L	H	"				"
			55	B	"	"	"	B	"	"	H	L	"	"	H	L	"				"
			56	B	"	B	"	B	"	B	"	"	B	"	"	"	B				"
			57	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			58	B	"	"	"	B	"	"	"	"	"	"	"	"	"				"
			59	"	B	"	"	"	B	"	H	L	"	"	L	H	"				"
			60	"	A	"	"	"	A	"	"	"	"	"	"	"	"				"
			61	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			62	B	"	"	"	B	"	"	"	"	"	"	"	"	"				"
			63	"	"	"	"	B	"	A	"	"	"	"	"	"	"				A
			64	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			65	B	"	"	"	B	"	"	L	H	"	"	H	L	"				"
			66	B	"	A	"	B	"	B	"	"	A	"	"	"	B				"
			67	A	"	"	"	A	"	"	"	"	"	"	"	"	"				"
			68	B	"	"	"	B	"	"	H	L	"	"	L	H	"				"
			69	A	B	"	"	A	B	A	"	"	"	"	"	"	A				"
			70	"	A	"	"	"	A	A	"	"	"	"	"	"	A				"
			71	"	"	"	"	"	B	B	"	"	"	"	"	"	B				"
			72	"	"	B	"	"	"	"	"	"	"	"	B	"	"				"
			73	B	"	B	"	B	"	B	"	"	"	L	H	B	A				"
			74	A	"	A	"	A	"	A	"	"	A	"	"	A	"				A
			75	"	"	B	"	"	"	"	"	"	A	"	"	B	"				"
			76	"	"	"	"	"	"	"	"	"	B	"	"	"	"				B
			77	B	"	"	"	"	"	B	"	"	B	H	L	"	L				H
			78	A	"	"	"	"	"	A	"	"	A	H	L	"	L				H
			79	B	"	"	"	"	"	B	"	"	"	L	H	"	H				L
			80	A	"	"	"	"	"	A	"	"	"	L	H	"	H				L
			81	A	B	"	"	"	B	"	"	B	"	H	L	"	L				H
8 2/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T _C =+125°C and -55°C.																				

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03. Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
				Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	$\bar{Q}$ 2	Q2	K2	GND	Q1	$\bar{Q}$ 1	J1		Min	Max	
9 T _C =+25°C	f _{MAX} 5/	(Fig. 7)	82	IN	B	2.4 V	5.0 V							GND	OUT		2.4 V	Clock/Q1	3		MHz
			83	IN	B	2.4 V											2.4 V	Clock/Q1			
			84					IN	B	2.4 V		OUT	2.4 V					Clock/Q2			
			85						B	2.4 V			2.4 V					Clock/Q2			
	t _{PLH}	3003 (Fig. 6)	*86 CKT A	IN	IN	GND											2.4 V	Clear/Q1	10	75	ns
			*86 CKT B	IN	IN	GND												Clear/Q1		50	
			*87 CKT A					IN	IN	2.4 V	OUT		GND		OUT			Clear/Q2		75	
			*87 CKT B						IN	2.4 V	OUT		GND					Clear/Q2		50	
	t _{PHL}	3003 (Fig. 7)	88 CKT A	IN	IN	GND									OUT		2.4 V	Clear1/Q1		200	
			88 CKT B	IN	IN	GND									OUT		2.4 V	Clear1/Q1		105	
			89 CKT A					IN	IN	2.4 V		OUT	GND					Clear2/Q2		200	
			89 CKT B						IN	2.4 V			GND					Clear2/Q2		105	
	t _{PLH}	3003 (Fig. 7)	90 CKT A	IN	J	2.4 V										OUT	2.4 V	Clock1/Q1		150	
			90 CKT B													OUT		Clock1/Q1		75	
			91 CKT A															Clock1/Q1		150	
			91 CKT B															Clock1/Q1		75	
	t _{PLH}	3003 (Fig. 7)	92 CKT A															Clock1/Q1		75	
			92 CKT B															Clock1/Q1		50	
			93 CKT A													OUT		Clock1/Q1		75	
			93 CKT B													OUT		Clock1/Q1		50	
	t _{PHL}	3003 (Fig. 7)	94 CKT A					IN	J	2.4 V		OUT	2.4 V					Clock2/Q2		75	
			94 CKT B									OUT						Clock2/Q2		50	
			95 CKT A															Clock2/Q2		75	
			95 CKT B															Clock2/Q2		50	
10 T _C =+125°C	f _{MAX} 5/	(Fig. 7)	98	IN	B	2.4 V									OUT		2.4 V	Clock/Q1	2.5		MHz
			99	IN	B	2.4 V											2.4 V	Clock/Q1			
			100					IN	B	2.4 V		OUT	2.4 V					Clock/Q2			
			101						B	2.4 V			2.4 V					Clock/Q2			
	t _{PLH}	3003 (Fig. 6)	*102 CKT A	IN	IN	GND											2.4 V	Clear1/Q1	10	125	ns
			*102 CKT B	IN	IN	GND											2.4 V	Clear1/Q1		65	
			*103 CKT A					IN	IN	2.4 V	OUT		GND		OUT			Clear2/Q2		125	
			*103 CKT B						IN	2.4 V	OUT		GND					Clear2/Q2		65	
	t _{PHL}	3003 (Fig. 7)	104 CKT A	IN	IN	GND									OUT		2.4 V	Clear1/Q1		250	
			104 CKT B	IN	IN	GND									OUT		2.4 V	Clear1/Q1		105	
			105 CKT A					IN	IN	2.4 V		OUT	GND					Clear2/Q2		250	
			105 CKT B						IN	2.4 V			GND					Clear2/Q2		105	
	t _{PLH}	3003 (Fig. 7)	106 CKT A	IN	J	2.4 V										OUT	2.4 V	Clock1/Q1		200	
			106 CKT B													OUT		Clock1/Q1		85	
			107 CKT A												OUT			Clock1/Q1		200	
			107 CKT B												OUT			Clock1/Q1		85	

See footnotes at end of device type 03.

TABLE III. Group A inspection for device type 03. Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
				Test no.	Clock 1	Clear 1	K1	V _{CC}	Clock 2	Clear 2	J2	$\overline{Q}$ 2	Q2	K2	GND	Q1	$\overline{Q}$ 1		J1	Min	
10 T _C =+125°C	t _{PLH}	3003 (Fig. 7)	108 CKT A	IN	J	2.4 V	5.0 V							GND	OUT	OUT	2.4 V	Clock1/Q1	10	125	ns
			108 CKT B	"	"	"	"							"	"	"	"	Clock1/ $\overline{Q}$ 1	"	65	"
			109 CKT A	"	"	"	"							"	"	OUT	"	Clock1/Q1	"	125	"
			109 CKT B	"	"	"	"							"	"	OUT	"	Clock1/ $\overline{Q}$ 1	"	65	"
			110 CKT A				"	IN	J	2.4 V		OUT	2.4 V	"	"	"	"	Clock2/Q2	"	125	"
			110 CKT B				"	"	"	"		"	"	"	"	"	"	Clock2/Q2	"	65	"
			111 CKT A				"	"	"	"	"	OUT	"	"	"	"	"	Clock2/ $\overline{Q}$ 2	"	125	"
			111 CKT B				"	"	"	"	"	"	"	"	"	"	"	Clock2/ $\overline{Q}$ 2	"	65	"
	t _{PHL}		112 CKT A				"	"	"	"	"	"	"	"	"			Clock2/ $\overline{Q}$ 2		200	"
			112 CKT B				"	"	"	"	"	"	"	"	"			Clock2/ $\overline{Q}$ 2		85	"
			113 CKT A				"	"	"	"	"	"	OUT	"	"			Clock2/ $\overline{Q}$ 2		200	"
			113 CKT B				"	"	"	"	"	"	OUT	"	"			Clock2/ $\overline{Q}$ 2		85	"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C.																				

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V, E = momentary GND, then open.
F = momentary 4.5 V, then GND. J = input pulse, t_p ≥ 100 ns, PRR = 0.5 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

- 1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).
2/ Tests shall be performed in sequence.
3/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or (b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.
4/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.
5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
* These tests are performed at device manufacturer's option.
** Test time limit ≤ 100 ns.

TABLE III. Group A inspection for device type 04. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit	
			Test no.	Clock	Preset 1	J1	V _{CC}	Clear	Preset 2	K2	Q2	$\overline{Q}$ 2	J2	GND	$\overline{Q}$ 1	Q1	K1		Min	Max		
1 T _C =+25°C	V _{OH}	3006	1	A	4.5 V	2.0 V	4.5 V	4.5 V						GND		-100μA	0.7 V	Q1	2.4		V	
			2	A	4.5 V	0.7 V	"	"						"		-100μA	2.0 V	Q1	"			
			3	4.5 V	0.7 V	4.5 V	"	"						"		-100μA	4.5 V	Q1	"			
			4	"	4.5 V	4.5 V	"	0.7 V						"			4.5 V	Q1	"			
			5	"			"	0.7 V	4.5 V	4.5 V	-100μA	-100μA	4.5 V	"				Q2	"			
			6	"			"	4.5 V	0.7 V	4.5 V	-100μA	-100μA	4.5 V	"				Q2	"			
			7	A			"	4.5 V	2.0 V	0.7 V			0.7 V	"				Q2	"			
			8	"			"	"	4.5 V	0.7 V	-100μA		2.0 V	"				Q2	"			
	V _{OH}	3007	9	"	4.5 V	0.7 V	"	"							"		2 mA	2.0 V	Q1			
			10	"	"	2.0 V	"	"						"			0.7 V	Q1				
			11	4.5 V	"	4.5 V	"	0.7 V						"	2 mA		4.5 V	Q1	0.3			
			12	"	0.7 V	4.5 V	"	4.5 V	4.5 V	4.5 V	2 mA	2 mA	4.5 V	"			4.5 V	Q1				
			13	"			"	0.7 V	4.5 V	2.0 V			0.7 V	"				Q2				
			14	"			"	4.5 V	0.7 V	0.7 V	2 mA	2 mA	2.0 V	"				Q2				
			15	A			"	"	4.5 V	2.0 V			0.7 V	"				Q2				
			16	"			"	"	4.5 V	0.7 V			2.0 V	"				Q2				
	I _{IL1}	3009	17	4.5 V		0.3 V	5.5 V	"	GND	GND			GND	"		E	E	J1	-43	-140	μA	
			18	"			"	"	GND	GND	E	E	GND	"			0.3 V	K1	"	"		
	19		"	GND	GND	"	"		0.3 V				"			GND	J2	"	"			
	20		"	GND	GND	"	"						"			GND	K2	"	"			
	I _{IL2}		21	4.5 V	0.3 V		"		0.3 V	4.5 V				"			4.5 V	Preset 1	-86	-280	"	
	I _{IL2}		22	4.5 V			"							"				Preset 2	-86	-280	"	
	I _{IL3}		23	0.3 V		4.5 V	"	B						"			4.5 V	Clock	-172	-560	"	
	I _{IL3}		24	4.5 V		4.5 V	"	0.3 V		"			4.5 V	"			4.5 V	Clear	-172	-560	"	
	I _{IH1}	3010	25	GND	B	2.4 V	"	GND							"				J1			
			26	"	B		"	B	"	2.4 V					"			2.4 V	K1			
			27	"	GND		"	B	GND						"			K2				
			28	"			"	GND	B				2.4 V	"				J2	10			
	I _{IH2}		29	"	B	5.5 V	"	GND	B					"				J1				
			30	"	GND		"	B		5.5 V				"				K1				
	31		"	"		"	B	GND					"				K2					
	32		"			"	GND	B				5.5 V	"				J2	100				
	I _{IH3}		33	"	2.4 V		"	"	2.4 V	GND				"			GND	Preset 1		20		
	I _{IH3}		34	"			"	"						"				Preset 2		20		
	I _{IH4}		35	"	5.5 V		"	"	5.5 V	GND				"				GND	Preset 1		200	
	I _{IH4}		36	"			"	"						"				Preset 2		200		
	I _{IH7}		37	"	GND	GND	"	2.4 V	GND					GND	"				Clear		40	
	I _{IH8}		38	"	GND	"	"	5.5 V	GND					"	"				Clear		400	
	I _{IH9}		39	2.4 V			"	"	GND					"	"				Clock		-400	
	I _{IH8}		40	5.5 V			"	"	GND					"	"				Clock		400	
	I _{OS}	3011	41	4.5 V	GND	4.5 V	"			GND	4.5 V			4.5 V	"	GND	GND	4.5 V	Q1	-3	-15	mA
			42	"		"	"	GND	GND	"			"	"		GND	GND	"	Q1	"	"	
			43	"		"	"	GND	GND	"			GND	"			"	Q2	"	"		
			44	"		"	"	"	"	GND	"			"	"		"	Q2	"	"		

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04.- Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit	
				Test no.	Clock	Preset 1	J1	V _{CC}	Clear	Preset 2	K2	Q2	$\overline{Q}$ 2	J2	GND	$\overline{Q}$ 1	Q1		K1	Min		Max
1 T _C =+25°C	I _{CC}	3005	45 CKT A 45 CKT B 46 CKT A 46 CKT B	GND " " "	4.5 V 4.5 V GND GND	GND " " "	5.5 V " " "	GND GND 4.5 V 4.5 V	4.5 V 4.5 V GND GND	GND " " "			GND " " "	GND " " "		$\overline{Q}$ 1	Q1 " " "	GND " " "	V _{CC} " " "	3.80	2.88 3.80 2.88	mA " " "
2	Same tests, terminal conditions and limits as for subgroup 1, except T _C = +125°C.																					
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C = -55°C.																					
7 T _C =+25°C 2/ 4/			47 48 49 50 51 52 53 54 55 56 57	A A B A B A B A B " "	B A " " " " " " " B A B	B " " " " " A " B B " B	4.5 V " " " " " " " " " B A	A " " " " " " " " " B A	B A " " " " " " A B B A	A " " " " " " " " " A B H L	H 3/ H L " " " " H H L H H	L 3/ L H " " " " L L H L H	B " " " " " A " B B " B	GND " " " " " " " " " " "	L 3/ L H " " " " L L H L H	H 3/ H L " " " " H H L L L	A " " " " " " " " " A A B B	All outputs	H or L as shown 3/			
8 2/ 4/	Same tests, terminal conditions, and limits as for subgroup 7, except T _C = +125°C and -55°C.																					
9 T _C =+25°C	f _{MAX} 5/	(Fig.9)	58 59 60 61	IN " " "	2.4 V 2.4 V	2.4 V 2.4 V	5.0 V " "	B " "					2.4 V 2.4 V	GND " "	OUT "	OUT	2.4 V 2.4 V	Clock/Q1 Clock/Q1 Clock/Q2 Clock/Q2	3 " MHz		"	
	t _{PLH}	3003 (Fig. 8)	*62 CKT A *62 CKT B *63 CKT A *63 CKT B *64 CKT A *64 CKT B *65 CKT A *65 CKT B	2.4 V " " " " " " "	J J IN IN	2.4V " " "	" " " " " " " "	IN IN J IN IN IN J J					2.4 V " " "	" " " " " " " "	OUT OUT " " OUT OUT	OUT OUT OUT OUT	2.4 V " " "	Clear/ $\overline{Q}$ 1 Clear/Q1 Preset 1/Q1 Preset 1/Q1 Clear/Q2 Clear/Q2 Preset 2/Q2 Preset 2/Q2	10 " " " " " " "	75 50 75 50 75 50 75 50	ns " " " " " " " "	
	t _{PHL}		66 CKT A 66 CKT B 67 CKT A 67 CKT B 68 CKT A 68 CKT B 69 CKT A 69 CKT B	GND " " " " " " "	J J IN IN	2.4 V " " "	" " " " " " " "	IN IN J IN IN IN J J					2.4 V " " "	" " " " " " " "	OUT OUT " " OUT OUT	OUT OUT OUT OUT	2.4 V " " "	Clear/Q1 Clear/Q1 Preset 1/Q1 Preset 1/Q1 Clear/Q2 Clear/Q2 Preset 2/Q2 Preset 2/Q2	" " " " " " " "	200 90 200 90 200 90 200 90	" " " " " " " "	
	t _{PLH}		3003 (Fig. 9)	70 CKT A 70 CKT B 71 CKT A 71 CKT B 72 CKT A 72 CKT B 73 CKT A 73 CKT B	IN " " " " " " "	2.4 V 2.4 V J J	2.4 V " " "	" " " " " " " "	J J 4.5 V 4.5 V J J 4.5 V 4.5 V					2.4 V 2.4 V " "	" " " " " " " "	OUT OUT " " OUT OUT	OUT OUT OUT OUT	2.4 V " " "	Clock1/Q1 Clock1/Q1 Clock1/Q1 Clock1/Q1 Clock2/Q2 Clock2/Q2 Clock2/Q2 Clock2/Q2	" " " " " " " "	75 50 75 50 75 50 75 50	" " " " " " " "

See footnotes at end of device type 04.

TABLE III. Group A inspection for device type 04.- Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,C,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit		
				Test no.	Clock	Preset 1	J1	V _{CC}	Clear	Preset 2	K2	Q2	$\overline{Q}$ 2	J2	GND	$\overline{Q}$ 1	Q1		K1	Min		Max	
9 T _C =+25°C	t _{PLH}	3003 (Fig. 9)	74 CKT A	IN	J	2.4 V	5.0 V	4.5 V							GND		OUT	2.4 V	Clock1/Q1	10	150	ns	
			74 CKT B	"	J	"	"	4.5 V							"		OUT	"	Clock1/Q1	"	70	"	
			75 CKT A	"	2.4 V	"	"	J							"	OUT	"	"	Clock1/Q1	"	150	"	
			75 CKT B	"	2.4 V	"	"	J							"	OUT	"	"	Clock1/Q1	"	70	"	
			76 CKT A	"			"	4.5 V	J	2.4 V	OUT			2.4 V	"			"	Clock2/Q2	"	150	"	
			76 CKT B	"			"	4.5 V	J	"	OUT			"	"			"	Clock2/Q2	"	70	"	
			77 CKT A	"			"	J	4.5 V	"	OUT	OUT		"	"			"	Clock2/Q2	"	150	"	
			77 CKT B	"			"	J	4.5 V	"	"			"	"			"	Clock2/Q2	"	70	"	
10 T _C =+125°C	f _{MAX} 5/	(Fig. 9)	78	"	2.4 V	2.4 V	"	B						"		OUT	OUT	2.4 V	Clock/Q1	2.5		"	
			79	"	2.4 V	2.4 V	"	"						"			2.4 V	Clock/Q1	"		"		
			80	"			"	"	2.4 V	2.4 V	OUT			2.4 V	"			"	Clock/Q2	"	MHz	"	
			81	"			"	"	2.4 V	2.4 V	"	OUT		2.4 V	"			"	Clock/Q2	"		"	
	t _{PLH}	3003 (Fig. 8)	*82 CKT A	2.4	J	2.4 V	"	IN							"	OUT	OUT	2.4 V	Clear/Q1	10	125	ns	
			*82 CKT B	"	J	"	"	IN						"				"	Clear/Q1	"	65	"	
			*83 CKT A	"	IN	"	"	J						"			OUT	"	Preset 1/Q1	"	125	"	
			*83 CKT B	"	IN	"	"	J	J	2.4 V		OUT		2.4 V	"			"	Preset 1/Q1	"	65	"	
			*84 CKT A	"			"	IN	J	"		OUT		"	"			"	Clear/Q2	"	125	"	
			*84 CKT B	"			"	IN	J	"		OUT		"	"			"	Clear/Q2	"	65	"	
			*85 CKT A	"			"	J	IN	"	OUT			"	"			"	Preset 2/Q2	"	125	"	
			*85 CKT B	"			"	J	IN	"	OUT			"	"			"	Preset 2/Q2	"	65	"	
	t _{PHL}		86 CKT A	GND	J	2.4 V	"	IN							"		OUT	OUT	2.4 V	Clear/Q1	"	250	"
			86 CKT B	"	J	"	"	IN						"				"	Clear/Q1	"	100	"	
			87 CKT A	"	IN	"	"	J						"		OUT	OUT	"	Preset 1/Q1	"	250	"	
			87 CKT B	"	IN	"	"	J						"				"	Preset 1/Q1	"	100	"	
			88 CKT A	"			"	IN	J	2.4 V		OUT		2.4 V	"			"	Clear/Q2	"	250	"	
			88 CKT B	"			"	IN	J	"		OUT		"	"			"	Clear/Q2	"	100	"	
			89 CKT A	"			"	J	IN	"				"	"			"	Preset 2/Q2	"	250	"	
			89 CKT B	"			"	J	IN	"		OUT		"	"			"	Preset 2/Q2	"	100	"	
	t _{PLH}	3003 (Fig. 9)	90 CKT A	IN	2.4 V	2.4 V	"	J							"		OUT	OUT	2.4 V	Clock/Q1	"	125	ns
			90 CKT B	"	2.4 V	"	"	J						"				"	Clock/Q1	"	65	"	
			91 CKT A	"	J	"	"	4.5 V						"		OUT	OUT	"	Clock/Q1	"	125	"	
			91 CKT B	"	J	"	"	4.5 V						"				"	Clock/Q1	"	65	"	
			92 CKT A	"			"	J	2.4 V	2.4 V	OUT			2.4 V	"			"	Clock/Q2	"	125	"	
			92 CKT B	"			"	J	2.4 V	"	OUT			"	"			"	Clock/Q2	"	65	"	
			93 CKT A	"			"	4.5 V	J	"		OUT		"	"			"	Clock/Q2	"	125	"	
			93 CKT B	"			"	4.5 V	J	"				"	"			"	Clock/Q2	"	65	"	
	t _{PHL}		94 CKT A	"	J	2.4 V	"	4.5 V							"		OUT	OUT	2.4 V	Clock/Q1			"
			94 CKT B	"	J	"	"	4.5 V						"				"	Clock/Q1		85	"	
			95 CKT A	"	2.4 V	"	"	J						"		OUT	OUT	"	Clock/Q1	200	200	"	
			95 CKT B	"	2.4 V	"	"	J						"				"	Clock/Q1		85	"	
			96 CKT A	"			"	4.5 V	J	2.4 V	OUT			2.4 V	"			"	Clock/Q2		200	"	
			96 CKT B	"			"	4.5 V	J	"				"	"			"	Clock/Q2		85	"	
			97 CKT A	"			"	J	4.5 V	"		OUT		"	"			"	Clock/Q2		200	"	
			97 CKT B	"			"	J	4.5 V	"		OUT		"	"			"	Clock/Q2		85	"	
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C =-55°C.																						

See footnotes on next page.

TABLE III. Group A inspection for device type 04.- Continued. 1/

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V, E = momentary GND, then open.
J = input pulse, $t_p \geq 100$ ns, $V_{OL} = 0$ V, $V_{OH} = 4.5$ V.

- 1/ Terminal conditions (pins not designated may be $H \geq 2.0$ V, or $L \leq 0.8$ V, or open).
- 2/ Tests shall be performed in sequence.
- 3/ Output voltages shall be either: (a) $H = 2.4$ V, minimum and $L = 0.4$ V, maximum when using a high speed checker double comparator; or
(b) $H \geq 1.5$ V and $L \leq 1.5$ V when using a high speed checker single comparator.
- 4/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.
- 5/ f_{MAX} , minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.
- * These tests are performed at device manufacturer's option.

TABLE III. Group A inspection for device type 05. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1				
1 T _C =+25°C	V _{OH}	3006	1	A	2.0 V	4.5 V	4.5 V							GND		-100µA	4.5 V	Q1	2.4		V
			2	A	0.7 V	4.5 V	"								"	-100µA	4.5 V	Q1	"		
			3			0.7 V	"								"	-100µA	2.0 V	Q1	"		
			4			2.0 V	"								"		0.7 V	Q1	"		
			5				"	4.5 V	2.0 V	A	4.5 V	-100µA			"			Q2	"		
			6				"	4.5 V	0.7 V	A	4.5 V				"			Q2	"		
			7				"	0.7 V			2.0 V				"			Q2	"		
			8				"	2.0 V			0.7 V				"			Q2	"		
	V _{OL}	3007	9	A	2.0 V	4.5 V	"								"	2 mA	4.5 V	$\overline{Q1}$			0.3
			10	A	0.7 V	4.5 V	"								"		4.5 V	Q1			
			11			0.7 V	"								"	2 mA	2.0 V	Q1			
			12			2.0 V	"								"		0.7 V	Q1			
			13				"	4.5 V	2.0 V	A	4.5 V	2 mA			"			Q2			
			14				"	4.5 V	0.7 V	A	4.5 V				"			Q2			
			15				"	0.7 V			2.0 V				"			Q2			
			16				"	2.0 V			0.7 V				"			Q2			
	I _{IL4}	3009	17	4.5 V	0.3 V	4.5 V	5.5 V								"		GND	D1	-60	-180	µA
			18	GND	GND	4.5 V	"	4.5 V	0.3 V	4.5 V	GND				"	0.3 V	Preset 1	"	"		
	19					"	4.5 V	GND		0.3 V				"			D2	"	"		
	20					"	4.5 V		4.5 V	GND	0.3 V			"			Preset 2	"	"		
I _{IL5}		21	0.3 V	GND	4.5 V	"								"		GND	Clock 1	-120	-360		
		22	4.5 V	4.5 V	0.3 V	"	4.5 V	GND	0.3 V	GND				"		4.5 V	Clear 1	"	"		
23					"								"			Clock 2	"	"			
24					"								"			Clear 2	"	"			
I _{IH1} I _{IH1}	3010	25	4.5 V	2.4 V	GND	"								"		4.5 V	D1			10	
		26				"	GND	2.4 V	4.5 V	4.5 V				"			D2				
I _{IH2} I _{IH2}		27	4.5 V	5.5 V	GND	"								"		4.5 V	D1			10	100
		28				"	GND	5.5 V	4.5 V	4.5 V				"			D2				
I _{IH3}		29	2.4 V	4.5 V	GND	"									"		4.5 V	Clock 1	100	20	
		30	B	4.5 V	4.5 V	"	GND	4.5 V	2.4 V	4.5 V				"		2.4 V	Preset 1	"	"		
		31				"								"			Clock 2	"	"		
		32				"	4.5 V	4.5 V	B	2.4 V	4.5 V			"			Preset 2	"	"		
I _{IH4}	33	5.5 V	4.5 V	GND	"									"		4.5 V	Clock 1		200		
	34	B	4.5 V	4.5 V	"	GND	4.5 V	5.5 V	4.5 V				"		5.5 V	Preset 1	"	"			
	35				"								"			Clock 2	"	"			
	36				"	4.5 V	4.5 V	B	5.5 V	5.5 V			"			Preset 2	"	"			
I _{IH5} I _{IH5}	3011	37	B	GND	2.4 V	"								"			Clear 1			30	
		38				"	2.4 V	GND	B					"			Clear 2				
I _{IH6} I _{IH6}		39	B	GND	5.5 V	"								"			Clear 1			300	-15
		40				"	5.5 V	GND	B					"			Clear 2				
I _{OS}		41			GND	"									"	GND	GND	Q1	-3	-15	mA
		42				"								"			Q1	"	"		
		43				"								"			Q2	"	"		
		44				"	GND							"			Q2	"	"		
I _{CC} I _{CC}	3005	45	GND	GND	4.5 V	"	4.5 V	GND	GND	GND				"		GND	V _{CC}		3.0	3.0	
	3005	46	GND	GND	GND	"	GND	GND	GND	4.5 V				"		4.5 V	V _{CC}		3.0		
2	Same tests, terminal conditions and limits as for subgroup 1, except T _C =+125°C and I _{IL4} = -50 µA min/-180 µA max for Preset 1 and Preset 2.																				
3	Same tests, terminal conditions and limits as for subgroup 1, except T _C =-55°C																				

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit		
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max			
			Test no.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1						
7 T _C =+25°C 2/ 3/			47	B	B	B	4.5 V	B	B	B	B	H 4/	H 4/	GND	H 4/	H 4/	B	All outputs	H or L as shown 3/				
			48	"	"	B	"	B	"	"	A	L	"	"	"	L	A						
			49	"	"	A	"	A	"	"	A	L	"	"	"	L	A					"	
			50	"	"	"	"	"	"	"	B	H	L	"	"	L	B					"	
			51	A	"	"	"	"	"	A	"	"	L	"	"	L	"					"	
			52	"	"	B	"	B	"	"	"	"	H	"	"	H	"					"	
			53	"	A	"	"	"	A	"	"	"	"	"	"	"	"					"	
			54	"	"	"	"	"	"	"	A	L	"	"	"	L	A					"	
			55	"	"	A	"	A	"	"	A	B	L	"	"	L	A					"	
			56	"	"	"	"	"	"	"	"	H	L	"	"	L	B					"	
			57	"	"	"	"	"	"	"	"	A	"	"	"	"	A					"	
			58	B	"	"	"	"	"	"	"	"	"	"	"	"	"					"	
			59	B	B	B	"	"	B	B	"	"	"	"	"	"	"					"	
			60	A	"	"	"	"	"	A	"	L	H	"	"	H	L					"	
			61	"	"	"	"	"	"	"	B	H	L	"	"	L	B					"	
			62	"	A	B	"	B	A	"	"	"	"	"	"	"	"					"	
			63	"	B	"	"	"	B	"	"	"	"	"	"	"	"					"	
			64	"	"	"	"	"	"	"	A	L	"	"	"	"	L					A	
			65	"	"	A	"	A	"	"	"	"	"	"	"	"	"					"	
			66	B	A	"	"	A	B	"	"	"	"	"	"	"	"					"	
			67	A	"	"	"	"	"	A	"	H	L	"	"	L	"					"	
			68	"	"	"	"	"	"	"	B	"	"	"	"	"	B					"	
			69	"	"	"	"	"	"	"	A	"	"	"	"	"	A					"	
70	"	"	B	"	B	"	"	"	L	H	"	"	H	L	"								
71	"	"	A	"	A	"	"	"	L	H	"	"	H	L	"								
72	"	B	"	"	"	B	"	B	H	L	"	"	L	B	"								
73	"	B	"	B	"	B	"	A	H	L	"	"	L	H	A	"							
8 2/ 3/ Same tests, terminal conditions, and limits as for subgroup 7, except T _C =+125°C and -55°C.																							
9 T _C =+25°C	f _{MAX} 5/	(Fig. 12)	74	IN	IN(H)	5.0 V	5.0 V							GND		OUT	OUT	B	Clock1/Q1	3			
			75	IN	IN(G)	5.0 V						B	OUT			"	OUT	B	Clock1/Q1	"			
			76					5.0 V	IN(H)	IN	B					"				Clock2/Q2	"	MHz	
			77					5.0 V	IN(G)	IN	B					"				Clock2/Q2	"		
	t _{PLH}	3003 (Fig. 10)	78 CKT A			IN									"	OUT		J	Clear1/Q1	10	75	ns	
			78 CKT B			IN									"	OUT		J	Clear1/Q1	"	65		
			79 CKT A			J					J				"		OUT	IN	Preset 1/Q1	"	75		
			79 CKT B			J					J				"		OUT	IN	Preset 1/Q1	"	65		
			80 CKT A					IN			J		OUT		"				Clear2/Q2	"	75		
			80 CKT B					IN			J		OUT		"				Clear2/Q2	"	65		
			81 CKT A					J			J	IN	OUT		"				Preset 2/Q2	"	75		
			81 CKT B					J			J	IN	OUT		"				Preset 2/Q2	"	65		
	t _{PHL}		82 CKT A			IN									"	OUT		J	Clear1/Q1	"	150		
			82 CKT B			IN									"	OUT		J	Clear1/Q1	"	100		
			83 CKT A			J									"		OUT	IN	Preset 1/Q1	"	150		
			83 CKT B			J									"		OUT	IN	Preset 1/Q1	"	100		
			84 CKT A					IN			J	OUT			"				Clear2/Q2	"	150		
			84 CKT B					IN			J	OUT			"				Clear2/Q2	"	100		
			85 CKT A					J			J		OUT		"				Preset 2/Q2	"	150		
			85 CKT B					J			J	IN	OUT		"				Preset 2/Q2	"	100		

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\bar{Q}$ 2	GND	$\bar{Q}$ 1	Q1	Preset 1				
9 T _C =+25°C	t _{PLH}	3003 (Fig. 11)	86 CKT A	IN	IN(G)	B	5.0 V							"		OUT	5.0 V	Clock1/Q1	10	100	ns
			86 CKT B	IN	IN(G)	B	"	B	IN(G)	IN	5.0 V	OUT		"			5.0 V	Clock1/Q1	"	72	"
			87 CKT A				"	B	IN(G)	IN	5.0 V	OUT	GND	"	OUT			Clock2/Q2	"	100	"
			87 CKT B				"	B	IN(G)	IN	5.0 V	OUT		"				Clock2/Q2	"	72	"
	t _{PHL}	3003 (Fig. 11)	88 CKT A	IN	IN(H)	B	"						"	OUT		5.0 V	Clock1/Q1	"	150	"	
			88 CKT B	IN	IN(H)	B	"	B	IN(H)	IN	5.0 V		"	OUT		5.0 V	Clock1/Q1	"	110	"	
			89 CKT A				"	B	IN(H)	IN	5.0 V	OUT		"			Clock2/Q2	"	150	"	
			89 CKT B				"	B	IN(H)	IN	5.0 V	OUT		"			Clock2/Q2	"	110	"	
t _{PLH}	3003 (Fig. 12)	90 CKT A	IN	IN(G)	5.0 V	"						"	OUT		B	Clock1/Q1	"	100	"		
		90 CKT B	IN	IN(G)	5.0 V	"	5.0 V	IN(G)	IN	B		"	OUT			Clock1/Q1	"	72	"		
		91 CKT A				"	5.0 V	IN(G)	IN	B	OUT		"			Clock2/Q2	"	100	"		
		91 CKT B				"	5.0 V	IN(G)	IN	B	OUT		"	B		Clock2/Q2	"	72	"		
t _{PHL}	3003 (Fig. 12)	92 CKT A	IN	IN(H)	5.0 V	"						"			B	Clock1/Q1	"	150	"		
		92 CKT B	IN	IN(H)	5.0 V	"				B	OUT		"		B	Clock1/Q1	"	110	"		
		93 CKT A				"	5.0 V	IN(H)	IN	B	OUT		"			Clock2/Q2	"	150	"		
		93 CKT B				"	5.0 V	IN(H)	IN	B	OUT	"	"	OUT		Clock2/Q2	"	110	"		
10 T _C =+125°C	f _{MAX} 5/	(Fig. 11)	94	IN	IN(H)	5.0 V	"						"		OUT	B	Clock1/Q1	2.5		"	
			95	IN	IN(G)	5.0 V	"						"		OUT	B	Clock1/Q1	"		"	
			96				"	5.0 V	IN(H)	IN	B	OUT		"			Clock2/Q2	"	MHz	"	
			97				"	5.0 V	IN(G)	IN	B	OUT	OUT	"			Clock2/Q2	"		"	
	t _{PLH}	3003 (Fig. 10)	98 CKT A			IN	"						"	OUT		J	Clear1/Q1	10	125	ns	
			98 CKT B			IN	"						"	OUT		J	Clear1/Q1	"	85	"	
			99 CKT A			J	"						"		OUT	IN	Preset 1/Q1	"	125	"	
			99 CKT B			J	"						"		OUT	IN	Preset 1/Q1	"	85	"	
101 CKT A				"	IN		J		J		OUT	"				Clear2/Q2	"	125	"		
	100 CKT B				"	IN		J		J		OUT	"			Clear2/Q2	"	85	"		
	101 CKT A				"	J		IN	OUT	OUT		"				Preset 2/Q2	"	125	"		
	101 CKT B				"	J		IN	OUT	OUT		"				Preset 2/Q2	"	85	"		

See footnotes at end of device type 05.

TABLE III. Group A inspection for device type 05 – Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases A,B,D	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Measured terminal	Test limits		Unit
			Case C	3	2	1	14	13	12	11	10	9	8	7	6	5	4		Min	Max	
			Test no.	Clock 1	D1	Clear 1	V _{CC}	Clear 2	D2	Clock 2	Preset 2	Q2	$\overline{Q}$ 2	GND	$\overline{Q}$ 1	Q1	Preset 1				
10 T _C =+125°C	t _{PHL}	3003 (Fig. 10)	102 CKT A			IN	5.0 V							GND		OUT	J	Clear1/Q1	10	200	ns
			102 CKT B			IN	"							"	OUT	J	Clear1/Q1	"	120	"	
			103 CKT A			J	"							"	OUT	IN	Preset 1/Q1	"	200	"	
			103 CKT B			J	"							"	OUT	IN	Preset 1/Q1	"	120	"	
			104 CKT A				"	IN		J	OUT		"				Clear2/Q2	"	200	"	
			104 CKT B				"	IN		J	OUT		"				Clear2/Q2	"	120	"	
			105 CKT A				"	J		IN		OUT	"				Preset 2/Q2	"	200	"	
			105 CKT B				"	J		IN		OUT	"				Preset 2/Q2	"	120	"	
	t _{PLH}	3003 (Fig. 11)	106 CKT A	IN	IN(G)	B	"							"		OUT	5.0 V	Clock1/Q1	"	150	"
			106 CKT B	IN	IN(G)	B	"	B	IN(G)	IN	5.0 V	OUT		"			5.0 V	Clock1/Q1	"	85	"
			107 CKT A				"	B	IN(G)	IN	5.0 V	OUT		"	OUT			Clock2/Q2	"	150	"
			107 CKT B				"	B	IN(G)	IN	5.0 V	OUT	"	"				Clock2/Q2	"	85	"
	t _{PHL}	3003 (Fig. 12)	108 CKT A	IN	IN(H)	B	"							"	OUT		5.0 V	Clock1/Q1	"	200	"
			108 CKT B	IN	IN(H)	B	"							"	OUT		5.0 V	Clock1/Q1	"	120	"
			109 CKT A				"	B	IN(H)	IN	5.0 V		OUT	"				Clock2/Q2	"	200	"
			109 CKT B				"	B	IN(H)	IN	5.0 V		OUT	"				Clock2/Q2	"	120	"
	t _{PLH}	3003 (Fig. 12)	110 CKT A	IN	IN(G)	5.0 V	"							"	OUT		B	Clock1/Q1	"	150	"
			110 CKT B	IN	IN(G)	5.0 V	"							"	OUT		B	Clock1/Q1	"	85	"
			111 CKT A				"	5.0 V	IN(G)	IN	B		OUT	"		B		Clock2/Q2	"	150	"
			111 CKT B				"	5.0 V	IN(G)	IN	B		OUT	"		B		Clock2/Q2	"	85	"
	t _{PHL}	3003 (Fig. 12)	112 CKT A	IN	IN(H)	5.0 V	"							"		OUT	B	Clock1/Q1	"	200	"
			112 CKT B	IN	IN(H)	5.0 V	"							"		OUT	B	Clock1/Q1	"	120	"
			113 CKT A				"	5.0 V	IN(H)	IN	B	OUT		"				Clock2/Q2	"	200	"
			113 CKT B				"	5.0 V	IN(H)	IN	B	OUT	"	"	OUT			Clock2/Q2	"	120	"
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C =+55°C																				

NOTE: A = normal clock pulse, B = momentary GND, then 4.5 V,
J = input pulse, t_p ≥ 100 ns, PRR = 0 MHz, V_{OL} = 0 V, V_{OH} = 4.5 V.

1/ Terminal conditions (pins not designated may be H ≥ 2.0 V, or L ≤ 0.8 V, or open).

2/ Tests shall be performed in sequence.

3/ Input voltages shown are: A = 2.4 V minimum and B = 0.4 V maximum.

4/ Output voltages shall be either: (a) H = 2.4 V, minimum and L = 0.4 V, maximum when using a high speed checker double comparator; or
(b) H ≥ 1.5 V and L ≤ 1.5 V when using a high speed checker single comparator.

5/ f_{MAX}, minimum limit specified is the frequency of the input pulse. The output frequency shall be one-half of the input frequency.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but it is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirement for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to acquiring activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND	Electrical ground (common terminal)
V _{IN}	Voltage level at an input terminal
I _{IN}	Current flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer lead lengths and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Device type</u>	<u>Commercial type</u>
01	54L71
02	54L72
03	54L73
04	54L78
05	54L74

6.8 Manufacturers' designation. Manufacturers' circuits included in this specification are designated as shown in table IV herein.

TABLE IV. Manufacturers designator.

Device Types	Texas Instruments	National Semiconductor
	A	B
01		X
02		X
03		X
04		X
05		X

6.9 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship; to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5962-2006-004)

Review activities:
 Army - MI, SM
 Navy - AS, CG, MC, SH, TD
 Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.