
PART NUMBER**54LS224AJB-ROCS**

Rochester Electronics**Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54LS222, SN54LS224, SN54LS227, SN54LS228 SN74LS222, SN74LS224, SN74LS227, SN74LS228 16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

JANUARY 1981 REVISED MARCH 1985

- Independent Synchronous Inputs and Outputs
- 16 Words of 4 Bits Each
- 3-State Outputs Drive Bus Lines Directly
- Data Rates from 0 to 10 MHz
- Fall-Through Time . . . 50 ns Typ
- Data Terminals Arranged for Optimum PC Board Layout
- Expandable Using External Gating

description

These 64-bit memories are Low-Power Schottky memory arrays organized as 16 words of 4 bits each. They can be expanded in multiples of $15m + 1$ words or $4n$ bits, or both, (where n is the number of packages in the vertical array and m is the number of packages in the horizontal array) however some external gating is required (see Figure 1). For longer words using the 'LS224 or 'LS228 the IR signals of the first-rank packages and OR signals of the last-rank packages must be ANDed for proper synchronization.

TYPE	INPUT-READY ENABLE AND OUTPUT READY ENABLE	OUTPUT
'LS222	Yes	3-State
'LS224	No	3-State
'LS227	Yes	Open-collector
'LS228	No	Open-collector

operation

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. These FIFOs are designed to process data at rates from 0 to 10 MHz in a bit-parallel format, word by word. Data is written into the memory on a high-to-low transition at the load clock input (LDCK) and read out on a low-to-high transition at the unload clock input (UNCK).

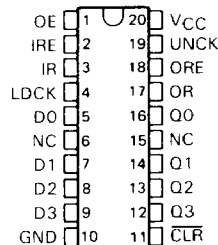
The memory is full when the number of words clocked in exceeds the number of words clocked out by 16. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

Status of the FIFO memory (see timing diagram) is monitored by the input ready (IR) and output ready (OR) flags that indicate "not full" and "not empty" conditions. The IR output will be high only when the memory is not full and the LDCK input is low. The OR output will be high only when the memory is not empty and UNCK is high.

A low level at the clear ($\overline{\text{CLR}}$) input resets the internal stack control counters and also sets IR high and OR low to indicate that old data remaining at the data outputs is invalid. Data outputs are noninverting with respect to the data inputs and are at high impedance when output enable (OE) is low. OE does not affect the IR and OR outputs.

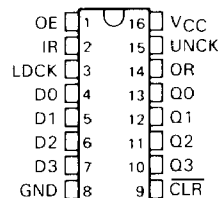
SN54LS222, SN54LS227 . . . J PACKAGE
SN74LS222, SN74LS227 . . . J OR N PACKAGE

(TOP VIEW)



SN54LS224, SN54LS228 . . . J PACKAGE
SN74LS224, SN74LS228 . . . J OR N PACKAGE

(TOP VIEW)

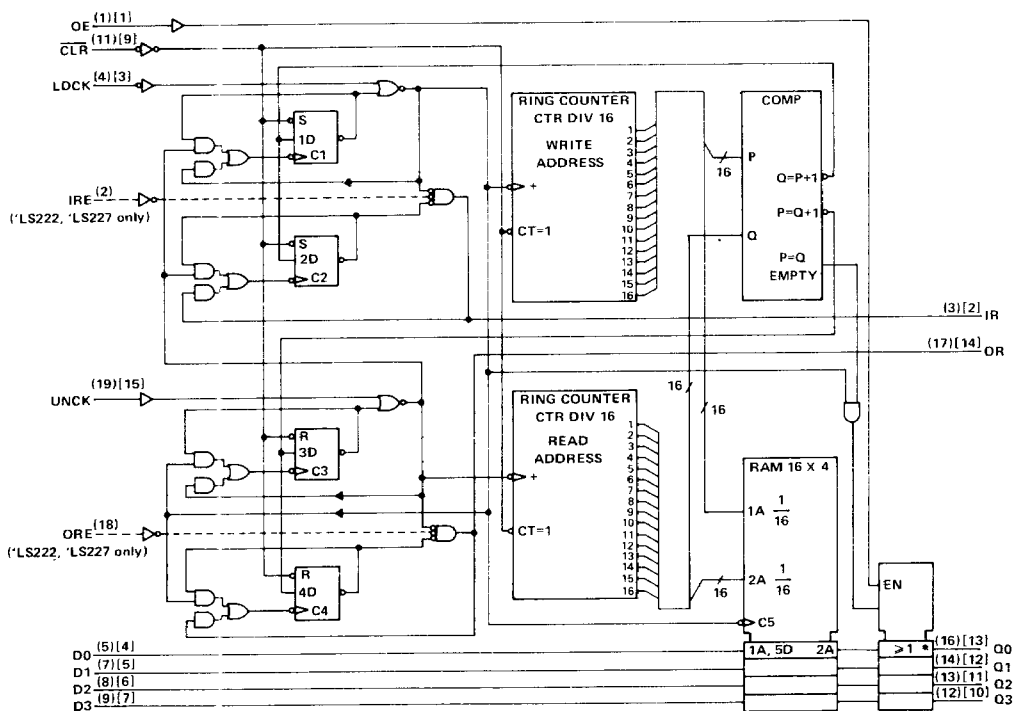


NC No internal connection

For chip carrier information
contact the factory.

**SN54LS222, SN54LS224, SN54LS227, SN54LS228
SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES**

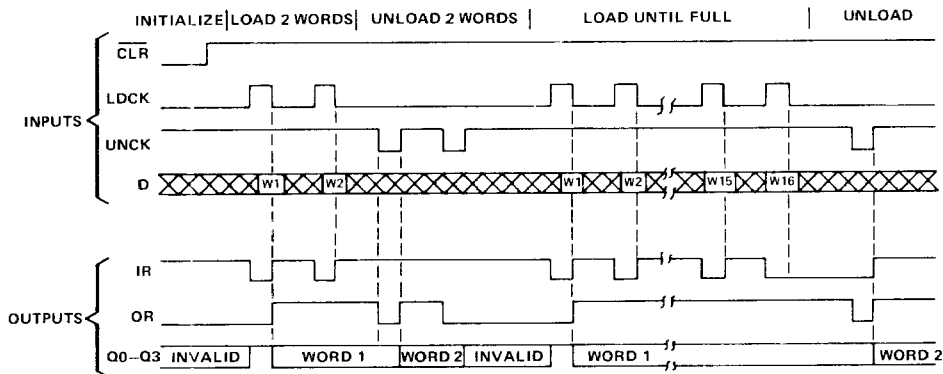
functional block diagram (positive logic)



*LS222 and LS224 have 3 state (◻) outputs.
LS227 and LS228 have open-collector (◻) outputs.

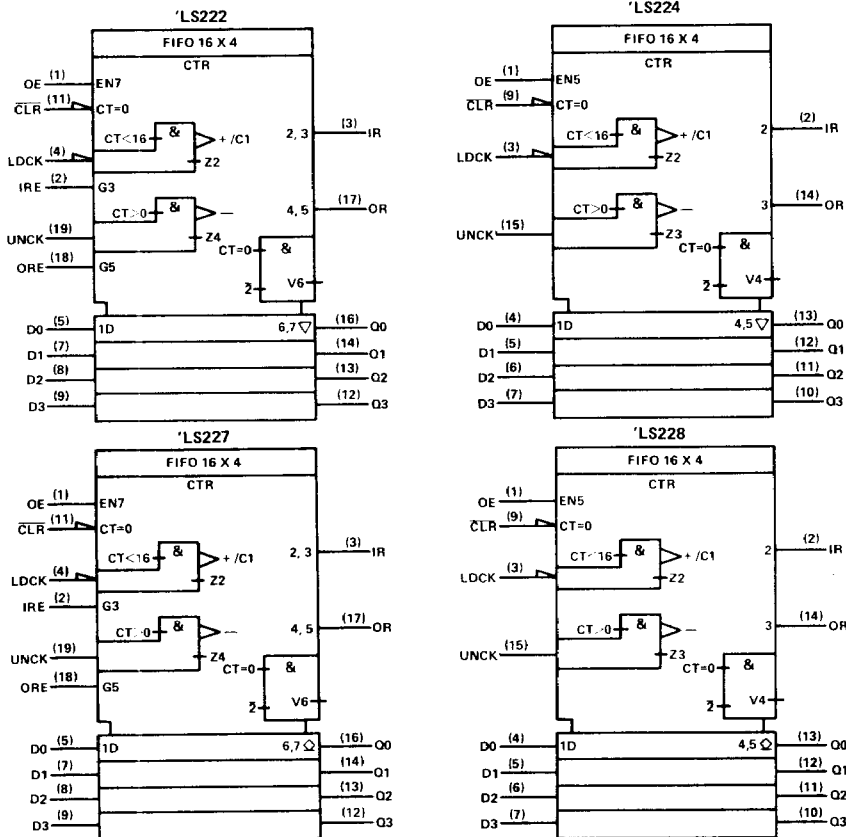
[LS222 and LS227 pin numbers]
[LS224 and LS228 pin numbers]

timing diagram



SN54LS222, SN54LS224, SN54LS227, SN54LS228 SN74LS222, SN74LS224, SN74LS227, SN74LS228 16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES

logic symbols†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

These symbols are functionally accurate but do not show the details of implementation; for these, see the functional block diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at that time. Output data is invalid when the counter content is 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (See Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range:	
SN54LS222, SN54LS224, SN54LS227, SN54LS228	-55°C to 125°C
SN74LS222, SN74LS224, SN74LS227, SN74LS228	0°C to 70°C
Storage range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS222, SN54LS224, SN74LS222, SN74LS224 **16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES** **WITH 3-STATE OUTPUTS**

recommended operating conditions

		SN54LS [†]			SN74LS [†]			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current	Q		–1			2.6	mA
		IR, OR		–0.4			–0.4	
I _{OL}	Low-level output current	Q		12			24	mA
		IR, OR		4			8	
t _w	Pulse duration	LDCK high		60			60	ns
		LDCK low		15			15	
		UNCK low		30			30	
		UNCK high		30			30	
		CLR low		20			20	
t _{su}	Setup time	D to LDCK↓		50			50	ns
		LDCK↓ before UNCK↓		50			50	
		UNCK↑ before LDCK↑		50			50	
t _h	Hold time	D from LDCK↓		0			0	ns
T _A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS†		SN74LS†		UNIT
				MIN	TYP‡	MAX	MIN	
VIK		VCC = MIN, II = -18 mA		-1.5		-1.5		V
VOH	Q	VCC = MIN, IOH = MAX		2.4	3.3	2.4	3.4	V
	IR, OR	VCC = MIN, IOH = -0.4 mA		2.5	3.4	2.7	3.4	
VOL	Q	VCC = MIN, IOL = 12 mA		0.25	0.4	0.25	0.4	V
		VCC = MIN, IOL = 24 mA				0.35	0.5	
	IR, OR	VCC = MIN, IOL = 4 mA		0.25	0.4	0.25	0.4	
		VCC = MIN, IOL = 8 mA				0.35	0.5	
IOZH	Q	VCC = MAX, VO = 2.7 V		20		20		μA
IOZL	Q	VCC = MAX, VO = 0.4 V		-20		-20		μA
II		VCC = MAX, VI = 7 V		0.1		0.1		mA
IIH		VCC = MAX, VI = 2.7 V		20		20		μA
IIL		VCC = MAX, VI = 0.4 V		-0.4		-0.4		mA
IOS§	Q	VCC = MAX,		-30	-130	-30	-130	mA
	IR, OR			-20	-100	-20	-100	
ICC	VCC = MAX,		Outputs high	84	135	84	135	mA
			Outputs low	87	155	87	155	
			Outputs disabled	89	155	89	155	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

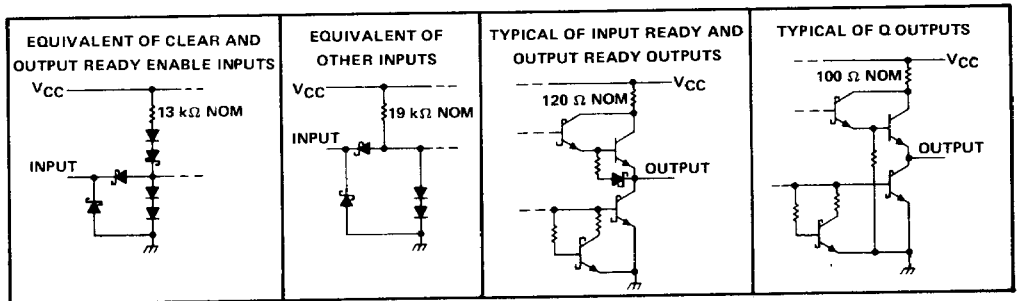
SN54LS222, SN54LS224, SN74LS222, SN74LS224 **16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES** **WITH 3-STATE OUTPUTS**

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM	TO	TEST CONDITIONS	LS222			LS224			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	$\overline{IRE}\uparrow$	$\overline{IR}$	$R_L = 2\text{ k}\Omega$, $C_L = 15\text{ pF}$, See Note 2		23	35				ns
t_{PHL}	$\overline{IRE}\downarrow$	$\overline{IR}$			9	15				ns
t_{PLH}	$\overline{ORE}\uparrow$	$\overline{OR}$			22	35				ns
t_{PHL}	$\overline{ORE}\downarrow$	$\overline{OR}$			9	15				ns
t_{PLH}	$\overline{LDCK}\downarrow$	$\overline{IR}$			25	40	25	40		ns
t_{PHL}	$\overline{LDCK}\uparrow$	$\overline{IR}$			36	50	36	50		ns
t_{PLH}	$\overline{LDC}\downarrow$	$\overline{OR}$			48	70	48	70		ns
t_{PLH}	$\overline{UNCK}\uparrow$	$\overline{OR}$			29	45	29	45		ns
t_{PHL}	$\overline{UNCK}\downarrow$	$\overline{OR}$			28	45	28	45		ns
t_{PLH}	$\overline{UNCK}\uparrow$	$\overline{IR}$			49	70	49	70		ns
t_{PLH}	$\overline{CLR}\downarrow$	$\overline{IR}$			36	55	36	55		ns
t_{PHL}	$\overline{CLR}\downarrow$	$\overline{OR}$			25	40	25	40		ns
t_{PHL}	$\overline{LDCK}\downarrow$	Q	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, See Note 2		34	50	34	50		ns
t_{PLH}	$\overline{UNCK}\uparrow$	Q			54	80	54	80		ns
t_{PHL}	$\overline{UNCK}\downarrow$	Q			45	70	45	70		ns
t_{PZL}	$\overline{OE}\uparrow$	Q			22	35	22	35		ns
t_{PZH}	$\overline{OE}\downarrow$	Q	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$, See Note 2		21	35	21	35		ns
t_{PLZ}	$\overline{OE}\downarrow$	Q			16	30	16	30		ns
t_{PHZ}	$\overline{OE}\downarrow$	Q			18	30	18	30		ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



SN54LS227, SN54LS228, SN74LS227, SN74LS228 **16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES** **WITH OPEN-COLLECTOR OUTPUTS**

recommended operating conditions

		SN54LS [†]			SN74LS [†]			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
V _{OH}	High-level output voltage			5.5			5.5	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			12			24	
				4			8	
t _w	Pulse duration			LDCK high	60		60	ns
				LDCK low	15		15	
				UNCK low	30		30	
				UNCK high	30		30	
				CLR low	20		20	
t _{su}	Setup time			D to LDCK↓	50		50	ns
				LDCK↓, before UNCK↓	50		50	
				UNCK↑ before LDCK↑	50		50	
t _h	Hold time			D from LDCK↓	0		0	ns
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'		SN74LS'		UNIT
				MIN	TYP‡	MAX	MIN	
VIK		VCC = MIN, II = - 18 mA		- 1.5		- 1.5		V
IOH		Q	VCC = MIN, VOH = 5.5 V	0.1		0.1		mA
VOH		IR, OR	VCC = MIN, IOH = - 0.4 mA	2.5	3.4	2.7	3.4	V
VOL	Q	VCC = MIN, IOL = 12 mA		0.25		0.4		V
		VCC = MIN, IOL = 24 mA				0.35		
	IR, OR	VCC = MIN, IOL = 4 mA		0.25		0.4		
		VCC = MIN, IOL = 8 mA				0.35		
IOZH		Q	VCC = MAX, VO = 2.7 V	20		20		μA
IOZL		Q	VCC = MAX, VO = 0.4 V	- 20		- 20		μA
II			VCC = MAX, VI = 7 V	0.1		0.1		mA
IIH			VCC = MAX, VI = 2.7 V	20		20		μA
IIL			VCC = MAX, VI = 0.4 V	- 0.4		- 0.4		mA
IOS§		IR, OR	VCC = MAX	- 20	- 100	- 20	- 100	mA
ICC			VCC = MAX	Outputs high		84	135	mA
				Outputs low		87	155	
				Outputs disabled		89	155	

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§]Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

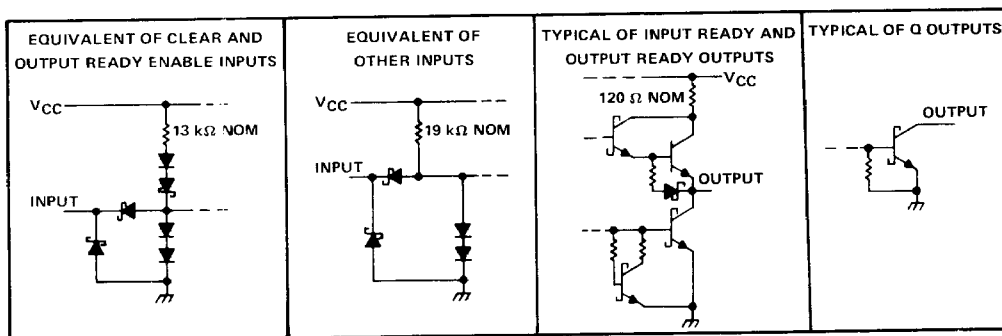
SN54LS227, SN54LS228, SN74LS227, SN74LS228 16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM	TO	TEST CONDITIONS	'LS227			'LS228			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	IRE*	IR	$R_L = 2\text{ k}\Omega$ $C_L = 15\text{ pF}$ See Note 2		23	35				ns
t_{PHL}	IRE*	IR			9	15				ns
t_{PLH}	ORE*	OR			22	35				ns
t_{PHL}	ORE*	OR			9	15				ns
t_{PLH}	LDCK*	IR			25	40		25	40	ns
t_{PHL}	LDCK*	IR			36	50		36	50	ns
t_{PLH}	LDCK*	OR			48	70		48	70	ns
t_{PLH}	UNCK*	OR			29	45		29	45	ns
t_{PHL}	UNCK*	OR			28	45		28	45	ns
t_{PLH}	UNCK*	IR			49	70		49	70	ns
t_{PLH}	CLR*	IR			36	55		36	55	ns
t_{PHL}	CLR*	OR			25	40		25	40	ns
t_{PHL}	LDCK*	Q	$R_L = 667\ \Omega$ $C_L = 45\text{ pF}$ See Note 2		34	50		34	50	ns
t_{PLH}	UNCK*	Q			54	80		54	80	ns
t_{PHL}	UNCK*	Q			45	70		45	70	ns
t_{PLH}	OE*	Q			21	30		21	30	ns
t_{PHL}	OE*	Q			20	35		20	35	ns

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



**SN54LS222, SN54LS224, SN54LS227, SN54LS228
SN74LS222, SN74LS224, SN74LS227, SN74LS228
16 X 4 SYNCHRONOUS FIRST-IN FIRST-OUT MEMORIES**

TYPICAL APPLICATIONS INFORMATION

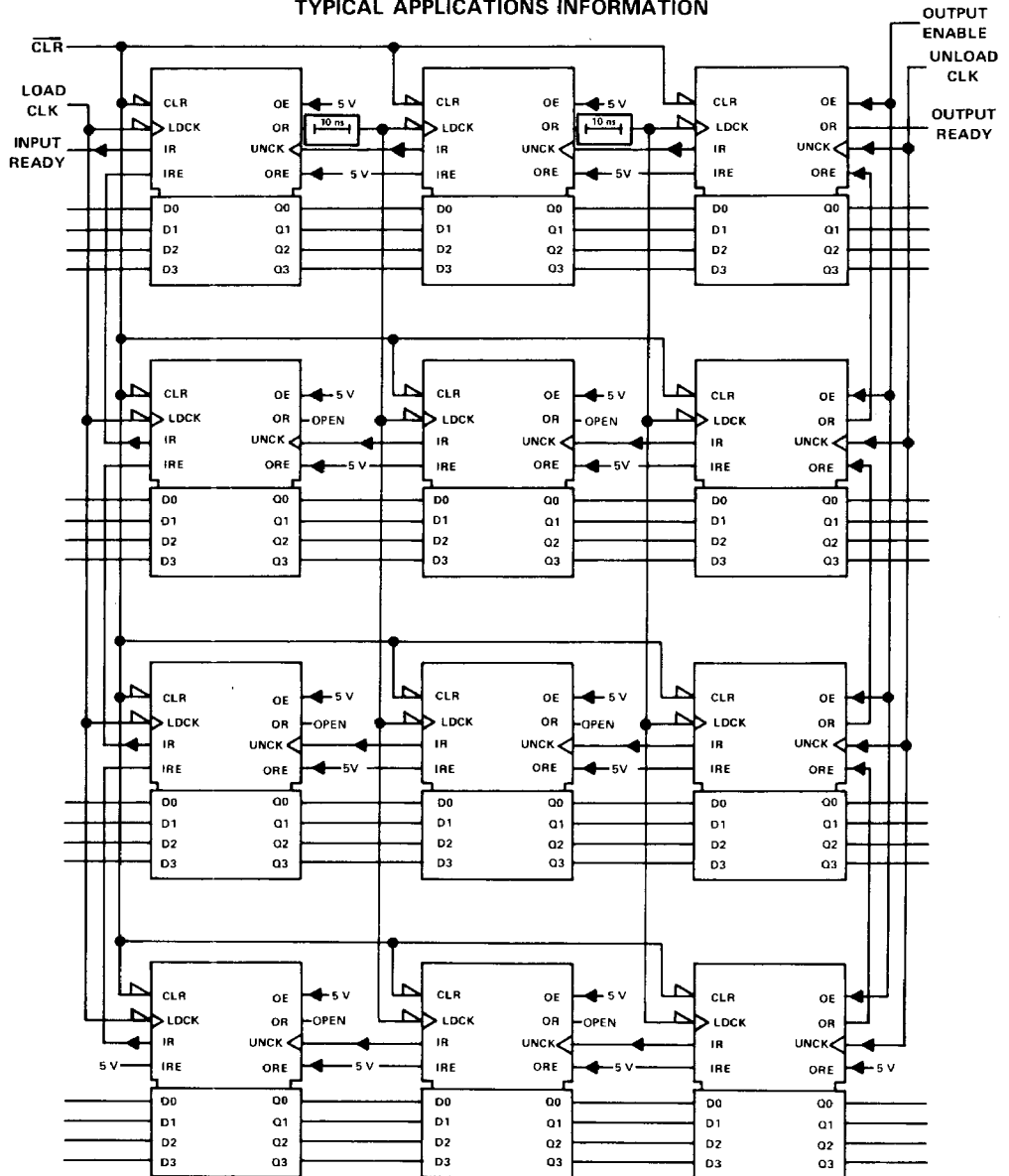


FIGURE 1. 46-WORD BY 16-BIT EXPANSION USING 'LS222

10 ns = Noninverting delay ≥ 10 ns (e.g., 2 stages of 'LS04), 2 places.