

# PART NUMBER 54LS348BEA-ROCV

# Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

# **Quality Overview**

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
  - Class Q Military
  - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

 Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SDLS161 - OCTOBER 1976 - REVISED MARCH 1988

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:

   N-Bit Encoding
   Code Converters and Generators
- Typical Data Delay . . . 15 ns
- Typical Power Dissipation . . . 60 mW

#### description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion. Outputs A0, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

#### **FUNCTION TABLE**

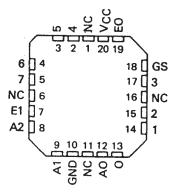
	INPUTS									Ol	JTPU	TS	
EI	0	1	2	3	4	5	6	7	A2 A1 A0 GS E				
Н	Х	Х	Χ	Х	Χ	X	X	Χ	Z	Z	Z	Н	Н
L	Н	Н	Н	Н	Н	Н	Н	Н	z	Z	Z	н	L
L	Х	Х	Х	Х	Х	Χ	Х	L	L	L	L	L	н
L	Х	Х	X	Х	Х	Х	L	Н	L	L	Н	L	н
L	Х	Х	Χ	X	Х	L	Н	Н	L	Н	L	L	н
L	Х	X	Χ	Х	L	Н	Н	Н	L	Н	Н	L	н
L	Ý	Х	Х	L	Н	Н	Н	Н	н	L	L	L	н
L	Х	Х	L	Н	Н	Н	Н	Н	н	L	н	L	н
L	Х	L	Н	H	Н	Н	Н	Н	н	Н	L	L	н
L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	н

H = high logic level, L = low logic level, X = irrelevant

SN54LS348 . . . J OR W PACKAGE SN74LS348 . . . D OR N PACKAGE (TOP VIEW)

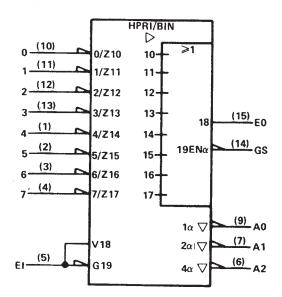
4 🗆	1	U <sub>16</sub> V <sub>CC</sub>
5 🗌	2	15 EO
6 🗌	3	14 🛮 GS
7 🛚	4	13 3
E1 🛚	5	12 2
A2 [	6	11 🛮 1
A1 🗌	7	10 🛮 0
GND [	8	OA 🗌 e

SN54LS348 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

### logic symbol<sup>†</sup>



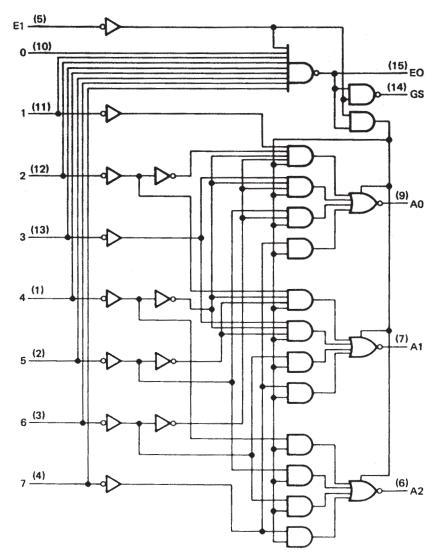
<sup>&</sup>lt;sup>†</sup>This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D, J, N, and W packages.



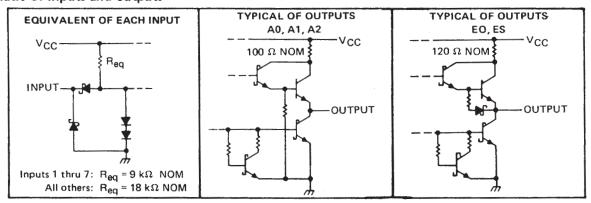
Z = high-impedance state

#### logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

#### schematic of inputs and outputs





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# absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1)	
Operating free-air temperature range	SN54LS348
	SN74LS348
Storage temperature range	

NOTE 1: Voltage values are with respect to network ground terminal.

#### recommended operating conditions

	·	SN54LS348			Si			
		MIN	NOM	MAX	MIN	MAX	UNIT	
Supply voltage, V <sub>CC</sub>		4.5	5	5.5	4.75	5	5,25	V
High-level output current, IOH	A0, A1, A2			-1			-2.6	mA
migriever output current, 10H	EO, GS	-400			-400			μА
Low-level output current, IOI	A0, A1, A2 E0, GS			12			24	mA
- Converse of the Content to C				4			8	mA
Operating free-air temperature, TA		-55		125	0		70	°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CON	SN	154LS3	48	SN74LS348			UNIT		
			TEST CON	MIN	TYP‡	MAX	MIN	TYP‡	MAX	ON		
V <sub>IH</sub> High-level input voltage					2			2			V	
VIL	Low-level input voltage					**	0.7			0.8	V	
VIK	Input clamp voltage		V <sub>CC</sub> = MIN,	I <sub>1</sub> = -18 mA			-1.5			-1.5	V	
Vлн	High-level	A0, A1, A2	V <sub>CC</sub> = MIN,	I <sub>OH</sub> = -1 mA	2.4	3.1						
	output voltage		V <sub>IH</sub> = 2 V,	I <sub>OH</sub> = -2.6 mA				2.4	3,1		V	
		EO, GS	V <sub>IL</sub> = V <sub>IL</sub> max	I <sub>OH</sub> = -400 μA	2.5	3.4		2.7	3.4			
		A0, A1, A2	V <sub>CC</sub> = MIN,	I <sub>OL</sub> = 12 mA		0.25	0.4		0.25	0.4	V	
VOL	Low-level		V <sub>IH</sub> = 2 V,	OL = 24 mA					0.35	0.5		
·OL	Output voltage	EO, GS	VIL = VILmax	1 <sub>OL</sub> = 4 mA		0.25	0.4		0.25	0.4		
		20, 30	VIL - VILINAX	I <sub>OL</sub> = 8 mA					0,35	0.5		
loz	Off-State (high-impedance	A0, A1, A2	V <sub>CC</sub> = MAX,	V <sub>O</sub> = 2.7 V		-	20			20		
102	state) output current	A0, A1, A2	V <sub>IH</sub> = 2 V	V <sub>O</sub> = 0.4 V		-2				-20	μ/	
11	Input current at maximum	Inputs 1 thru 7	V 1440 V	V - 7.V			0.2			0.2		
'1	input voltage	All other inputs	V <sub>CC</sub> = MAX,	V  = / V			0.1			0.1	m	
ΙН	High-level input current	Inputs 1 thru 7	V 140V	V 07V			40			40		
'IH	riigii-ievei triput current	All other inputs	V <sub>CC</sub> = MAX,	V = 2.7 V			20			20	μA	
111	Low-level input current	Inputs 1 thru 7	V 144.V				-0.8			-0.8		
11L	Low-level input current	All other inputs	V <sub>CC</sub> = MAX,	V   = 0.4 V			-0.4		· · · · · · · · · · · · · · · · · · ·	-0.4	m.	
los	Short-circuit output current §	Outputs A0, A1, A2	V MAY		-30		-130	-30	***************************************	-130		
-03		Outputs EO, GS	V <sub>CC</sub> = MAX		-20		-100	-20		-100	m	
Icc	Supply current		V <sub>CC</sub> = MAX,	Condition 1		13	25		13	25		
ICC Supply current			See Note 2	Condition 2		12	23		12	23	m	

For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: ICC (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open. ICC (condition 2) is measured with all inputs and outputs open.



<sup>‡</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^{\circ} \text{ C}$ .

<sup>§</sup>Not more than one output should be shorted at a time.

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## switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ} \text{ C}$

PARAMETER <sup>†</sup>	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ФLН	1 thru 7	A0, A1, or A2	In-phase		111	11	17	ns
tPHL.	1 11114 /	A0, A1, 01 A2	output	C. = 45 = 5		20	30	113
ФLН	1 thru 7	A0, A1, or A2	Out-of-phase	CL = 45 pF,		23	35	ns
<b>tPHL</b>	i thru /	AU, A1, 01 A2	output	RL = 667 Ω, See Note 3		23	35	113
<b>tPZH</b>	EI	A0, A1, or A2		See Note 3		25	39	ns
ΨZL	] '	70, 71, 01 72				24	41	] ""
<b>tPLH</b>	0 thru 7	EO	Out-of-phase	CL = 15 pF RL = 2 kΩ,		11	18	ns
<b>tPHL</b>	0 thru 7	20	output			26	40	
<b>tPLH</b>		GS	In-phase			38	55	ns
tPHL			output			9	21	
<b>tPLH</b>	EI	EI GS In-phase		See Note 3		11	17	
<b>tPHL</b>	1 -	43	output	See Note S		14	36	ns
ФLН	EI	EO	In-phase			17	26	
tPHL	1 "		output	:		25	40	ns
tPHZ	EI	A0, A1, or A2		CL = 5 pF		18	27	
ヤLZ	] -'	70, 71, 01 72		R <sub>L</sub> = 667 Ω		23	35	ns

<sup>†</sup> tpLH = propagation delay time, low-to-high-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

### TYPICAL APPLICATION DATA

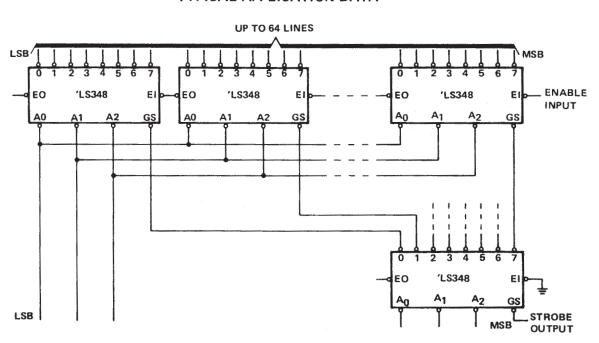


FIGURE 1-PRIORITY ENCODER WITH UP TO 64 INPUTS.



tpHL = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

tpLZ = output disable time from low level

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APPLICATION NOTES | RELATED DOCUMENTS

PRODUCT SUPPORT: TRAINING

#### SN74LS348, 8-Line To 3-Line Priority Encoder

DEVICE STATUS: ACTIVE

PARAMETER NAME	SN74LS348
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
Output	3S
From	8
То	3

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- · 3-State Outputs Drive Bus Lines Directly
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DESCRIPTION ▲Back to Top

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The 'LS348 circuits encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion. Outputs AO, A1, and A2 are implemented in three-state logic for easy expansion up to 64 lines without the need for external circuitry. See Typical Application Data.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74ls348.pdf (192 KB) (Updated: 03/01/1988)

**APPLICATION NOTES** 

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View Application Notes for Digital Logic

- Designing With Logic (Rev. C) (SDYA009C Updated: 06/01/1997)
- Designing with the SN54/74LS123 (Rev. A) (SDLA006A Updated: 03/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 Updated: 06/20/2001)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 Updated: 10/01/1996)
- Live Insertion (SDYA012 Updated: 10/01/1996)

RELATED DOCUMENTS	

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB Updated: 04/22/2002)

#### PRICING/AVAILABILITY/PKG ▲Back to Top TI INVENTORY STATUS REPORTED DISTRIBUTOR INVENTORY DEVICE INFORMATION AS OF 3:00 PM GMT, 26 Sep 2002 AS OF 3:00 PM GMT, 26 Sep 2002 BUDGETARY **STD** ORDERABLE **PRODUCT** DISTRIBUTOR **PACKAGE** IN PROGRESS **STATUS** TEMP (°C) PRICING **PACK** IN STOCK LEAD TIME IN STOCK PURCHASE DEVICE TYPE PINS CONTENT QTY|DATE COMPANY | REGION QTY | \$US QTY ACTIVE View Contents SN74LS348D 16 0 TO 70 1KU | 1.64 40 <u>N/A\*</u> 1114 | 03 Oct 4 WKS <u>(D)</u> >10k | 10 Oct SN74LS348DR ACTIVE 16 0 TO 70 View Contents 1KU | 1.67 2500 <u>N/A\*</u> 1114 | 03 Oct 4 WKS (D) >10k | 10 Oct SN74LS348N ACTIVE 16 0 TO 70 View Contents 1KU | 1.64 25 <u>N/A\*</u> 1325 | 4 WKS 9839 | 02 Oct 375 | 03 Oct >10k | 07 Oct >10k | 14 Oct <u>PDIP</u> SN74LS348N3 OBSOLETE 16 0 TO 70 View Contents 1KU | <u>N/A\*</u> Not Available (N) <u>SOP</u> SN74LS348NSR ACTIVE View Contents 1KU | 1.64 2000 N/A\* >10k | 07 Oct 4 WKS 16 (NS) >10k | 14 Oct

Table Data Updated on: 9/26/2002



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