
PART NUMBER**54LS681JB-ROCV**

**Rochester Electronics
Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54LS646, 54LS681

Octal Bus Transceivers and Registers

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CSA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

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FOR REFERENCE ONLY

**SN54LS646 THRU SN54LS649
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS**
D2661, DECEMBER 1982 — REVISED MARCH 1988

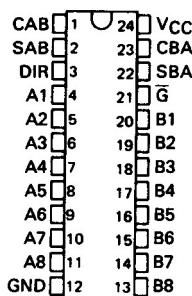
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Included Among the Package Options Are Compact 24-pin 300-mil-Wide Plastic and Ceramic DIPs, Ceramic Chip Carriers, and Plastic "Small Outline" Packages
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'LS646	3-State	True
'LS647	Open-Collector	True
'LS648	3-State	Inverting
'LS649	Open-Collector	Inverting

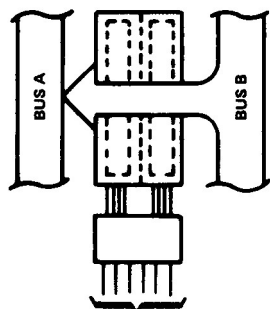
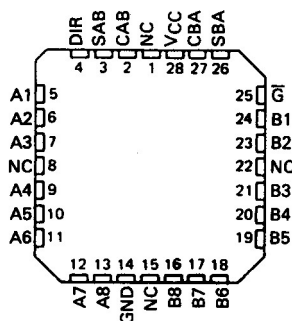
description

These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

**SN54LS'...JT PACKAGE
SN74LS'...DW OR NT PACKAGE
(TOP VIEW)**

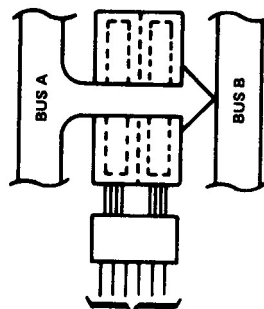


**SN54LS'...FK PACKAGE
(TOP VIEW)**



(21) (3) (1) (23) (2) (22)
G DIR CAB CBA SAB SBA
L L X H or L X L

**REAL-TIME TRANSFER
BUS B TO BUS A**



(21) (3) (1) (23) (2) (22)
G DIR CAB CBA SAB SBA
L H H or L X L X

**REAL-TIME TRANSFER
BUS A TO BUS B**

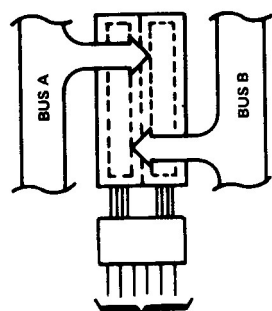
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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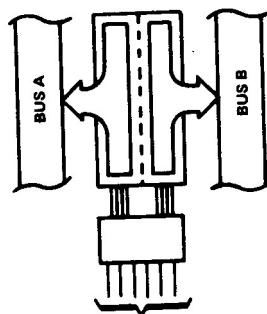
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SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649 OCTAL BUS TRANSCEIVERS AND REGISTERS



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21)	(3)	(1)	(23)	(2)	(22)
\bar{G}	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER
STORED DATA
TO A OR B

Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0° to 70°C .

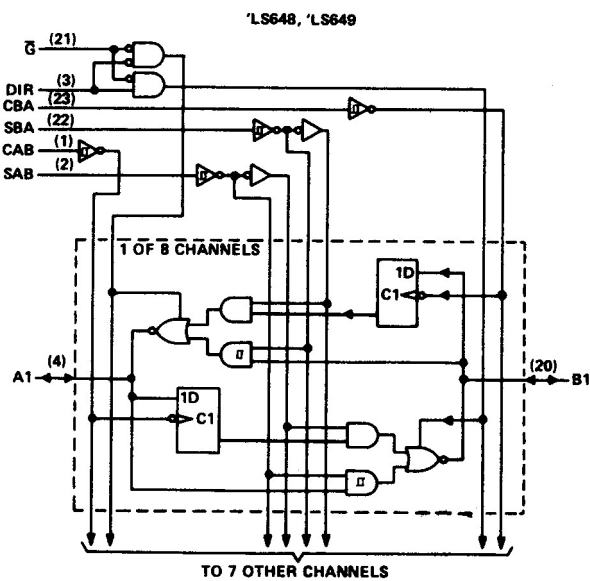
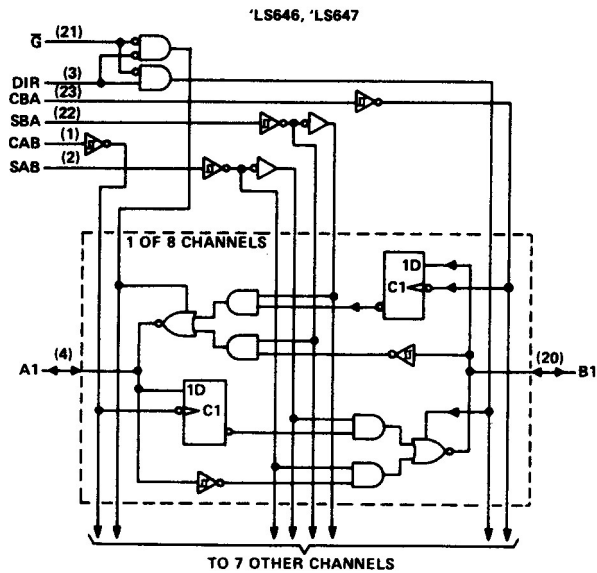
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
\bar{G}	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	LS646, LS647	LS648, LS649
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time \bar{B} Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored \bar{B} Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time \bar{A} Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored \bar{A} Data to B Bus

† The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

SN54LS646 THRU SN54LS649, SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

logic diagrams (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

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TTL Devices

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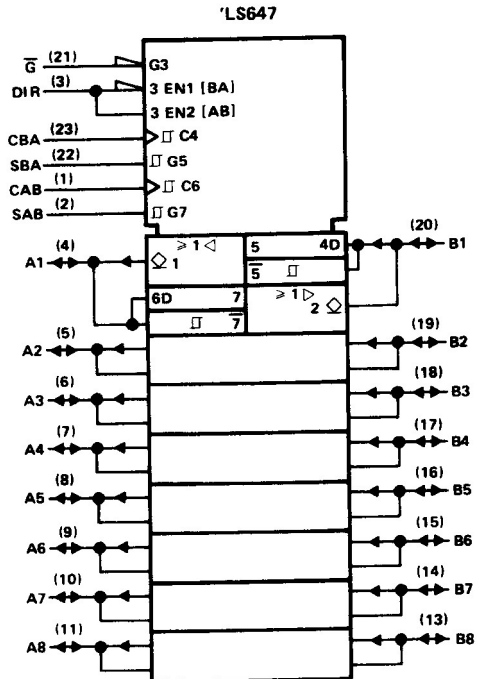
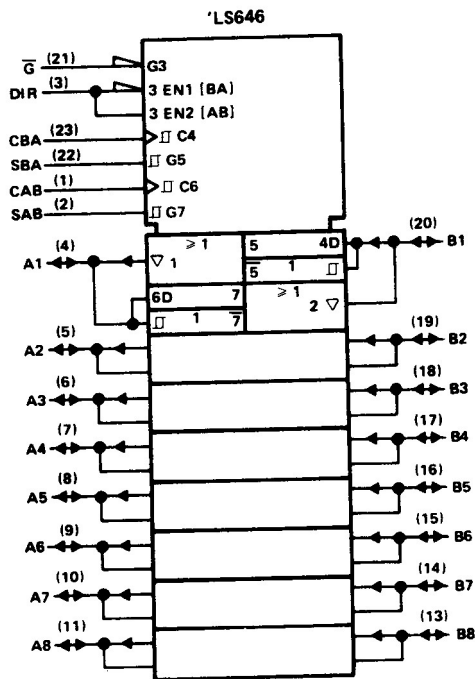
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SN54LS646, SN54LS647, SN74LS646, SN74LS647 **OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†

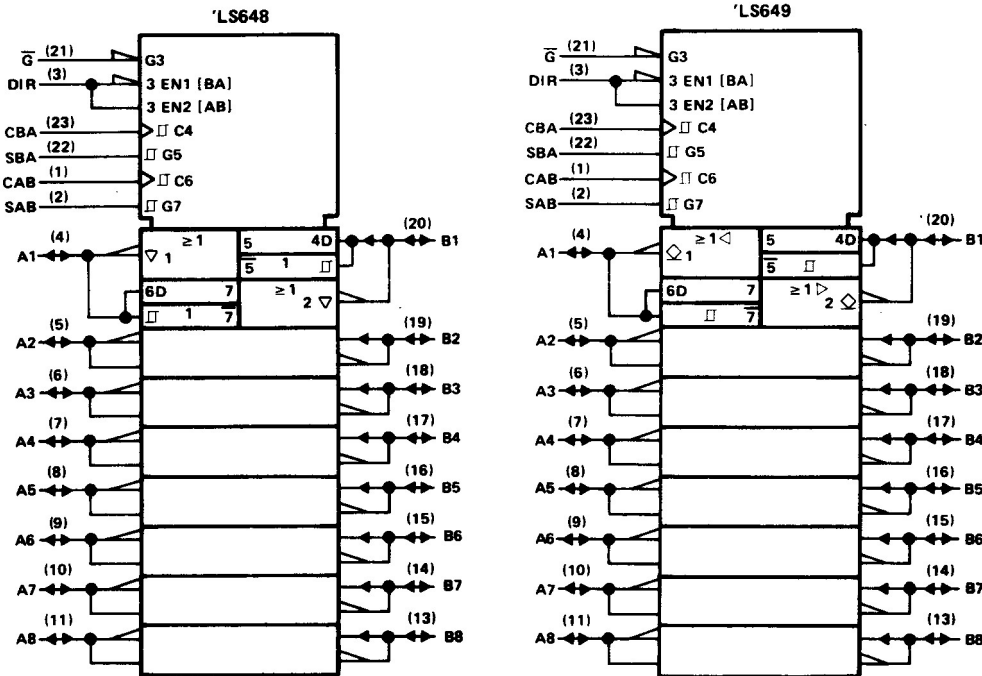
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TTL Devices



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for DW, JT, and NT packages.

SN54LS648, SN54LS649, SN74LS648, SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS

logic symbols[†] (continued)



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for DW, JT, and NT packages.

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 TTL Devices

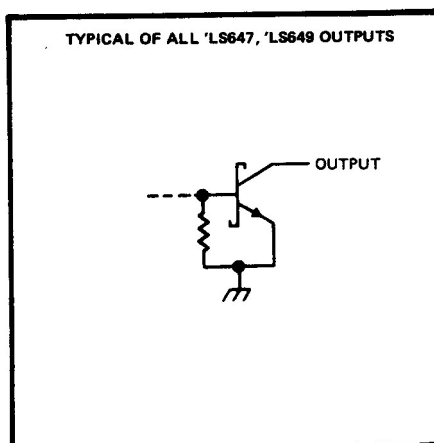
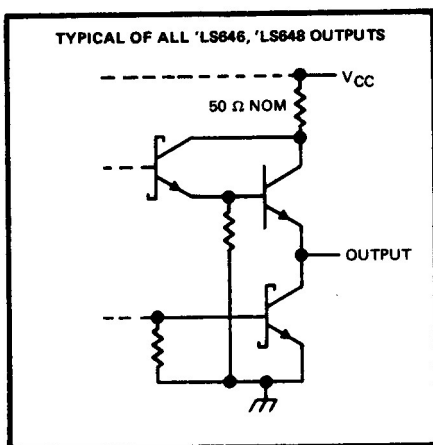
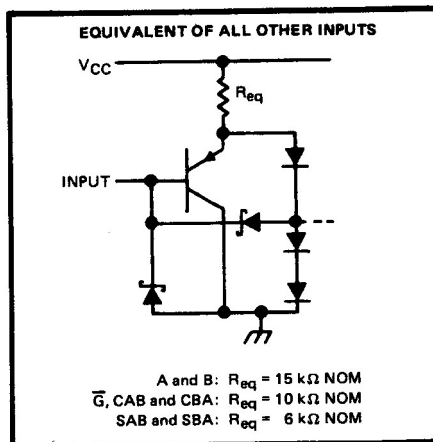
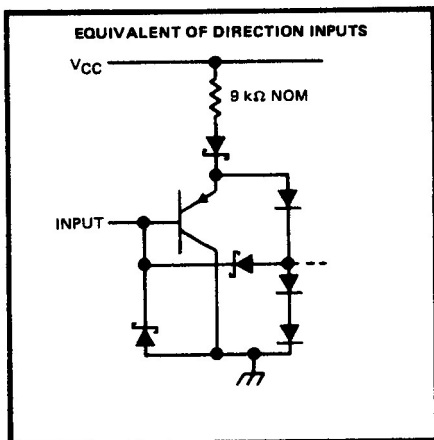
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**SN54LS646 THRU SN54LS649,
SN74LS646 THRU SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS**

schematics of inputs and outputs



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TTL Devices

SN54LS646, SN54LS648, SN74LS646, SN74LS648

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54LS646, SN54LS648	– 55°C to 125°C
SN74LS646, SN74LS648	0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

			SN54LS646/648			SN74LS646/648			UNIT		
			MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V		
V _{IH}	High-level input voltage		2			2			V		
V _{IL}	Low-level input voltage				0.5			0.6	V		
I _{OH}	High-level output current				− 12			− 15	mA		
I _{OL}	Low-level output current				12			24	mA		
t _w	Pulse duration	CBA or CAB high	15			15			ns		
		CBA or CAB low	30			30					
		Data high or low	30			30					
t _{su}	Setup time before CAB† or CBA †	A or B	15			15			ns		
t _h	Hold time after CAB† or CBA †	A or B	0			0			ns		
T _A	Operating free-air temperature		− 55			125			0	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS646/648		SN74LS646/648		UNIT	
				MIN	TYP‡	MAX	MIN		TYP‡
VIK		VCC = MIN, II = - 18 mA		- 1.5		- 1.5		V	
Hysteresis (VT+ - VT-)	A or B input	VCC = MIN		0.1	0.4	0.2	0.4	V	
VOH		VCC = MIN, VIH = 2 V, VIL = MAX		IOH = - 3 mA		2.4 3.4		V	
				IOH = - 12 mA		2			
				IOH = - 15 mA		2			
VOL		VCC = MIN, VIH = 2 V, VIL = MAX		IOL = 12 mA		0.25 0.4		V	
				IOL = 24 mA		0.35 0.5			
II	Control inputs	VCC = MAX, VI = 7 V		0.1		0.1		mA	
	A or B ports	VCC = MAX, VI = 5.5 V		0.1		0.1			
IIH	Control inputs	VCC = MAX, VI = 2.7 V		20		20		µA	
	A or B ports†			20		20			
IIL	Control inputs	VCC = MAX, VI = 0.4 V		- 0.4		- 0.4		mA	
	A or B ports†			- 0.4		- 0.4			
IOS‡		VCC = MAX, VO = 0 V		- 40	- 225	- 40	- 225	mA	
ICC	LS646	VCC = MAX		Outputs high	91	145	91	145	mA
				Outputs low	103	165	103	165	
				Outputs disabled	103	165	103	165	
	LS648			Outputs high	91	145	91	145	
				Outputs low	103	165	103	165	
				Outputs disabled	120	180	120	180	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

¶ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

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SN54LS646, SN54LS648, SN74LS646, SN74LS648
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS646		'LS648		UNIT
				MIN	TYP	MAX	MIN	
t_{PLH}	CAB or CBA	A or B	$R_L = 667\ \Omega, \quad C_L = 45\text{ pF},$ See Note 2	15	25	15	25	ns
t_{PHL}				23	35	24	40	ns
t_{PLH}				A or B	B or A	12	18	12
t_{PHL}	13	20				15	25	ns
t_{PLH}	SAB or SBA† with Bus input high	A or B		26	40	37	55	ns
t_{PHL}				21	35	24	40	ns
t_{PLH}	SAB or SBA† with Bus input low			33	50	26	40	ns
t_{PHL}				14	25	23	40	ns
t_{PZH}	\overline{G}	A or B		33	55	30	50	ns
t_{PZL}				42	65	37	55	ns
t_{PZH}	DIR			28	45	23	40	ns
t_{PZL}				39	60	30	45	ns
t_{PHZ}	\overline{G}	A or B	23	35	28	45	ns	
t_{PLZ}			22	35	22	35	ns	
t_{PHZ}	DIR		20	30	24	35	ns	
t_{PLZ}			19	30	19	30	ns	

† These parameters are measured with the internal output state of the storage register opposite to that of the input.
 NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

SN54LS647, SN54LS649, SN74LS647, SN74LS649

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (control inputs)	7 V
Off-state output voltage (A and B ports)	5.5 V
Operating free-air temperature range: SN54LS647, SN54LS649	– 55°C to 125°C
SN74LS647, SN74LS649	– 0°C to 70°C
Storage temperature range	– 65°C to 150°C

recommended operating conditions

		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage	0.5			0.6			V
V _{OH}	High-level output voltage	5.5			5.5			V
I _{OL}	Low-level output voltage	12			24			mA
t _w	Pulse duration	CBA or CAB high			15			ns
		CBA or CAB low			30			
		Data high or low			30			
t _{su}	Setup time before CAB † or CBA †	A or B			15			ns
t _h	Hold time after CAB † or CBA †	A or B			0			ns
T _A	Operating free-air temperature	− 55			125			°C

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TTL Devices

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS647 SN54LS649			SN74LS647 SN74LS649			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		– 1.5			– 1.5			V
Hysteresis ($V_{T+} - V_{T-}$)	A or B input	$V_{CC} = \text{MIN}$		0.1	0.4		0.2	0.4		V
I_{OH}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}, V_{OH} = 5.5 \text{ V}$		0.1			0.1			mA
V_{OL}		$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = \text{MAX}$	$I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$	0.25	0.4		0.25	0.4		V
I_I	A or B	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$	0.1			0.1			mA
	All others	$V_{CC} = \text{MAX}$	$V_I = 7 \text{ V}$	0.1			0.1			mA
I_{IH}		$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20			20			µA
I_{IL}		$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$		– 0.4			– 0.4			mA
I_{CC}	'LS647	$V_{CC} = \text{MAX}, \text{Outputs open}$	Outputs high	79	130		79	130		mA
			Outputs low	94	150		94	150		
	'LS649	$V_{CC} = \text{MAX}, \text{Outputs open}$	Outputs high	79	130		79	130		
			Outputs low	94	150		94	150		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$.

TEXAS
INSTRUMENTS

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SN54LS647, SN54LS649, SN74LS647, SN74LS649
OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS647			'LS649			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	CAB or CBA	A or B	$R_L = 667\ \Omega$, $C_L = 45\ \text{pF}$, See Note 2	22	35	17	30	ns		
t_{PHL}				28	45	28	45	ns		
t_{PLH}	A or B	B or A		17	26	15	25	ns		
t_{PHL}				18	27	20	30	ns		
t_{PLH}	SAB or SBA [†] with Bus input high	A or B		33	50	37	55	ns		
t_{PHL}					29	45	28	45	ns	
t_{PLH}	SAB or SBA [†] with Bus input low	A or B		39	60	30	45	ns		
t_{PHL}					19	30	26	40	ns	
t_{PLH}	G	A or B		25	40	21	40	ns		
t_{PHL}					33	50	34	50	ns	
t_{PLH}	DIR	A or B		23	35	19	30	ns		
t_{PHL}					25	40	27	45	ns	

† These parameters are measured with the internal outputs state of the storage register opposite to that of the bus input.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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TTL Devices