Rochester Electronics

Datasheet

PART NUMBER

9511A

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Am9511A

Arithmetic Processor

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- 2 and 3 MHz operation; fixed point 16-bit and 32-bit operations
- Floating point 32-bit operations; binary data formats
- Add, Subtract, Multiply and Divide; trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation; float-to-fixed fixed-to-float conversions
- Stack-oriented operand storage; DMA or programmed I/O data transfers
- End signal simplifies concurrent processing; Synchronous/Asynchronous operations
- General purpose 8-bit data bus interface; standard 24-pin package

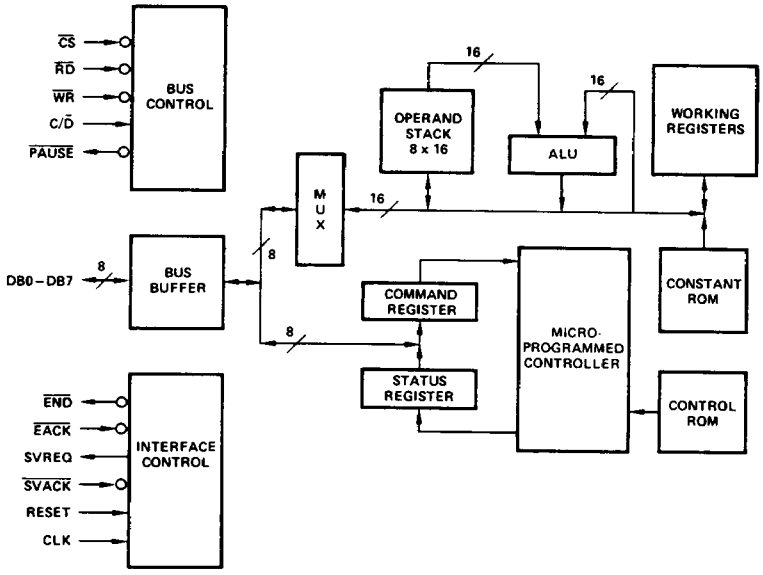
GENERAL DESCRIPTION

The Am9511A Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high-performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack, and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end-of-execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

BLOCK DIAGRAM



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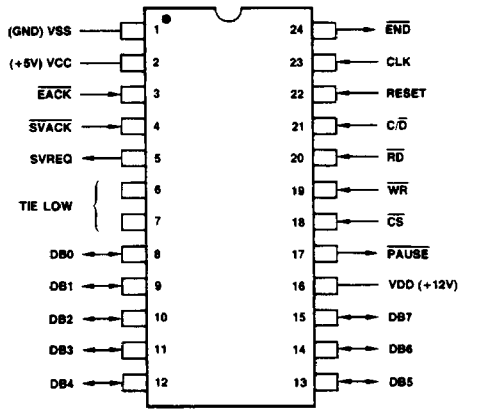
Publication # 09224 | Rev. A | Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View



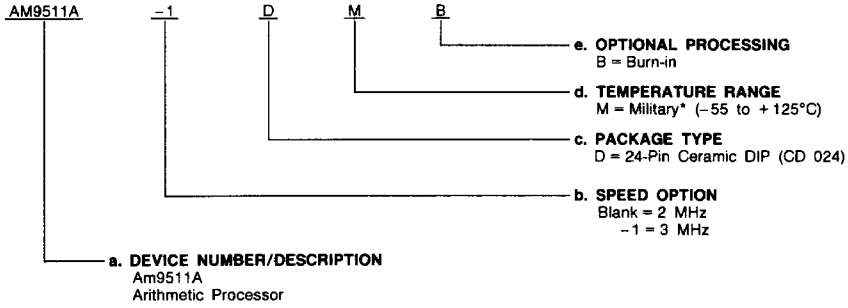
CD005172

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

NPL Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM9511A	DMB
AM9511A-1	

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
V_{DD} with Respect to V_{SS} ..... −0.5 V to +15.0 V
V_{CC} with Respect to V_{SS} ..... −0.5 V to +7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −5.0 V to +7.0 V
Power Dissipation (Package Limitation) ..... 2.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%
(V_{DD}) ..... 12 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

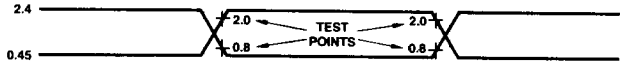
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −200 μA	3.7		V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}*	V
V_{IL}	Input LOW Voltage			0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		±10	μA
I_{OZ}	Data Bus Leakage	V_O = 0.4 V	−10		μA
		V_O =		10	
I_{CC}	V_{CC} Supply Current			100	mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_O	Output Capacitance	f_C = 1.0 MHz, Inputs = 0 V		10*	pF
C_I	Input Capacitance			8*	pF
C_{IO}	I/O Capacitance			12*	pF

*Not tested; guaranteed by design.

SWITCHING TEST INPUT WAVEFORM



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SWITCHING CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description		Am9511A Min.	Am9511A Max.	Am9511A-1 Min.	Am9511A-1 Max.	Unit
TAPW	$\overline{EACK}$ LOW Pulse Width		100		75		ns
TCDR	C/$\overline{D}$ to $\overline{RD}$ LOW Setup Time		0		0		ns
TCDW	C/$\overline{D}$ to $\overline{WR}$ LOW Setup Time		0		0		ns
TCPH	Clock Pulse HIGH Width		200		140		ns
TCPL	Clock Pulse LOW Width		240		160		ns
TCSR	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup Time		0		0		ns
TCSW	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup Time		0		0		ns
TCY	Clock Period		480	5000	320	3300	ns
TDW	Data Bus Stable to $\overline{WR}$ HIGH Setup Time		150		150		ns
TEAE	$\overline{EACK}$ LOW to $\overline{END}$ HIGH Delay			20		175	ns
TEPW	$\overline{END}$ LOW Pulse Width (Note 4)		400		270		ns
TOP	Data Bus Output Valid to $\overline{PAUSE}$ HIGH Delay		0		0		ns
TPPWR	$\overline{PAUSE}$ LOW Pulse Width Read (Note 5)	Data	3.5TCY + 50	5.5TCY + 300	3.5TCY + 50	5.5TCY + 200	ns
		Status	3.5TCY + 50	3.5TCY + 300	1.5TCY + 50	3.5TCY + 200	
TPPWW	$\overline{PAUSE}$ LOW Pulse Width Write (Note 8)			50		50	ns
TPR	$\overline{PAUSE}$ HIGH to $\overline{RD}$ HIGH Hold Time		0		0		ns
TPW	$\overline{PAUSE}$ HIGH to $\overline{WR}$ HIGH Hold Time		0		0		ns
TRCD	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold Time		0		0		ns
TRCS	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH Hold Time		0		0		ns
TRO	$\overline{RD}$ LOW to Data Bus ON Delay		50		50		ns
TRP	$\overline{RD}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		150	ns
TRZ	$\overline{RD}$ HIGH to Data Bus OFF Delay		50	200	50	150	ns
TSAPW	$\overline{SVACK}$ LOW Pulse Width		100		75		ns
TSAR	$\overline{SVACK}$ LOW to SVREQ LOW Delay			300		200	ns
TWCD	$\overline{WR}$ HIGH to C/$\overline{D}$ Hold Time		60		30		ns
TWCS	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold Time		60		30		ns
TWD	$\overline{WR}$ HIGH to Data Bus Hold Time		20		20		ns
TWI	Write Inactive Time	Command	4TCY		4TCY		ns
		Data	5TCY		5TCY		
TWP	$\overline{WR}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		150	ns

Notes:
1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20 ns or less, output loading of one TTL gate plus 100 pF ±20 pF and timing reference levels of 0.8 V and 2.0 V.
4. $\overline{END}$ low pulse width is specified for $\overline{EACK}$ tied to V_{SS}. Otherwise TEAE applies.
5. Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown.
6. $\overline{PAUSE}$ is pulled low for both command and data operations.
7. TEX is the execution time of the current command (see the Command Execution Times table).
8. $\overline{PAUSE}$ low pulse width is less than 50 ns when writing into the data port or the control port as long as the duty requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated up to 500 ns as long as the extended TPPWW that results is observed. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown.

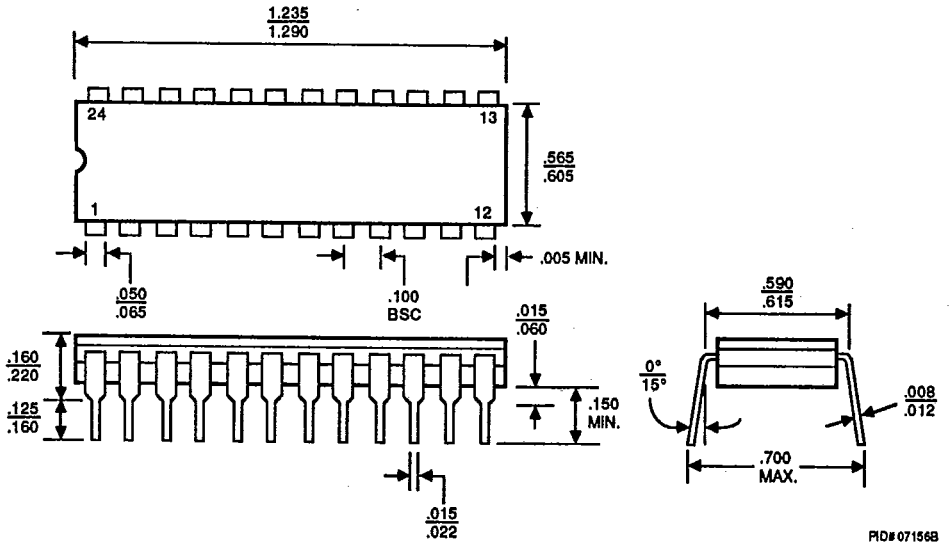
CHAPTER 6
General Information

T-90-20

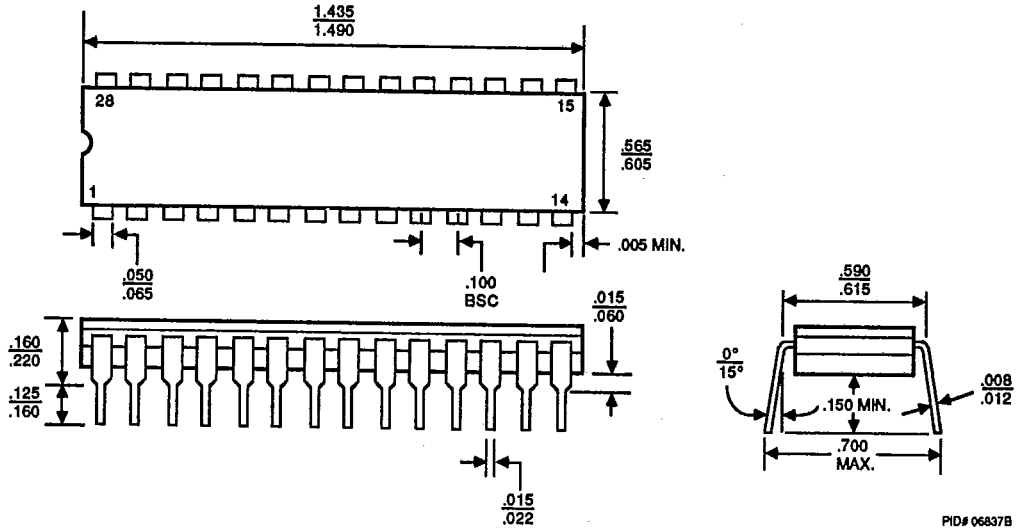
PACKAGE OUTLINES*

Ceramic DIPs (CD)

CD 024



CD 028



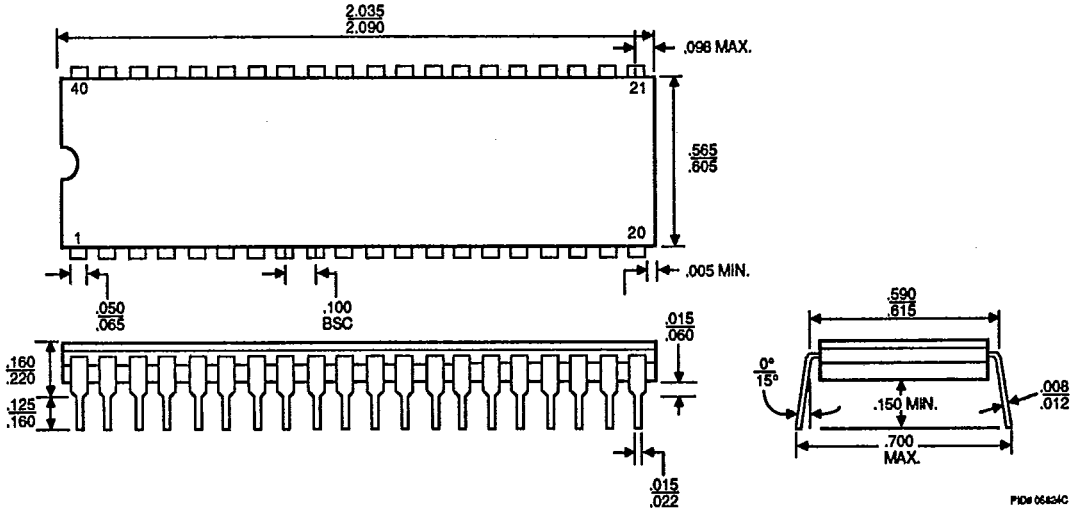
* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

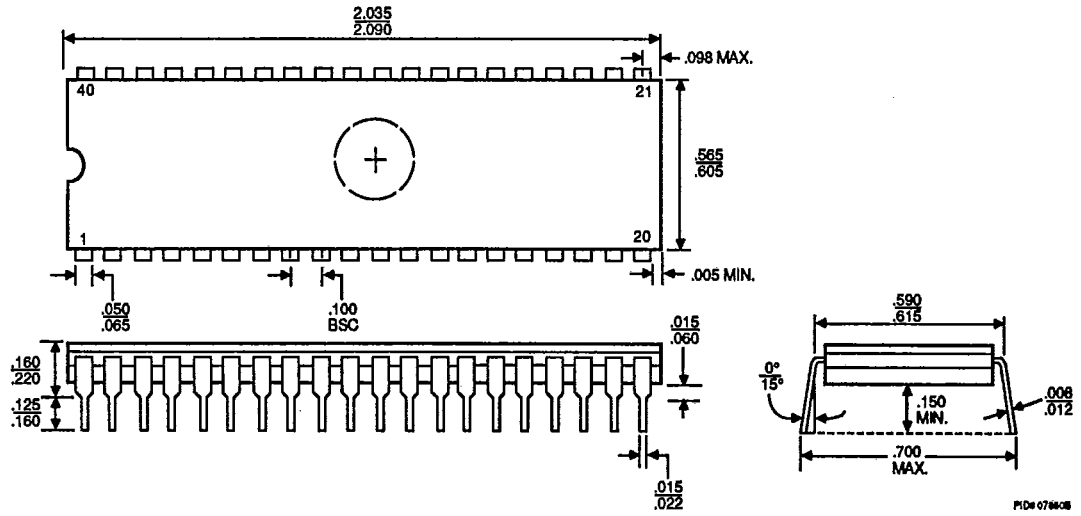
PACKAGE OUTLINES (Continued)

Ceramic DIPs (CD) (Continued)

CD 040



CDV040



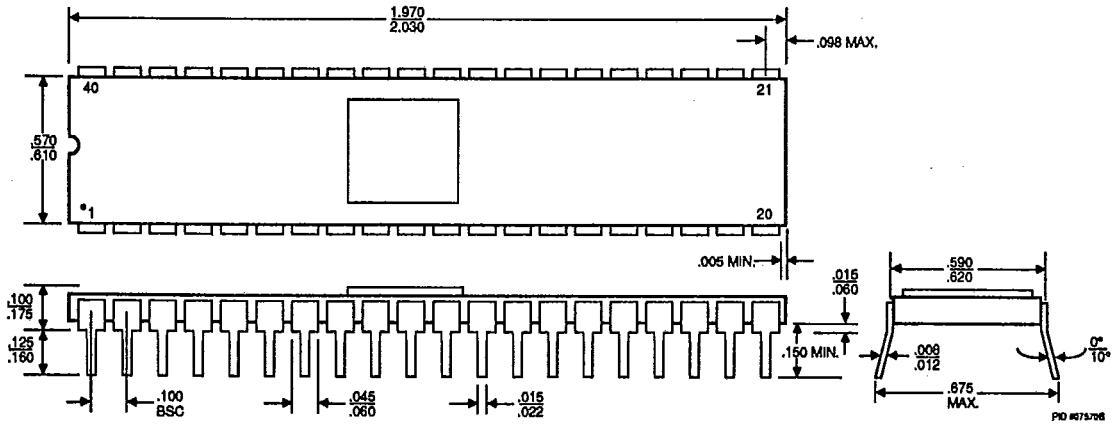
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

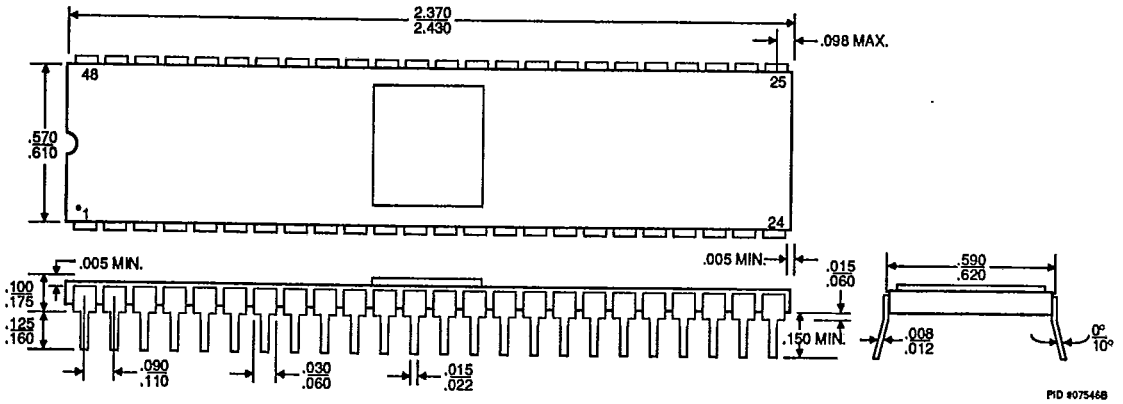
T-90-20

Ceramic Sidebrazed DIPs (SD)

SD 040



SD 048



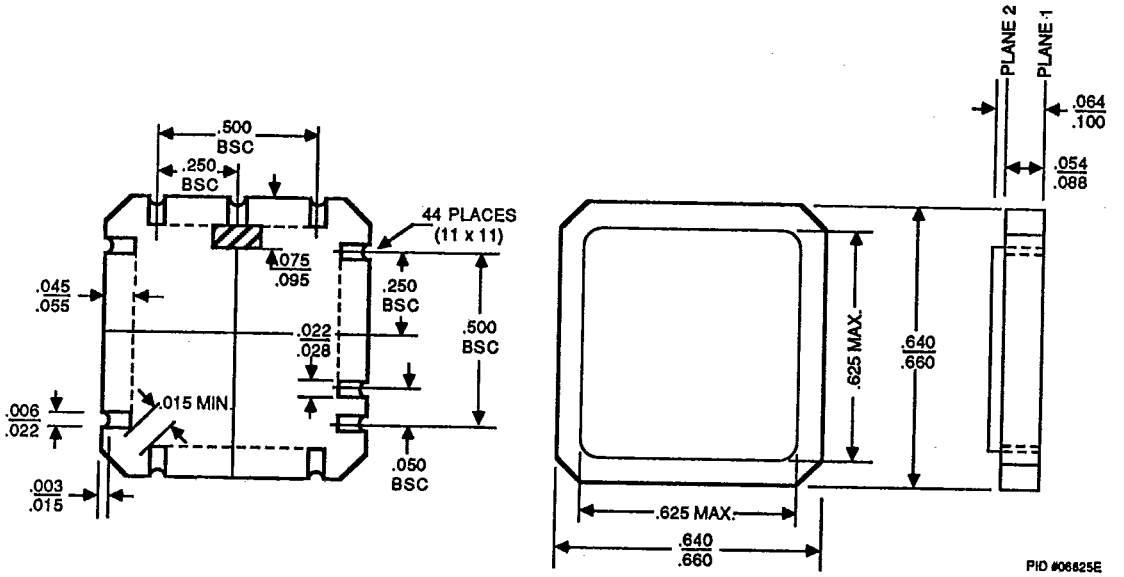
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

1782 A-13

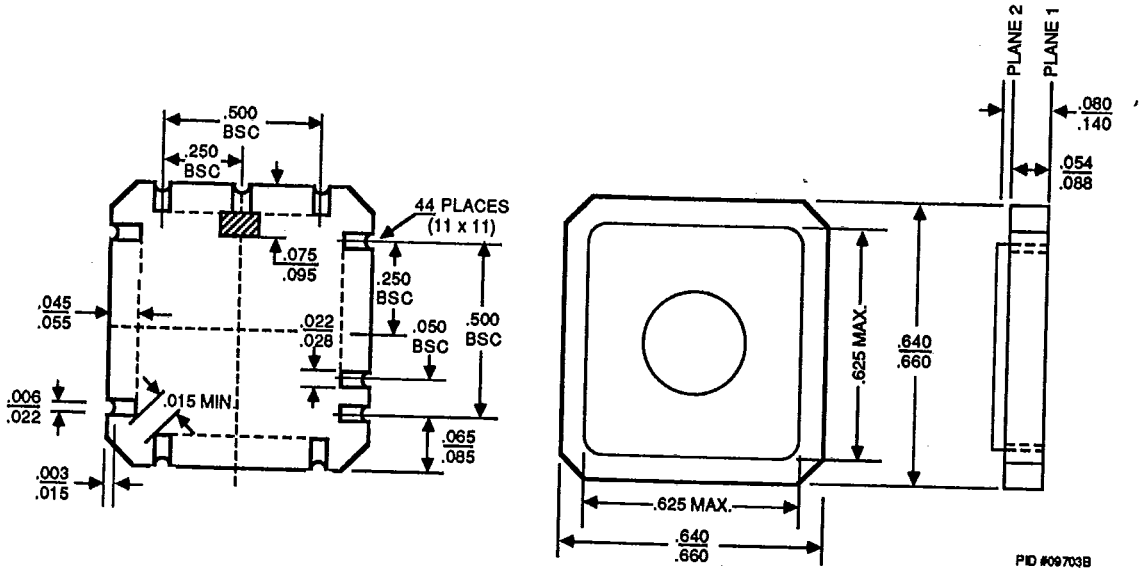
PACKAGE OUTLINES (Continued)

Ceramic Leadless Chip Carriers (CL/CLV)

CL 044



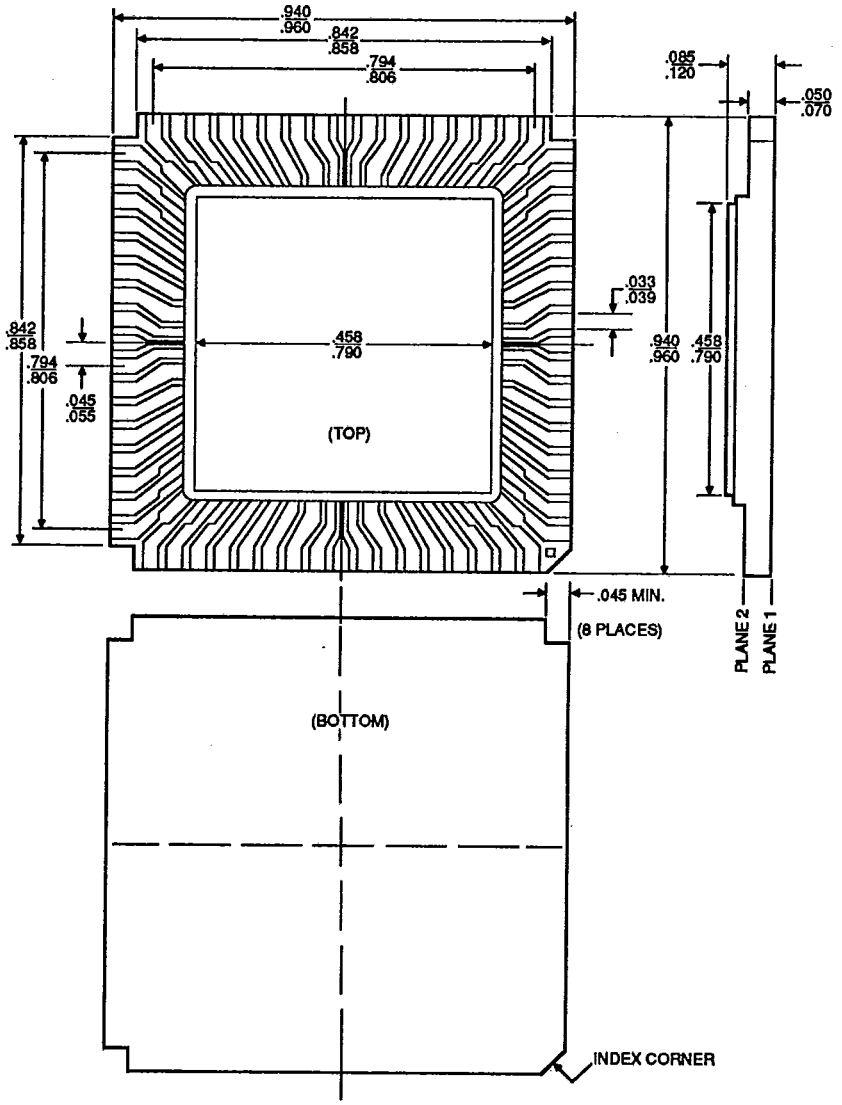
CLV044



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

68-Pin Square Leadless Chip Carrier (CA2)
CA2068



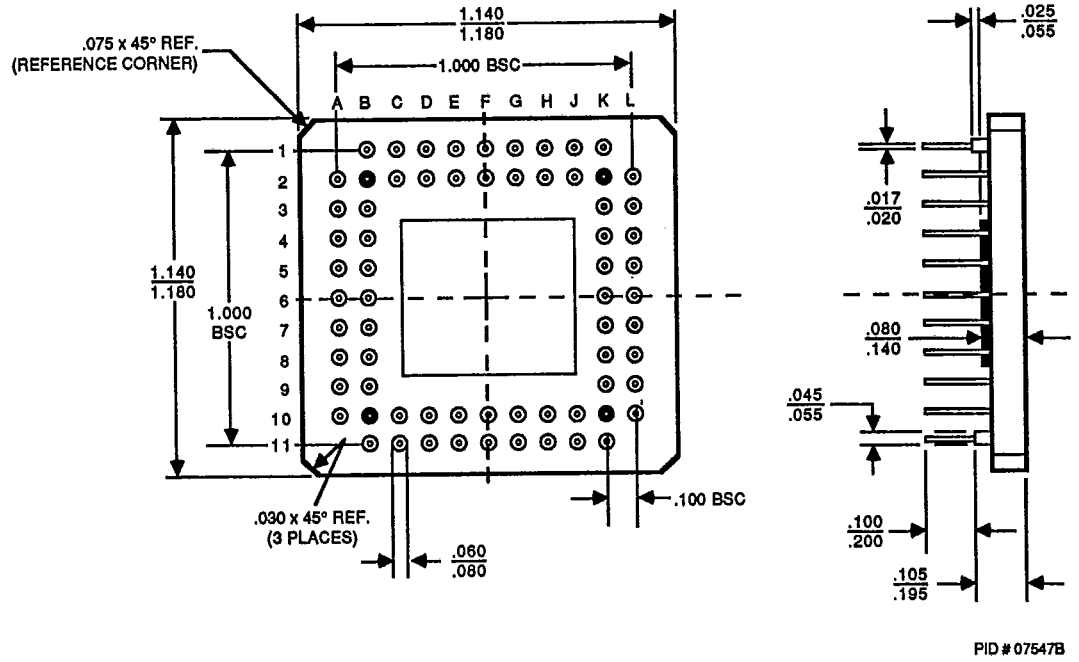
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

Ceramic Pin-Grid-Array Package (CG/CGX)

CGX068

BOTTOM VIEW



PID # 07547B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.