
PART NUMBER**UC2633N-G-ROCV**

**Rochester Electronics
Manufactured Components**

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Phase Locked Frequency Controller

FEATURES

- Precision Phase Locked Frequency Control System
- Crystal Oscillator
- Programmable Reference Frequency Dividers
- Phase Detector with Absolute Frequency Steering
- Digital Lock Indicator
- Double Edge Option on the Frequency Feedback Sensing Amplifier
- Two High Current Op-Amps
- 5V Reference Output

DESCRIPTION

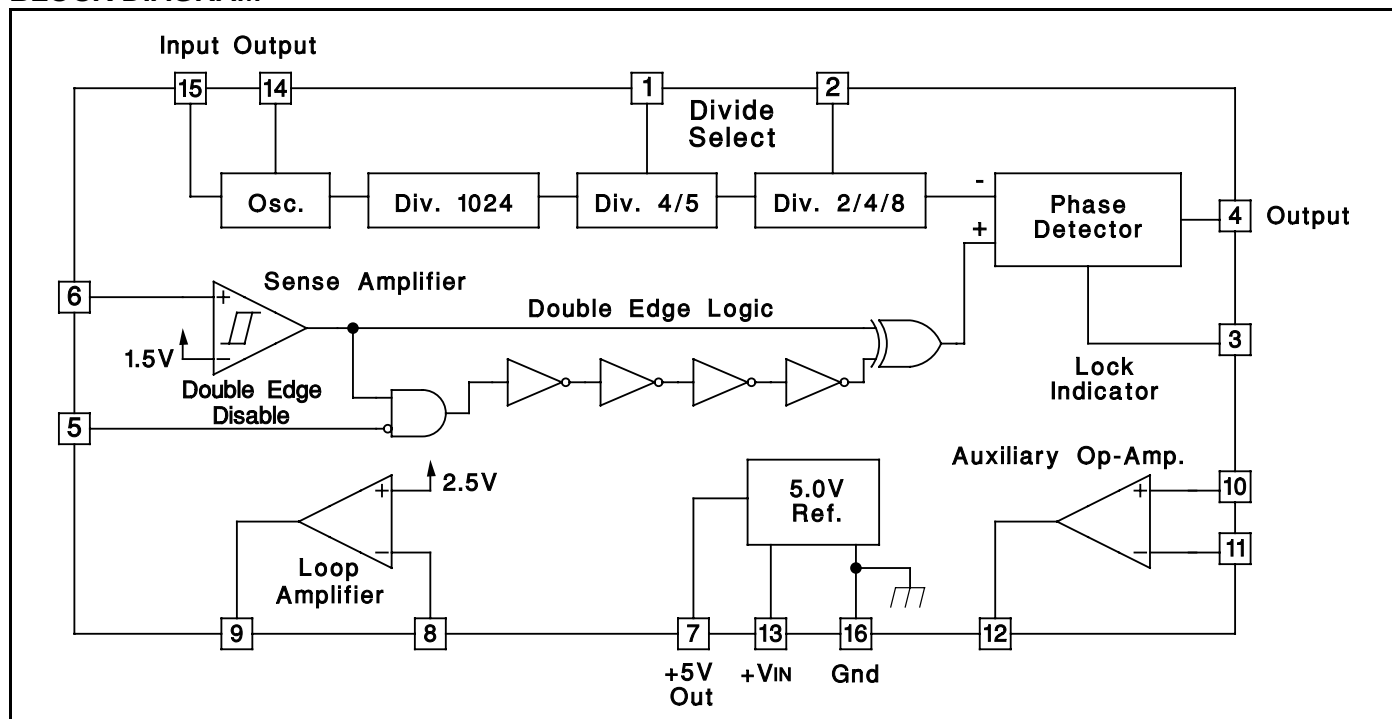
The UC1633 family of integrated circuits was designed for use in phase locked frequency control loops. While optimized for precision speed control of DC motors, these devices are universal enough for most applications that require phase locked control. A precise reference frequency can be generated using the device's high frequency oscillator and programmable frequency dividers. The oscillator operates using a broad range of crystals, or, can function as a buffer stage to an external frequency source.

The phase detector on these integrated circuits compares the reference frequency with a frequency/phase feedback signal. In the case of a motor, feedback is obtained at a hall output of other speed detection device. This signal is buffered by a sense amplifier that squares up the signal as it goes into the digital phase detector. The phase detector responds proportionally to the phase error between the reference and the sense amplifier output. This phase detector includes absolute frequency steering to provide maximum drive signals when any frequency error exists. This feature allows optimum start-up and lock times to be realized.

Two op-amps are included that can be configured to provide necessary loop filtering. The outputs of the op-amps will source or sink in excess of 16mA, so they can provide a low impedance control signal to driving circuits.

Additional features include a double edge option on the sense amplifier that can be used to double the loop reference frequency for increased loop bandwidths. A digital lock signal is provided that indicates when there is zero frequency error, and a 5V reference output allows DC operating levels to be accurately set.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (+VIN)	+20V
Reference Output Current	-30mA
Op-Amp Output Currents	±30mA
Op-Amp Input Voltages	-3V to +20V
Phase Detector Output Current	±10mA
Lock Indicator Output Current	+15mA
Lock Indicator Output Voltage	+20V
Divide Select Input Voltages	-3V to +10V
Double Edge Disable Input Voltage	-3V to +10V
Oscillator Input Voltage	-3V to +5V
Sense Amplifier Input Voltage	.3V to +20V
Power Dissipation at TA = 25°C (Note 2)	1000mW
Power dissipation at Tc = 25°C (Note 2)	2000mW
Operating Junction Temperature	-55°C to +150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

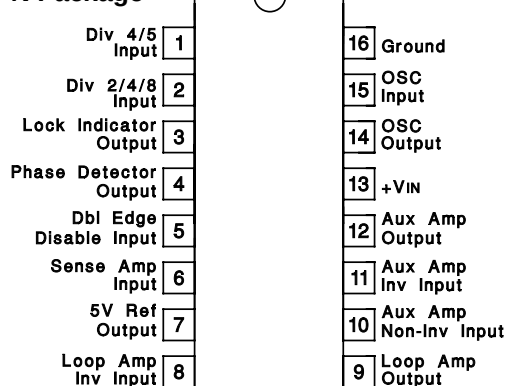
Note1: Voltages are referenced to ground, (Pin 16). Currents are positive into, negative out of, the specified terminals.

Note 2: Consult Packaging Section of Databook for thermal limitations and considerations of package.

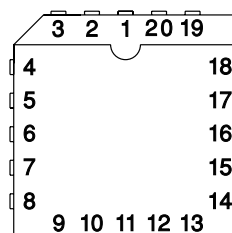
CONNECTION DIAGRAMS

DIL-16 (TOP VIEW)

J or N Package



PLCC-20 (TOP VIEW) Q Package



PACKAGE PIN FUNCTION

FUNCTION	PIN
N/C	1
Div 4/5 Input	2
Div 2/4/8 Input	3
Lock Indicator Output	4
Phase Detector Output	5
N/C	6
Dbl Edge Disable Input	7
Sense Amp Input	8
5V Ref Output	9
Loop Amp Inv Input	10
N/C	11
Loop Amp Output	12
Aux Amp Non-Inv Input	13
Aux Amp Inv Input	14
Aux Amp Output	15
N/C	16
+VIN	17
OSC Output	18
OSC Input	19
Ground	20

ELECTRICAL CHARACTERISTICS: (Unless otherwise stated, these specifications apply for TA = 0°C to +70°C for the UC3633, -25°C to +85°C for the UC2633, -55°C to +125°C for the UC1633, +VIN = 12V; TA=TJ.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	+VIN = 15V		20	28	mA
Reference					
Output Voltage (VREF)		4.75	5.0	5.25	V
Load Regulation	IOUT = 0V to 7mA		5.0	20	mV
Line Regulation	+VIN = 8V to 15V		2.0	20	mV
Short Circuit Current	VOUT = 0V	12	30		mA
Oscillator					
DC Voltage Gain	Oscillator Input to Oscillator Output	12	16	20	dB
Input DC Level (VIB)	Oscillator Input Pin Open, TJ = 25°C	1.15	1.3	1.45	V
Input Impedance (Note 3)	VIN = VIB ±0.5V, TJ = 25°C	1.3	1.6	1.9	kΩ
Output DC Level	Oscillator Input Pin Open, TJ = 25°C	1.2	1.4	1.6	V
Maximum Operating Frequency		10			MHz
Dividers					
Maximum Input Frequency	Input = 1VPP at Oscillator Input	10			MHz
Div. 4/5 Input Current	Input = 5V (Div. by 4)		150	500	μA
	Input = 0V (Div. by 5)	-5.0	0.0	5.0	μA
Div. 4/5 Threshold		0.5	1.6	2.2	V

Note 3: These impedance levels will vary with TJ at about 1700ppm/°C

ELECTRICAL CHARACTERISTICS (cont.): (Unless otherwise stated, these specifications apply for $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ for the UC3633, -25°C to $+85^\circ\text{C}$ for the UC2633, -55°C to $+125^\circ\text{C}$ for the UC1633, $+V_{IN} = 12\text{V}$; $T_A = T_J$.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Dividers (cont.)					
Div. 2/4/8 Input Current	Input = 5V (Div. by 8)		150	500	μA
	Input = 0V (Div. by 2)	-500	-150		μA
Div. 2/4/8 Open Circuit Voltage	Input Current = $0\mu\text{A}$ (Div. by 4)	1.5	2.5	3.5	V
Div. by 2 Threshold		0.20	0.8		V
Div. by 4 Threshold		1.5		3.5	V
Div. by 8 Threshold	Volts Below V_{REF}	0.20	0.8		V
Sense Amplifier					
Threshold Voltage	Percent of V_{REF}	27	30	33	%
Threshold Hysteresis			10		mV
Input Bias Current	Input = 1.5V	-1.0	-0.2		μA
Double Edge Disable Input					
Input Current	Input = 5V (Disabled)		150	500	μA
	Input = 0V (Enabled)	-5.0	0.0	5.0	μA
Threshold Voltage		0.5	1.6	2.2	V
Phase Detector					
High Output Level	Positive Phase/Freq. Error, Volts Below V_{REF}		0.2	0.5	V
Low Output Level	Negative Phase/Freq. Error		0.2	0.5	V
Mid Output Level	Zero Phase/Freq. Error, Percent of V_{REF}	47	50	53	%
High Level Maximum Source Current	$V_{OUT} = 4.3\text{V}$	2.0	8.0		mA
Low Level Maximum Sink Current	$V_{OUT} = 0.7\text{V}$	2.0	5.0		mA
Mid Level Output Impedance (Note 3)	$I_{OUT} = -200$ to $+200\mu\text{A}$, $T_J = 25^\circ\text{C}$	4.5	6.0	7.5	$\text{k}\Omega$
Lock Indicator Output					
Saturation Voltage	Freq. Error, $I_{OUT} = 5\text{mA}$		0.3	0.45	V
Leakage Current	Zero Freq. Error, $V_{OUT} = 15\text{V}$		0.1	1.0	μA
Loop Amplifier					
NON INV. Reference Voltage	Percent of V_{REF}	47	50	53	%
Input Bias Current	Input = 2.5V	-0.8	-0.2		μA
AVOL		60	75		dB
PSRR	$+V_{IN} = 8\text{V}$ to 15V	70	100		dB
Short Circuit Current	Source, $V_{OUT} = 0\text{V}$	16	35		mA
	Sink, $V_{OUT} = 5\text{V}$	16	30		mA
Auxiliary Op-Amp					
Input Offset Voltage	$V_{CM} = 2.5\text{V}$			8	mV
Input Bias Current	$V_{CM} = 2.5\text{V}$	-0.8	-0.2		μA
Input Offset Current	$V_{CM} = 2.5\text{V}$		.01	0.1	μA
AVOL		70	120		dB
PSRR	$+V_{IN} = 8\text{V}$ to 15V	70	100		dB
CMRR	$V_{CM} = 0\text{V}$ to 10V	70	100		dB
Short Circuit Current	Source, $V_{OUT} = 0\text{V}$	16	35		mA
	Sink, $V_{OUT} = 5\text{V}$	16	30		mA

Note 3: These impedance levels will vary with T_J at about $1700\text{ppm}/^\circ\text{C}$

APPLICATION AND OPERATING INFORMATION

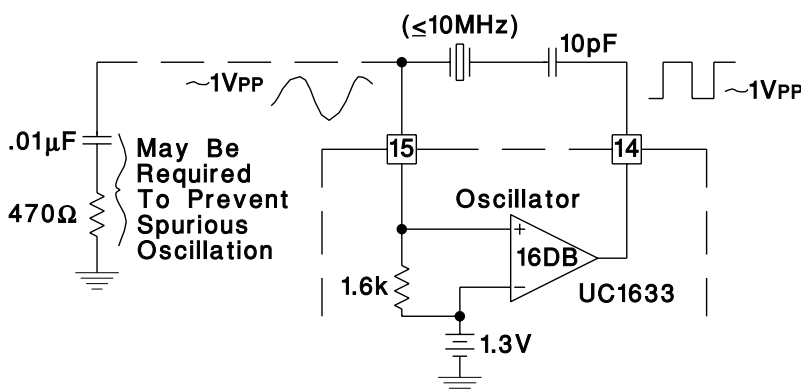
Determining the Oscillator Frequency

The frequency at the oscillator is determined by the desired RPM of the motor, the divide ratio selected, the number of poles in the motor, and the state of the double edge select pin.

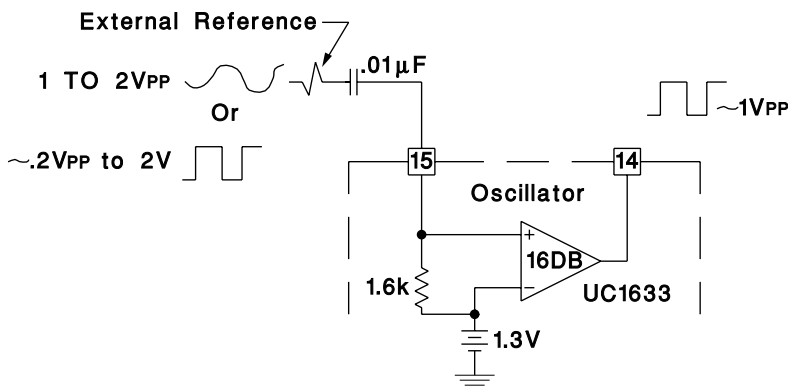
$$f_{osc}(\text{Hz}) = (\text{Divide Ratio}) \cdot (\text{Motor RPM}) \cdot (1/60 \text{ SEC/MIN}) \cdot (\text{No. of Rotor Poles}/2) \cdot (x 2 \text{ if Pin 5 Low})$$

The resulting reference frequency appearing at the phase detector inputs is equal to the oscillator frequency divided by the selected divide ratio. If the double edge option is used, (Pin 5 low), the frequency of the sense amplifier input signal is doubled by responding to both the rising and falling edges of the input signal. Using this option, the loop reference frequency can be doubled for a given motor RPM.

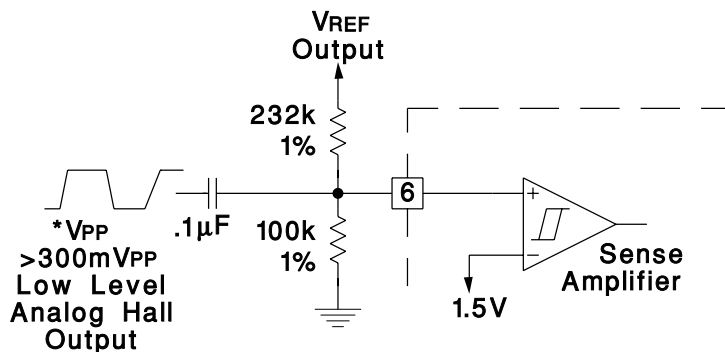
Recommended Oscillator Configuration Using AT Cut Quartz Crystal



External Reference Frequency Input



Method for Deriving Rotation Feedback Signal from Analog Hall Effect Device



**This signal may require filtering if chopped mode drive scheme is used.*

APPLICATION AND OPERATION INFORMATION

Phase Detector Operation

The phase detector on these devices is a digital circuit that responds to the rising edges of the detector's two inputs. The phase detector output has three states: a high, 5V state, a low, 0V state, and a middle, 2.5V state. In the high and low states the output impedance of the detector is low and the middle state output impedance is high, typically 6.0k Ω . When there is any static frequency difference between the inputs, the detector output is fixed at its high level if the +input (the sense amplifier signal) is greater in frequency, and fixed at its low level if the -input (the reference frequency signal) is greater in frequency.

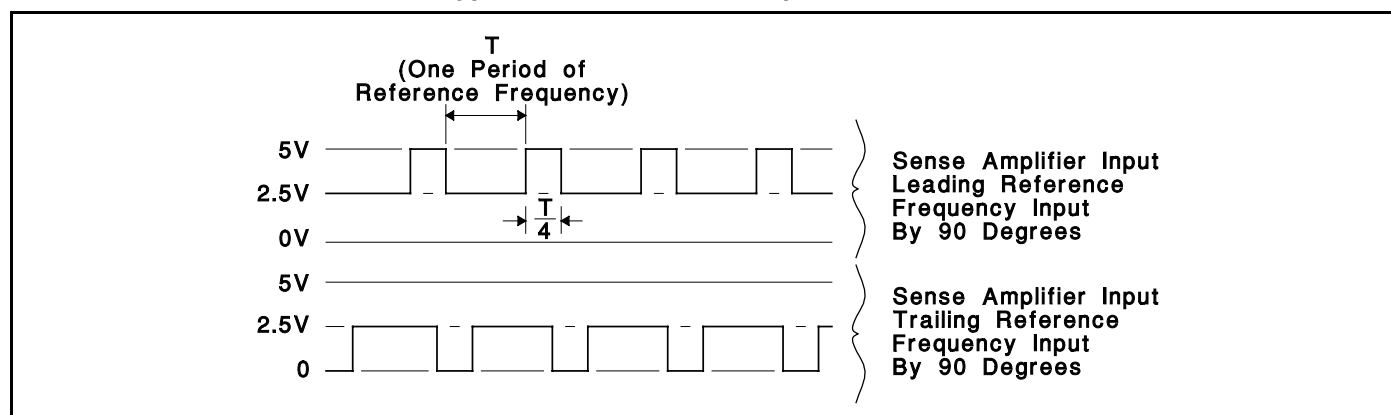
When the frequencies of the two inputs to the detector are equal, the phase detector switches between its middle state and either the high or low states, depending on the relative phase of the two signals. If the +input is leading in phase then, during each period of the input frequency, the detector output will be high for a time equal to the time difference between the rising edges of the inputs, and will be at its middle level for the remainder of the period. If the phase relationship is reversed, then the detector will go low for a time proportional to the phase difference of the inputs. The resulting gain of the phase detector, k_{ϕ} , is

$5V/4\pi$ radians or about 0.4V/radian. The dynamic range of the detector is $\pm 2\pi$ radians.

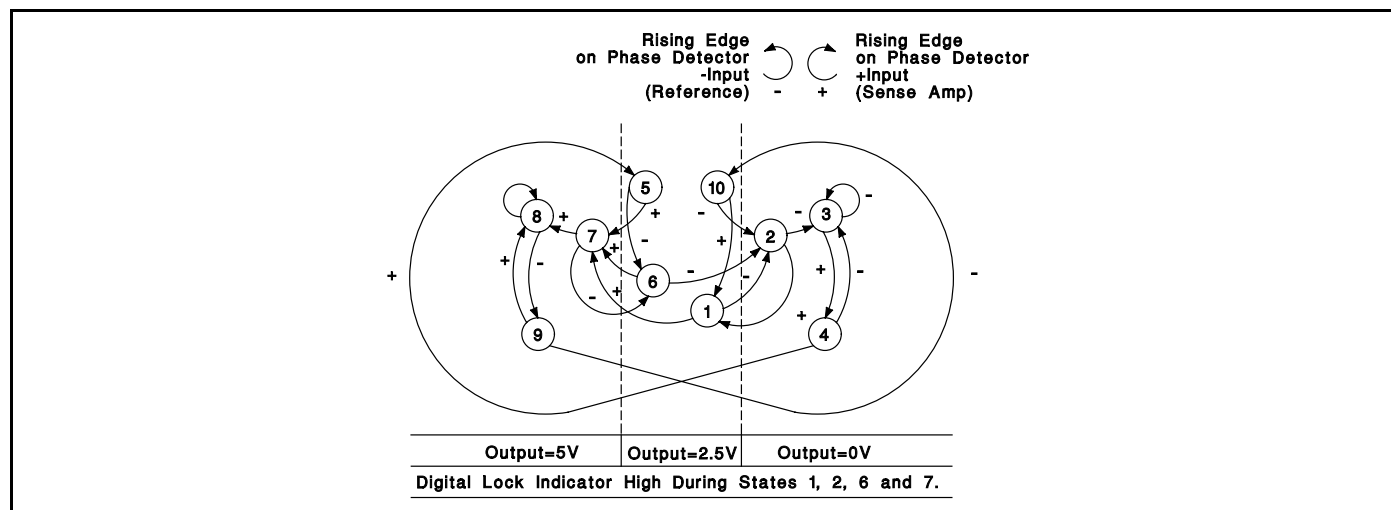
The operation of the phase detector is illustrated in the figures below. The upper figure shows typical voltage waveforms seen at the detector output for leading and lagging phase conditions. The lower figure is a state diagram of the phase detector logic. In this figure, the circles represent the 10 possible states of the logic, and the connecting arrows represent the transition events/paths to and from these states. Transition arrows that have a clockwise rotation are the result of a rising edge on the +input, and conversely, those with counter-clockwise rotation are tied to the rising edge of the -input signal.

The normal operational states of the logic are 6 and 7 for positive phase error, 1 and 2 for a negative phase error. States 8 and 9 occur during positive frequency error, 3 and 4 during negative frequency error. States 5 and 10 occur only as the inputs cross over from the frequency error to a normal phase error only condition. The level of the phase detector output is determined by the logic state as defined in the state diagram figure. The lock indicator output is high, off, when the detector is in states 1, 2, 6, or 7.

Typical Phase Detector Output Waveforms

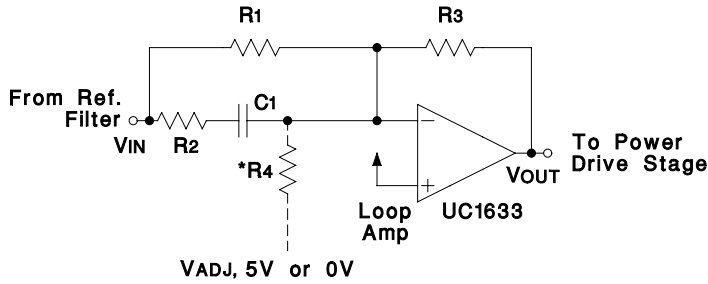


Phase Detector State Diagram



APPLICATION AND OPERATION INFORMATION

Suggested Loop Filter Configuration



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{R_3}{R_1} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p}$$

$$\omega_p = \frac{1}{R_2 C_1}$$

$$\omega_z = \frac{1}{(R_1 + R_2) C_1}$$

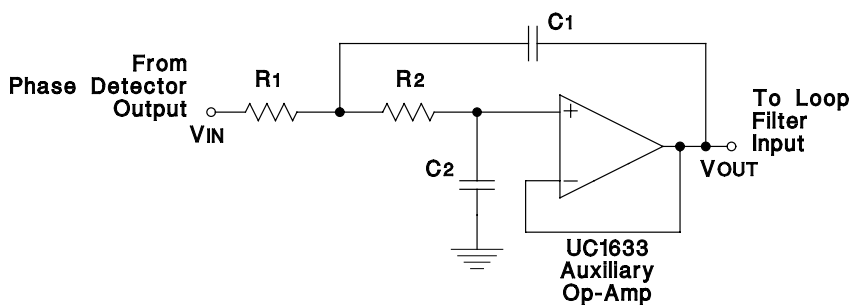
* The static phase error of the loop is easily adjusted by adding resistor, R4, as shown. To lock at zero phase error R4 is determined by:

$$R_4 = \frac{2.5V \cdot R_3}{|\Delta V_{OUT}|}$$

Where: $|\Delta V_{OUT}| = |V_{OUT} - 2.5V|$
and V_{OUT} = DC Operating Voltage At
Loop Amplifier Output During Phase Lock

If: $(V_{OUT} - 2.5) > 0$, R4 Goes to 0V
 $(V_{OUT} - 2.5) < 0$, R4 Goes to 5.0V

Reference Filter Configuration



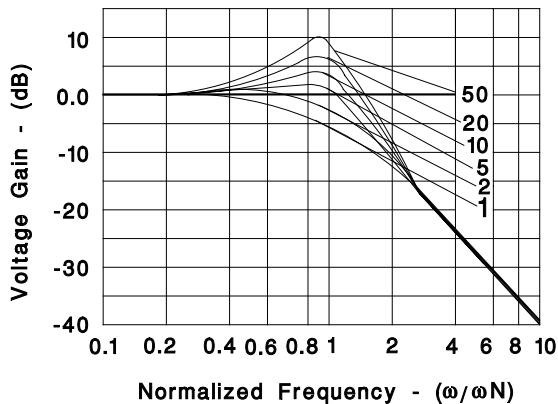
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s^2 \zeta^2}{\omega_N^2} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2} \sqrt{\frac{C_2}{C_1}} \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

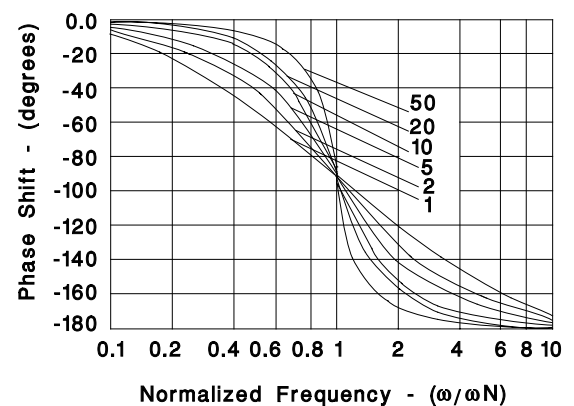
Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid - Gain Response



Variable is $1/\zeta^2$
(For $R_1=R_2$, $1/\zeta^2=C_1/C_2$)

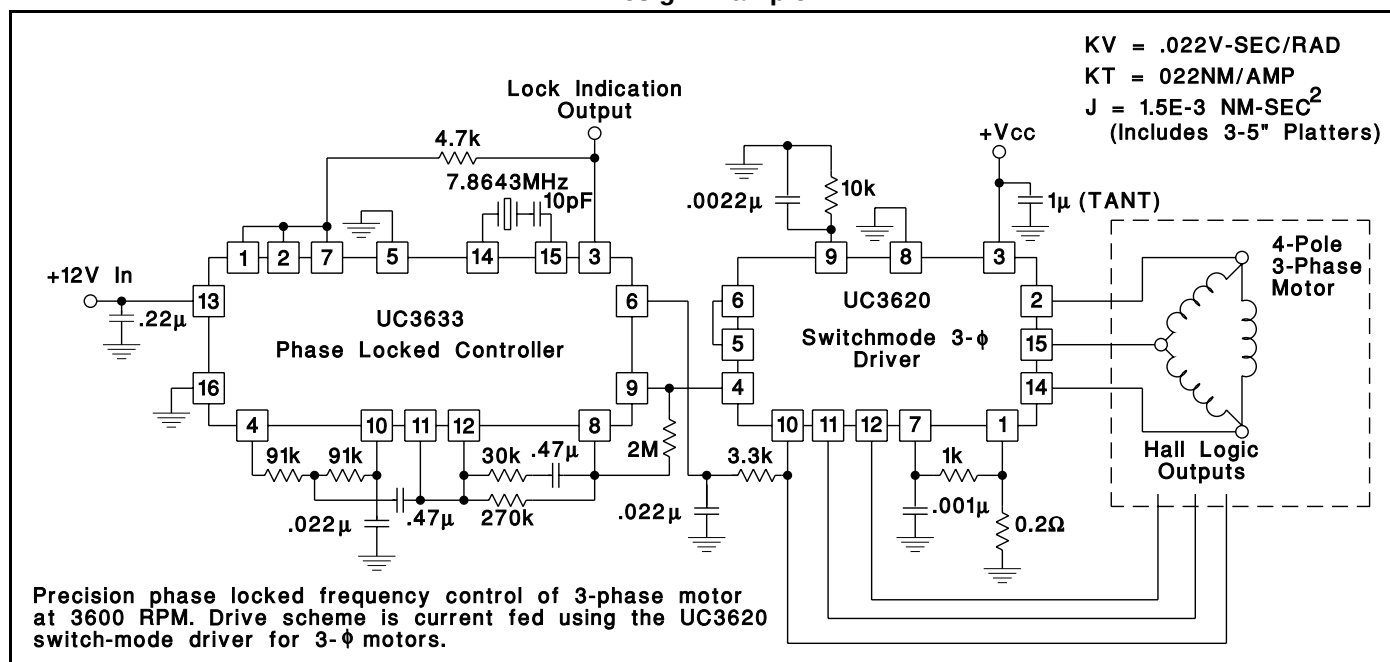
Reference Filter Design Aid - Phase Response



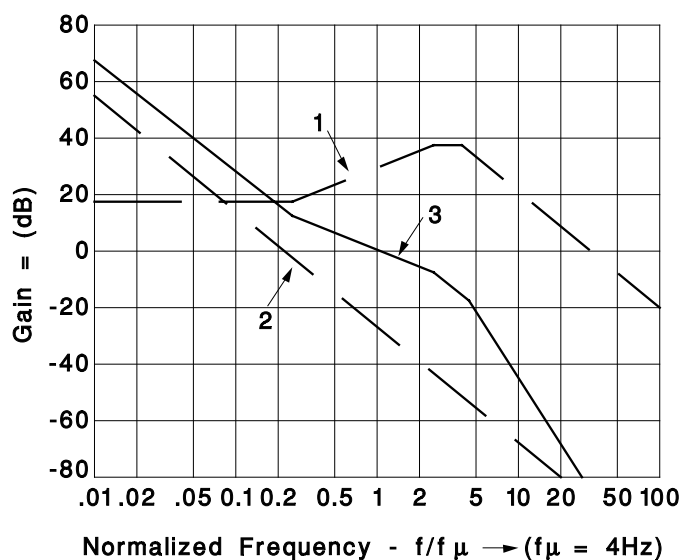
Variable is $1/\zeta^2$
(For $R_1=R_2$, $1/\zeta^2=C_1/C_2$)

APPLICATION AND OPERATION INFORMATION

Design Example



Bode Plots - Design Example Open Loop Response



- 1.) $K_{LF}(s) \cdot K_{RF}(s)$
- 2.)* $\frac{N \cdot K_{\phi} \cdot G_{PD} \cdot K_T}{s^2 \cdot J}$
- 3.) Combined Overall Open Loop Response

Where:

$K_{LF}(s)$ = Loop Filter Response

$K_{RF}(s)$ = Reference Filter Response

$N = 4$ (Using Double Edge Sensing With 4 Pole Motor)

K_{ϕ} = Phase Detector Gain (.4V/RAD)

G_{PD} = Power Stage Transductance (1A/V)

K_T = Motor Torque Constant (.022NM/A)

J = Motor Moment of Inertia (.0015NM/A - SEC²)

$s = 2\pi jf$

*Note: For a current mode driver the electrical time constant, L_M / R_M , of the motor does not enter into the small signal response. If a voltage mode drive scheme is used, then the asymptote, plotted as 2 above, can be approximated by:

$$\frac{N \cdot K_{\phi} \cdot K_{PD} \cdot K_T}{s^2 \cdot J \cdot R_M} \quad \text{if: } R_M > K_T \sqrt{\frac{L_M}{J}} \quad \text{and,} \quad \frac{K_T^2}{2\pi \cdot J \cdot R_M} < f < \frac{R_M}{2\pi \cdot L_M}$$

Here: K_{PD} = Voltage gain of Driver Stage

R_M = Motor Winding Resistance

L_M = Motor Winding Inductance

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9098701Q2A	OBSOLETE	TO/SOT	L	20		TBD	Call TI	Call TI
5962-9098701QEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1633J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC1633J883B	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2633N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
UC3633DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3633DWTR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI
UC3633N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Power Mgmt	power.ti.com
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