Three Phase Brushless Motor Pre-driver

BD63003MUV

General Description

BD63003MUV is a Pre-driver IC for 3-phase brushless motor. It generates a driving signal from the Hall sensor and applies PWM in the input control signal for motor control. It has a built-in booster circuit which allows Nch-Nch MOS transistors to be used as the external power Transistor. It is compatible with 12 V or 24 V power supply and has various controls and built-in protection functions, making it useful for variety of purposes. Since the IC adopts a small package, it can also be used on small diameter motors.

Key Specifications

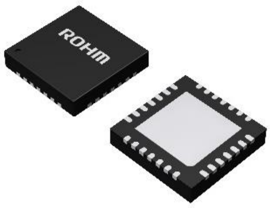
- Power Supply Voltage Rating: 40 V
- Low Side Gate Drive Voltage: 10 V (Typ)
- High Side Gate Drive Voltage: 10 V (Typ)
- Operating Temperature Range: -40 °C to +85 °C
- Current Limit Detect Voltage: 0.2 V±10 %
- UVLO Lockout Voltage: 6.0 V (Typ)
- OVLO Lockout Voltage: 28.5 V (Typ)

Package

Package	W (Typ) x D (Typ) x H (Max)
VQFN032V5050	5.0 mm x 5.0 mm x 1.0 mm

Features

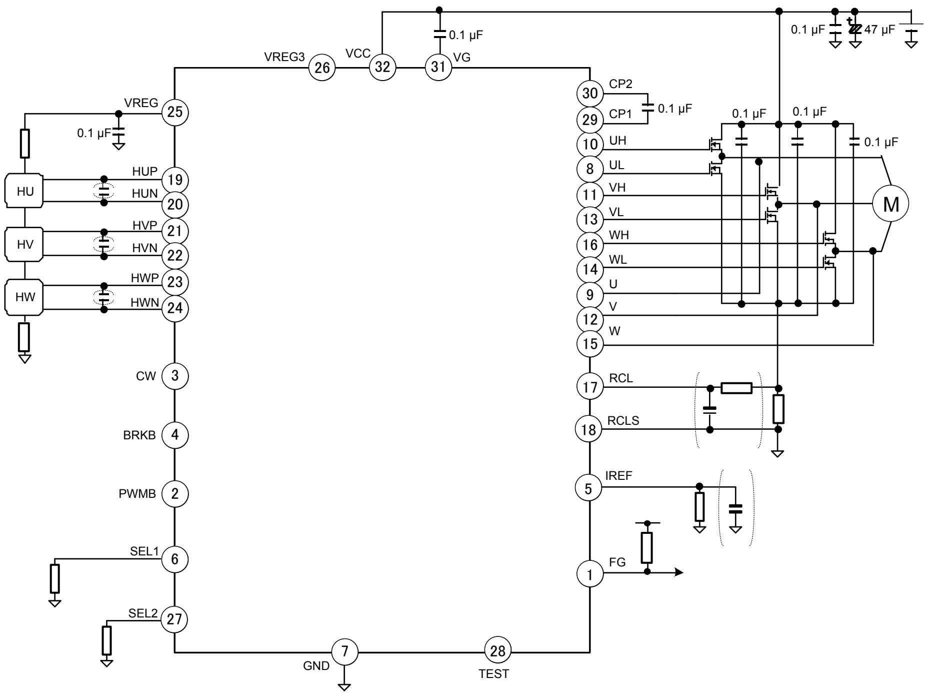
- Built in 120° Commutation Logic Circuit
- Driving with Nch-Nch MOS Transistors
- Built in Peak Current Control Function
- For Controller Input of 3.3 V and 5 V
- PWM Control Mode (lower arm switching)
- CW/CCW Function
- Short Brake Function
- FG Output (1FG / 3FG conversion)
- Built-in Protection Circuit for Current Limit (CL), Overheating (TSD), Under Voltage (UVLO), Over Voltage (OVLO), Motor Lock (MLP)



Applications

- OA Machines
- Other General Civil Equipment

Typical Application Circuit



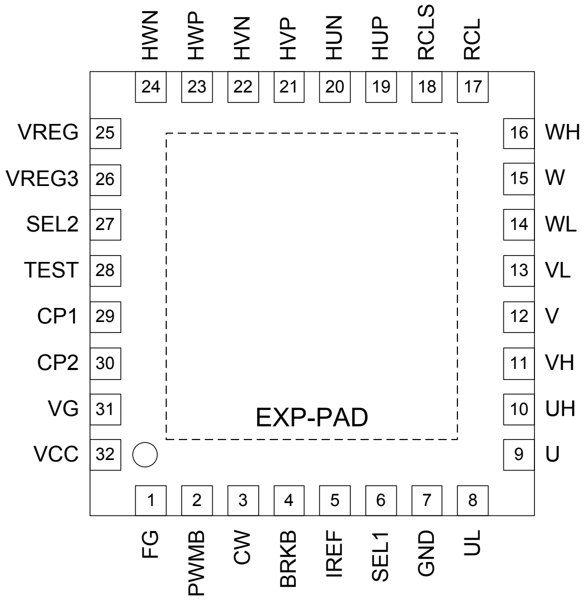
○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Contents

General Description 1
Features 1
Applications 1
Key Specifications 1
Package 1
Typical Application Circuit 1
Pin Configuration 3
Pin Descriptions 3
Block Diagram 4
Description of Blocks 5
Absolute Maximum Ratings 11
Thermal Resistance 11
Recommended Operating Conditions 11
Electrical Characteristics 12
Timing Chart 14
I/O Equivalence Circuits 15
Operational Notes 17
Ordering Information 19
Marking Diagram 19
Physical Dimension and Packing Information 20
Revision History 21

Pin Configuration

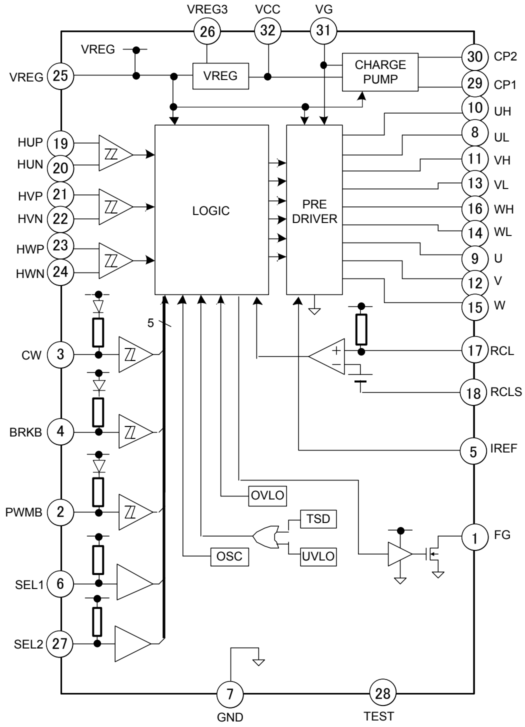
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	FG	1FG / 3FG output	17	RCL	Detect voltage input for over current
2	PWMB	PWM input (negative logic)	18	RCLS	RCL sense input
3	CW	Changing direction of rotation (H: CW, L: CCW)	19	HUP	U phase hall input +
4	BRKB	Brake input (negative logic)	20	HUN	U phase hall input -
5	IREF	Output driving current setting	21	HVP	V phase hall input +
6	SEL1	Function setting input 1	22	HVN	V phase hall input -
7	GND	GND	23	HWP	W phase hall input +
8	UL	U phase lower output	24	HWN	W phase hall input -
9	U	U phase output feedback	25	VREG	VREG output
10	UH	U phase upper output	26	VREG3	VREG3 output
11	VH	V phase upper output	27	SEL2	Function setting input 2
12	V	V phase output feedback	28	TEST	TEST input (GND)
13	VL	V phase lower output	29	CP1	Charge pump setting 1
14	WL	W phase lower output	30	CP2	Charge pump setting 2
15	W	W phase output feedback	31	VG	Charge pump output
16	WH	W phase upper output	32	VCC	Power supply
-	EXP-PAD	Connect EXP-PAD to GND			

Block Diagram



Description of Blocks

Commutation logic (120° commutation)

Truth Table

HU	HV	HW	CW (CW = H or OPEN)						FG	
			UH	UL	VH	VL	WH	WL	1FG	3FG
H	L	H	$\overline{\text{PWM}}$	PWM(Note 1)	H	L	L	L	L	Hi-z
H	L	L	$\overline{\text{PWM}}$	PWM(Note 1)	L	L	H	L	L	L
H	H	L	L	L	$\overline{\text{PWM}}$	PWM(Note 1)	H	L	L	Hi-z
L	H	L	H	L	$\overline{\text{PWM}}$	PWM(Note 1)	L	L	Hi-z	L
L	H	H	H	L	L	L	$\overline{\text{PWM}}$	PWM(Note 1)	Hi-z	Hi-z
L	L	H	L	L	H	L	$\overline{\text{PWM}}$	PWM(Note 1)	Hi-z	L
H	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	Hi-z	Hi-z

HU	HV	HW	CCW (CW = L)						FG	
			UH	UL	VH	VL	WH	WL	1FG	3FG
H	L	H	H	L	$\overline{\text{PWM}}$	PWM(Note 1)	L	L	L	Hi-z
H	L	L	H	L	L	L	$\overline{\text{PWM}}$	PWM(Note 1)	L	L
H	H	L	L	L	H	L	$\overline{\text{PWM}}$	PWM(Note 1)	L	Hi-z
L	H	L	$\overline{\text{PWM}}$	PWM(Note 1)	H	L	L	L	Hi-z	L
L	H	H	$\overline{\text{PWM}}$	PWM(Note 1)	L	L	H	L	Hi-z	Hi-z
L	L	H	L	L	$\overline{\text{PWM}}$	PWM(Note 1)	H	L	Hi-z	L
H	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	L	L	Hi-z	Hi-z

(*Note 1*) When PWM = "L", PWM = "H". When PWMB = H, PWMB = L.

1. Regulator Output Pin (VREG)
   This is constant voltage output pin of 5 V (Typ). Connect capacitors of 0.01 µF to 1 µF. Be careful that VREG current does not exceed absolute maximum ratings in case of being used for bias power supply of hall elements.

2. Regulator Output Pin (VREG3)
   This is constant voltage output pin of 3.3 V (Typ). VREG3 can be used for bias voltage of hall elements. Be careful that VREG3 current does not exceed absolute maximum ratings in case of being used.

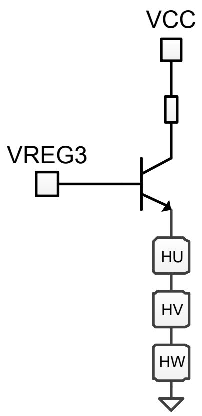
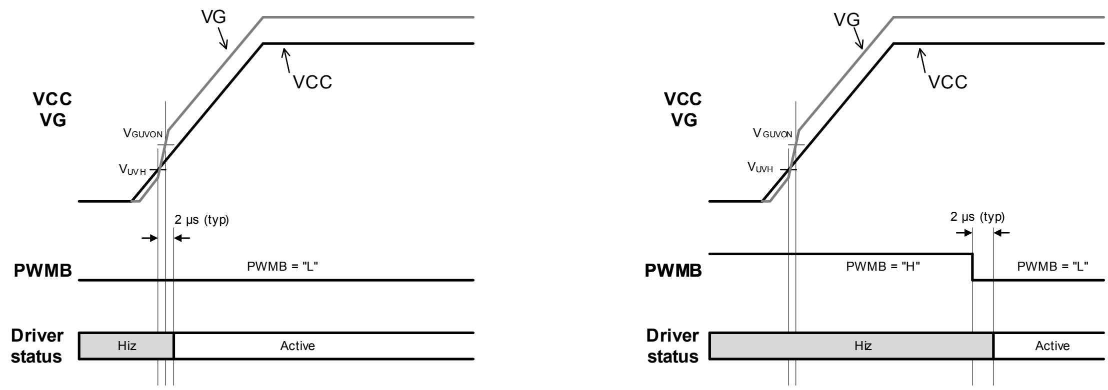


Figure 1. VREG3 reference circuit

Description of Blocks - continued

3. PWM Input Pin (PWMB)
Speed can be controlled by inputting PWM signal into the PWMB pin (negative logic). Synchronous rectifier PWM can be achieved through lower switching. When PWMB = "L", lower external FET that matches to Hall input logic is “L”. When PWMB = "H" or open, lower external FET is "H". When PWMB = "H" or OPEN status is detected for 104 μs (Typ), the synchronous rectifier is OFF. Synchronous rectifier turns ON through the falling edges of subsequent PWMB signals. At startup, External FET keeps “Hi-z” states in which all phase is OFF (stand-by) until PWMB = "L" status is detected 2 μs (Typ) or more [figure 2]. However, the internal regulator of VREG, VG, the other regulator, protection function of OVLO, and the other ones are operated in the stand-by. Additionally, the PWMB pin is pulled up by internal 3.3V (Typ) through a resistance of 100 kΩ ± 30 kΩ and pulled down by GND through a resistance of 1000 kΩ ± 300 kΩ.

PWMB	PWM phase Lower External FET
H or OPEN	OFF
L	ON



1. PWMB = "L" (VCC Rise Up)

2. PWMB = "H" (VCC Rise Up)

Figure 2. PWMB Status

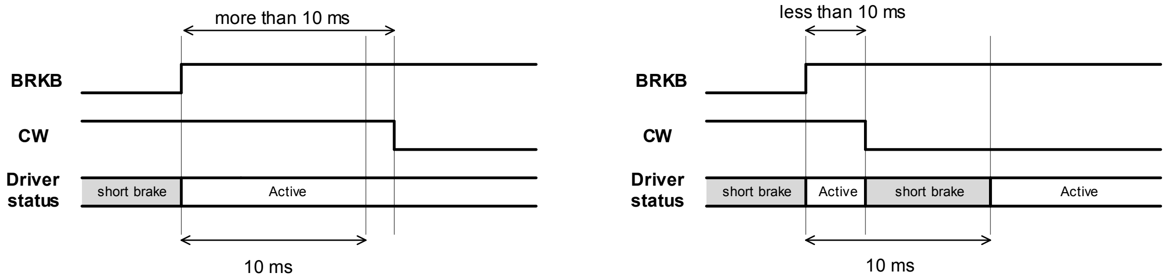
4. BRKB Pin (BRKB)
Motor rotation can be quickly stopped using the BRKB Pin (negative logic). When BRKB = "L", this causes all the upper external FET to turn "OFF" and all the lower external FET to turn "ON", initiating short break operation. When BRKB = "H" or OPEN, then short brake operation will be released. Additionally, the BRKB pin is pulled up by internal 3.3V (Typ) through a resistance of 100 kΩ ± 30 kΩ and pulled down by GND through a resistance of 1000 kΩ ± 300 kΩ.

BRKB	Operation
H or OPEN	Normal
L	Short brake

Description of Blocks - continued

5. Rotatory Direction Change Pin (CW)
   Rotation direction can be switched with the CW pin. When CW = "H" or OPEN, the direction is Clockwise (CW). When CW = "L", the direction will be Counter Clockwise (CCW). We do not recommend switching rotation direction when motor is rotating. If rotation direction is switched when rotating, the operation is the following due to the condition of SEL1.

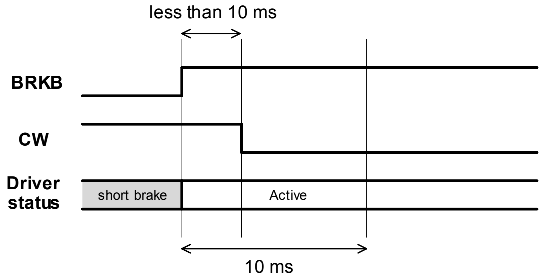
   (1) SBRK = "Enable" (SEL1 = "H" or "M1")
   After having performed short brakes movement until hall frequency becomes approximately 40 Hz (Typ) or less, rotatory direction is replaced. In the case of this condition, do not change the logic of CW for 10 ms after brakes cancellation by the BRKB input (Figure 3).



I. OK (SBRK = "Enable")   II. NG (SBRK = "Enable")

Figure 3. BRKB, CW Control Timing Limitation 1

   (2) SBRK = "Disable" (SEL1 = "M2" or "L")
   Without the short brake such as (1), direction is replaced. In this case, be careful since high current may sometimes flow in the external FET when the direction is replaced as described. In addition, there is no limitation in timing of BRKB and CW such as (1) in this condition (Figure 4).



III. OK (SBRK = "Disable")

Figure 4. BRKB, CW Control Timing Limitation 2

   In addition, the CW pin is pulled up by internal 3.3 V (Typ) through resistance of 100 kΩ ± 30 kΩ and pulled down by GND through a resistance of 1000 kΩ ± 300 kΩ.

CW	Direction
H or OPEN	CW
L	CCW

Description of Blocks - continued

6. Select Pin 1 (SEL1)
The SEL1 pin can be used to select 1FG / 3FG and “Enable” or “Disable” of the short brakes (SBRK) at the direction change with the CW pin. The SEL1 pin is a 4 input pin and can be set by being OPEN, 220 kΩ [± 5 %] to GND, 47 kΩ [± 5 %] to GND, and tied to GND. In addition, the SEL1 pin is pulled up by VREG through resistance of 100 kΩ ± 30 kΩ.

SEL1	FG	SBRK(CW/CCW)
H (OPEN)	3FG	Enable
M1 (220 kΩ [±5 %] to GND)	1FG	Enable
M2 (47 kΩ [±5 %] to GND)	1FG	Disable
L (tied to GND)	3FG	Disable

7. Select Pin 2 (SEL2)
The SEL2 pin can be used to select Enable/Disable of MLP and OVLO. In addition, the SEL2 pin is pulled up by VREG through resistance of 100 kΩ ± 30 kΩ.

SEL2	MLP	OVLO
H (OPEN)	2.2 s (Typ)	28.5 V (Typ)
M1 (220 kΩ [±5 %] to GND)	Disable	28.5 V (Typ)
M2 (47 kΩ [±5 %] to GND)	2.2 s (Typ)	Disable
L (tied to GND)	Disable	Disable

8. FG Output pin (FG)
FG signal is composed by a hall signal and is outputted by the FG pin. Changing between 1FG and 3FG can be done with SEL1. In addition, the FG pin, which is an open drain output, should be externally pulled-up by a resistance of the about 10 kΩ to 100 kΩ.

9. Hall Input (Hall: HUP, HUN, HVP, HVN, HWP, HWN)
Hall comparator inside the IC is designed with hysteresis (±15 mV (Typ)) in order to prevent malfunction due to noise. Always set correct bias current for the Hall element so that the amplitude of Hall input voltage will be the minimum input voltage ($V_{HALLMIN}$) or more. Furthermore, the output of the comparator has a digital filter of 2 µs (Typ). However, if it can’t prevent the noise, it is recommended to connect a ceramic capacitor with about 100 pF to 0.01 µF value between the input pins of the Hall comparator. The in-phase input voltage range (V_{HALLCM}: 0 V to V_{REG}-1.7 V (Typ)) is designed for Hall comparator, set within this range when applying bias to the Hall element. When all Hall inputs become "H" or "L", all external FETs will be "OFF" by the hall input abnormal detection circuit.

10. Booster Circuit
There is built-in booster circuit used to drive upper Nch MOS transistor. The VG pins can produce a boost voltage (the VCC voltage+10 V (Typ) through connecting capacitors between CP1 - CP2 and between VG - VCC. We recommend connected capacitors to be 0.1 µF or more. Because CP1 and CP2 are oscillated, the capacitors have to be located near IC. If need, add GND line for the shield. In addition, because VG voltage are boosted from the voltage that based on VCC, if VCC voltage is instability, it can be caused the malfunction such as VG voltage rise up. Therefore, add capacitor between VCC and GND as necessary to stabilize VCC voltage when using large current and motor with large BEMF. Because there is built-in protection circuit for insufficient booster, when VG voltage is V_{GUVON} (V_{CC}+7 V (Typ)) or less, all external FETs will be "OFF".

11. Current Limit Circuit (CL Circuit)
Output current limit (Current Limit: CL) circuit can be formed by connecting a low resistance used for detecting current between the RCL pin and the RCLS pin. When RCL voltage is detected 0.2 V (Typ) or more, all lower external FET will be "OFF". It returns by itself after a set amount of time (32 µs (Typ)). This operation does not synchronize with PWM signal input into the PWMB pin. In addition, in order to avoid misdetection of output current due to RCL noise, the IC sets up a noise-masking period (1 µs to 2 µs (Typ)). During the noise-masking period, current detection is disabled. RCLS is the sense line of RCL. If RCLS becomes OPEN, Current Limit may not be normally Function. Connect the RCLS pin to the GND nearest to the current sense resistor’s pin.

Description of Blocks - continued

12. Thermal Shutdown Circuit (TSD Circuit)
When chip temperature of driver IC rises and exceeds the set temperature (165 °C (Typ)), the thermal Shutdown circuit (Thermal Shutdown: TSD) begins working. At this time, all external FETs will be "OFF". In addition, the TSD circuit is designed with hysteresis (25 °C (Typ)), and will return to normal working condition when the chip temperature drops. Moreover, the purpose of the TSD circuit is to protect the driver IC from thermal breakdown, therefore, temperature of this circuit will be over working temperature when this circuit operates. Thus, thermal design should have sufficient margin, so do not take continuous use and operation of the circuit as precondition.

13. Under Voltage Lock Out Circuit (UVLO Circuit)
There is a built-in under voltage lockout circuit (Under Voltage Lockout: UVLO circuit) used to ensure the minimum power supply voltage for drive IC to work and to prevent error in the operation of IC. When VCC voltage declined to V_{UVL} (6 V (Typ)), all external FETs should be "OFF". At the same time, UVLO circuit is designed with hysteresis (1 V (Typ)), so when VCC voltage reaches V_{UVH} (7 V (Typ)) or more, it will enter normal operation.

14. Over Voltage Lock Out Circuit (OVLO Circuit)
There is built-in over voltage lockout circuit (Over Voltage Lockout: OVLO circuit) used to restrain the increase of VCC voltage when motor is decelerating. When VCC voltage is 28.5 V (Typ) or more, short brake action will be conducted. In order to avoid misdetection, the IC sets up a noise-masking period (2 μs to 3 μs (Typ)). The short brake operation is released after a certain period of time (4 ms) when the VCC voltage is less than or equal to 27.5 V (Typ) and returns to normal operation. OVLO function does not work in case of SEL2 = “Disable”

15. Motor Lock Protection Circuit (MLP Circuit)
There is built-in motor lock protection circuit (Motor Lock Protection: MLP), ON/OFF of MLP circuit can be set by the SEL2 pin. When the MLP setting of SEL2 = "Enable" and the Hall signal logic does not change for 2.2 s (Typ) or more, all external FETs will all be latched as "OFF". Latch can be released through switching BRKB/CW logic. Moreover, when PWMB = "H" or OPEN state is detected for about 15 ms (Typ), latch can be released by the falling edges of subsequent PWMB. However, the MLP circuit does not operate when the MLP setting of the SEL2 pin is "Disable" and when the short brake (including when switching the direction of rotation) or the TSD circuit is in operation.

16. Predriver Output
The drive signal generated by the internal logic outputs the drive signal to the external output power transistor. Driving voltage of upper gate is VG voltage (V_{CC}+10 V (Typ)) and driving voltage of lower gate is the internal REG voltage (10 V (Typ)). In addition, a dead time (0.2 μs (Typ)) is designed between the driving signals of upper gate and lower gate in order to prevent the upper and lower FET from being set to ON at the same time during synchronous rectifier PWM operation. Due to the influence of the motor’s counter electromotive force, the output feedback pin (U, V, W) might swing under GND potential, which can cause malfunctions or destruction. When negative potential exceeds -2 V (min), Schottky diode can be inserted to prevent malfunction or destruction.

17. Pre-driver Output Peak Current Setting Pin (IREF)
A current of the pre-driver output can be set by connecting a resistor between the IREF Pin and GND. Note that if the IREF pin is connected with GND or open, it may cause malfunction. The range of the resistance is 27 kΩ [±5 %] to 150 kΩ [±5 %]. About the approximate value of the output current, refer to the following table.

Resistor Value [kΩ]	Output Source Current [mA]	Output Sink Current [mA]
150	16	27
120	18	33
100	22	40
82	26	48
68	31	58
56	36	68
47	42	84
39	48	96
33	55	113
27	63	136

Figure 5. The reference value of Pre-driver output current

Description of Blocks - continued

18. Control Signal Sequence
    Though we recommend you to input control signals of the CW, PWMB, and BRKB pins after inputting VCC, there won't be any problem if done otherwise. However, if MLP = "Enable" is set at startup, the MLP circuit will not be able to start the motor if the rotation of the motor is not detected within the set time (the edge of the FG signal is not input). Moreover, the control signal and the IC internal signal are given priority. Refer to the table below.

Priority of Control Signal

Priority	Input / Internal signals
1st	UVLO
2nd	BRKB↑↓(Note 2), CW↑↓ (Note 2), PWMB↓ (Note 2)
3rd	TSD, MLP, HALLERR
4th	OVLO
5th	VG_UVLO, stand-by
6th	BRKB
7th	CL
8th	PWMB, CW,

(*Note 2*) ↑↓ means rising and falling edge of the signal.
Refer to a figure of in condition transition for the signal name.

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{CC}	-0.3 to +40.0	V
VG Voltage	V_{G}	-0.3 to +52.0	V
External FET Output Feedback Voltage	$V_{(U, V, W)}$	40	V
FG Voltage	V_{FG}	-0.3 to +7.0	V
RCL Voltage	V_{RCL}	-0.3 to +5.5	V
RCLS Voltage	V_{RCLS}	-0.3 to +0.3	V
Voltage of Input of Control and Hall Pins	$V_{I/O}$	-0.3 to +7.0	V
FG Output Current	I_{FG}	5	mA
VREG Output Current	I_{VREG}	-30	mA
VREG3 Output Current	I_{VREG3}	-5	mA
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 3)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 5)*	2s2p *(Note 6)*	
VQFN032V5050				
Junction to Ambient	θ_{JA}	138.9	39.1	°C/W
Junction to Top Characterization Parameter *(Note 4)*	Ψ_{JT}	11	5	°C/W

(Note 3) Based on JESD51-2A (Still-Air).
(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 5) Using a PCB board based on JESD51-3.
(Note 6) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(Note 7)*	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	Topr	-40	+25	+85	°C
Power Supply Voltage	V_{CC}	10.8	24.0	26.4	V

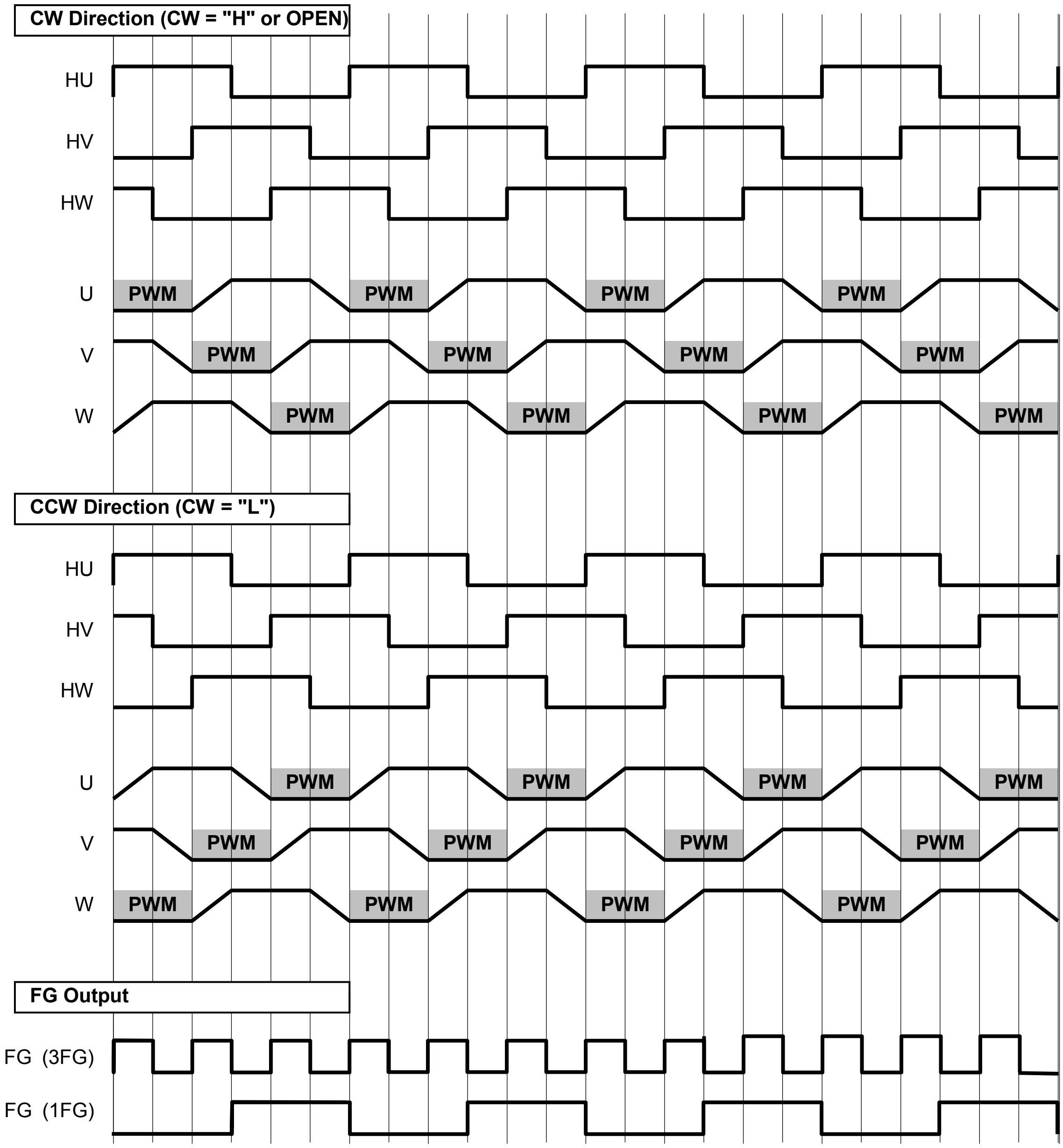
Electrical Characteristics (Unless otherwise specified V_{CC} = 24 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Whole						
Circuit Electric Current	I_{CC}	-	4.5	9	mA	
The VREG Voltage	V_{REG}	4.5	5.0	5.5	V	I_{VREG} = -10 mA
The VREG3 Voltage	V_{REG3}	3.0	3.3	3.6	V	I_{VREG3} = -1 mA
Booster Circuit						
VG Voltage	V_{G1}	V_{CC}+7	V_{CC}+10	V_{CC}+11.5	V	I_{VG} = 15 mA
VG UVLO Voltage	V_{GUVON}	V_{CC}+6	V_{CC}+7	V_{CC}+8	V	
Driver Output						
High Side V_{GS} Gate Drive Voltage	V_{GSH1}	7	10	11.5	V	
Low Side V_{GS} Gate Drive Voltage	V_{GSL1}	7	10	12.5	V	
Source Electric Current Setting Range	I_{RNG1}	-	-	70	mA	R_{IREF} = 27 kΩ
Sink Electric Current Setting Range	I_{RNG2}	-	-	140	mA	R_{IREF} = 27 kΩ
Output Peak Source Current	I_{OH}	-	18	-	mA	R_{IREF} = 120 kΩ
Output Peak Sink Current	I_{OL}	-	33	-	mA	R_{IREF} = 120 kΩ
IREF Voltage	V_{IREF}		1.2		V	
Hall Input						
Input Bias Current	I_{HALL}	-2.0	-0.1	+2.0	μA	V_{IN} = 0 V
Range of In-phase Input Voltage	V_{HALLCM}	0	-	V_{REG}-1.7	V	
Minimum Input Voltage	$V_{HALLMIN}$	50	-	-	mVp-p	
HYS Level +	$V_{HALLHY+}$	5	15	25	mV	
HYS Level -	$V_{HALLHY-}$	-25	-15	-5	mV	
Input of Control: PWMB, CW, BRKB						
Input Electric Current	I_{IN}	-46	-33	-20	μA	V_{IN} = 0 V
The Input H Voltage	V_{INH}	2.0	-	5.5	V	
The Input L Voltage	V_{INL}	0	-	0.8	V	
The Smallest Input Pulse Width	t_{PLSMIN}	1	-	-	ms	CW, BRKB
Input Frequency Range	f_{PWM}	10	-	50	kHz	PWMB
Input of Control: SEL1, SEL2						
Input Current	I_{SEL}	-80	-50	-30	μA	V_{SEL} = 0 V
FG Output						
Output Voltage L	V_{FGOL}	0	0.1	0.3	V	I_{FG} = 2 mA
Leak Current	I_{FGLEAK}	-	0	1	μ A	V_{FG} = 5 V
Current Limit						
The Detection Voltage	V_{CL}	0.18	0.20	0.22	V	
Input Bias Electric Current	I_{RCL}	-32	-20	-12	μA	V_{RCL} = 0V
Input Voltage Range	V_{RCL}	-0.3	-	+1.0	V	

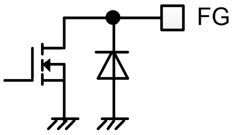
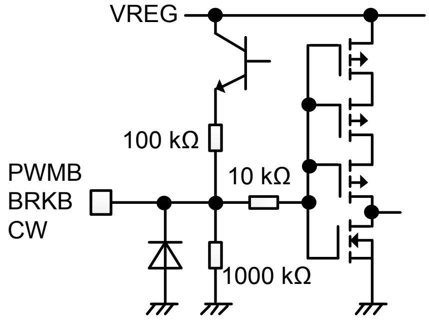
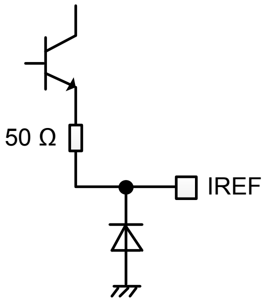
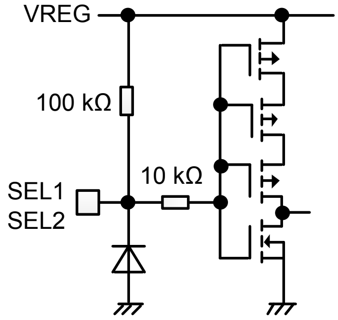
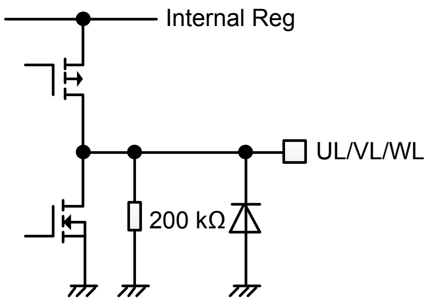
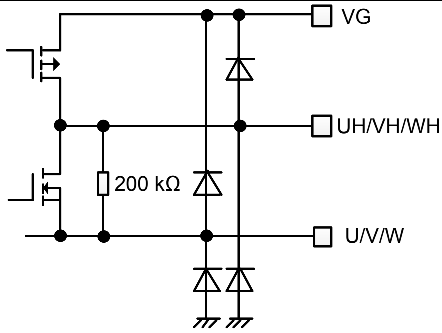
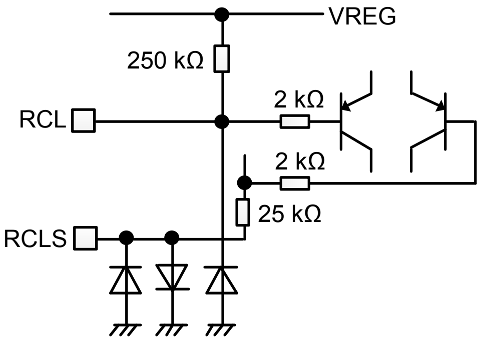
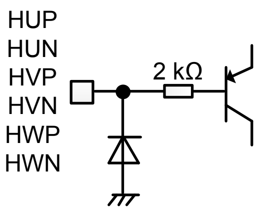
Electrical Characteristics - continued (Unless otherwise specified V_{CC} = 24 V, Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
UVLO						
Release Voltage	V_{UVH}	6.5	7.0	7.5	V	
Lockout Voltage	V_{UVL}	5.5	6.0	6.5	V	
OVLO						
Release Voltage	V_{OVL}	26.5	27.5	28.5	V	OVLO Enable
Lockout Voltage	V_{OVH}	27.5	28.5	29.5	V	OVLO Enable
MLP						
Motor Lock Protection Detect Time	t_{MLP}	1.54	2.20	2.86	s	MLP Enable

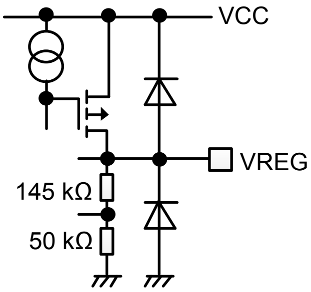
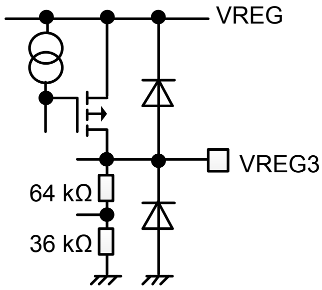
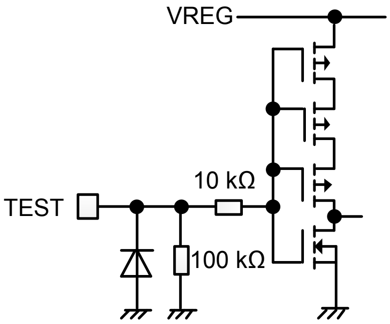
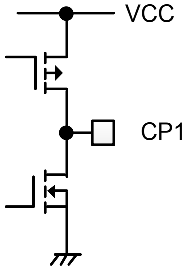
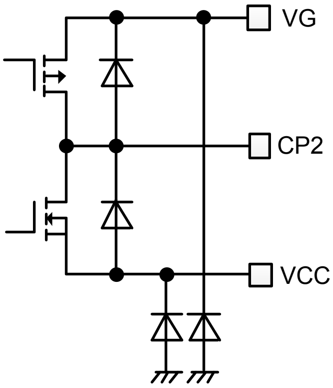
Timing Chart



I/O Equivalence Circuits

Pin No	Pin Name	Equivalence Circuit	Pin No	Pin Name	Equivalence Circuit
1	FG		2 3 4	PWM B CW BRKB	
5	IREF		6 27	SEL1 SEL2	
8 13 14	UL VL WL		9 10 11 12 15 16	U UH VH V W WH	
17 18	RCL RCLS		19 20 21 22 23 24	HUP HUN HVP HVN HWP HWN	

I/O Equivalence Circuits - continued

25	VREG		26	VREG3	
28	TEST		29	CP1	
30 31 32	CP2 VG VCC				

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

10. **Regarding the Input Pin of the IC**
    This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

    When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
    When GND > Pin B, the P-N junction operates as a parasitic transistor.

    Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

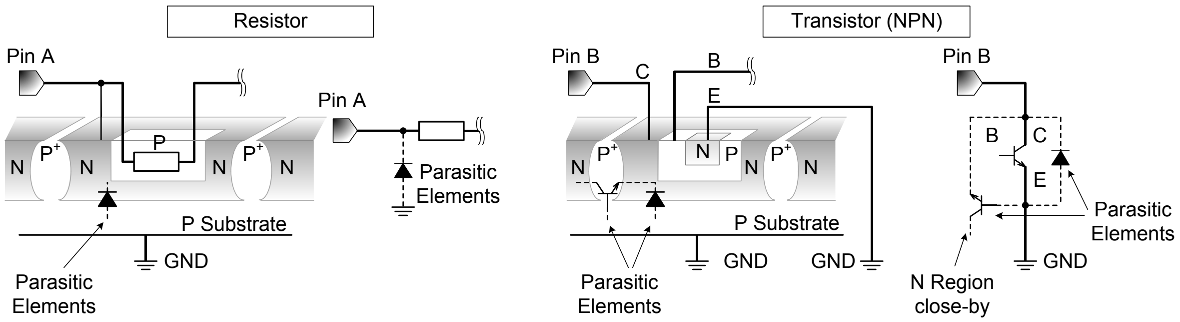


Figure 6. Example of Monolithic IC Structure

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. **Thermal Shutdown Circuit (TSD)**
    This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
    Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

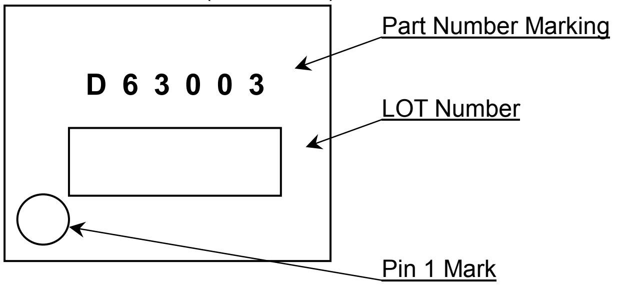
B	D	6	3	0	0	3	M	U	V	-	E 2

Package
MUV: VQFN032V5050

Packaging and forming specification
E2: Embossed tape and reel

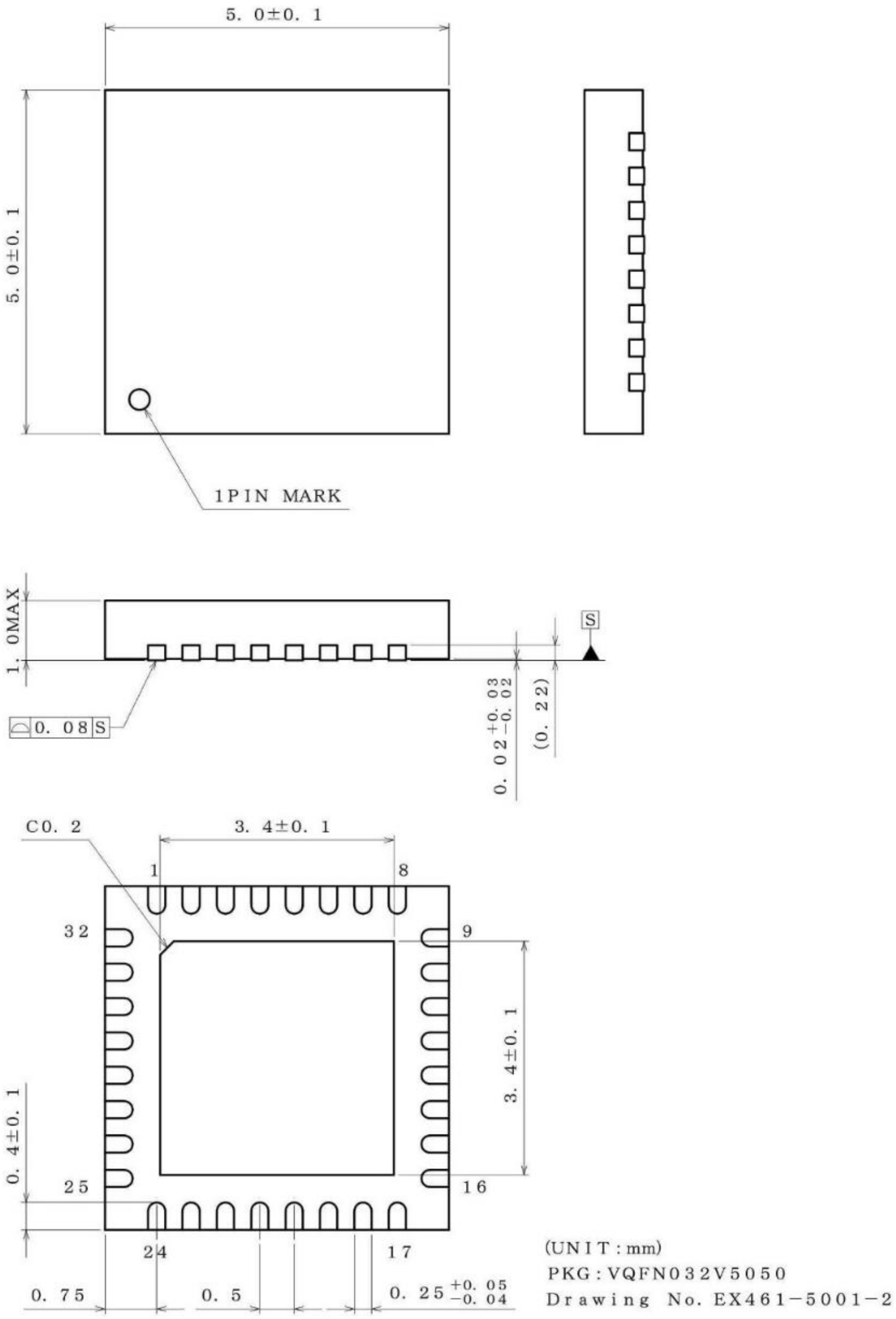
Marking Diagram

VQFN032V5050 (TOP VIEW)



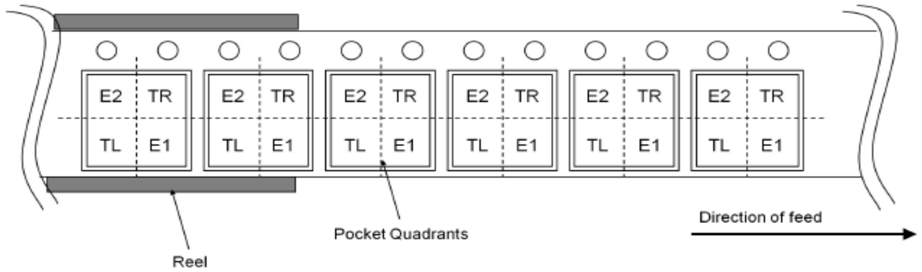
Physical Dimension and Packing Information

Package Name	VQFN032V5050



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
10.Jul.2020	001	New Release

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

3. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the Products or the information contained in this document. Provided, however, that ROHM will not assert its intellectual property rights or other rights against you or your customers to the extent necessary to manufacture or sell products containing the Products, subject to the terms and conditions herein.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.