

AFE7951 4T4R RF Sampling AFE with 12 GSPS DACs and 3 GSPS ADCs

1 Features

- [Request full data sheet](#)
- Quad RF sampling 12-GSPS transmit DACs
- Quad RF sampling 3-GSPS receive ADCs
- Maximum RF signal bandwidth: 400 MHz
- RF frequency range: 600 MHz - 12 GHz
- Digital step attenuators (DSA):
 - TX: 40 dB range, 0.125-dB steps
 - RX: 25 dB range, 0.5-dB steps
- Single or dual-band DUC or DDCs
- 16x NCOs per TX or RX
- Optional Internal PLL or VCO for DAC or ADC clocks or external clock at DAC or ADC sample rate
- SerDes data interface:
 - JESD204B and JESD204C compatible
 - 8 SerDes transceivers up to 29.5 Gbps
 - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- [Radar](#)
- [Seeker front end](#)
- [Defense radio](#)
- Tactical communications infrastructure
- [Wireless communications test](#)

3 Description

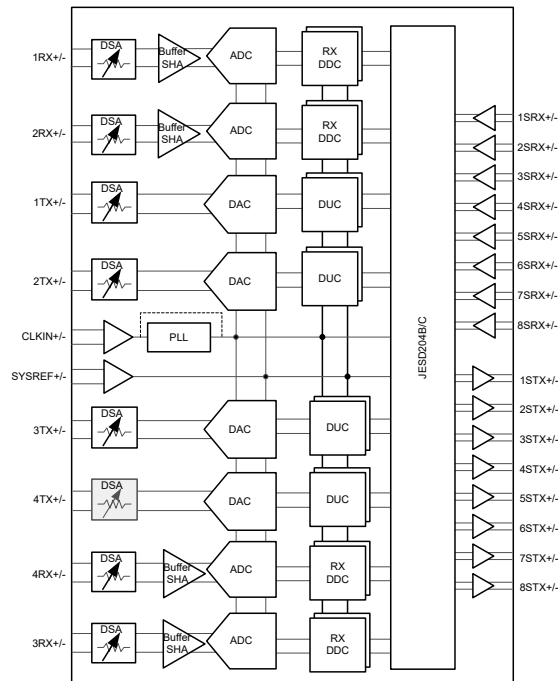
The AFE7951 is a high performance, wide bandwidth multi-channel transceiver, integrating four RF sampling transmitter chains and four RF sampling receiver chains. With operation up to 12 GHz, this device enables direct RF sampling in the L, S, C and X-band frequency ranges without the need for additional frequency conversions stages. This improvement in density and flexibility enables high-channel-count, multi-mission systems.

The TX signal paths support interpolation and digital up conversion options that deliver up to 400 MHz of signal bandwidth per TX channel. The output of the DUCs drives a 12-GSPS DAC (digital to analog converter) with a mixed mode output option to enhance 2nd Nyquist operation. The DAC output includes a variable gain amplifier (TX DSA) with 40-dB range and 1-dB analog and 0.125-dB digital steps.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
AFE7951	FC-BGA	17 mm × 17 mm

- (1) For more information, see *Mechanical, Packaging, and Orderable Information*.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable.



Functional Block Diagram



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4 Description (continued)

Each receiver chain includes a 25-dB range DSA (Digital Step Attenuator), followed by a 3-GSPS ADC (analog-to-digital converter). Each receiver channel has an analog peak power detector and various digital power detectors to assist an external or internal autonomous automatic gain controller, and RF overload detectors for device reliability protection. Flexible decimation options provide optimization of signal bandwidth of up to 400 MHz per RX channel.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2023	*	Initial Release

6 Pin Configuration and Functions

A	B	C	D	E	F	G	H	I	J	K	L	M	N	P	R	T	U	V	W	Y
20	VDD1P2 TXCLK	2TXOUT+	2TXOUT-	VDD1P2 TXCLK	VDD1P8TX	1TXOUT-	1TXOUT+	VDD1P8TX	VSSTX	VDD1P2 PLLCLK REF	VDD1P8 PLLVC0	VSSTX	VDD1P8TX	3TXOUT+	3TXOUT-	VDD1P8TX	VDD1P2 TXCLK	4TXOUT-	4TXOUT+	VDD1P2 TXCLK
19	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTX	VSSTX	PLL _DDOUT	SYSREF+	SYSREF-	VSSPLL	VSSTX	VSSTX	VSSTX	VSSTX	VSSTXCLK	VSSTX	VSSTX	VSSTXCLK
18	VSSFBCLK	VSSFBCLK	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSPLL CLKREF	VDD1P2 PLLCLK REF	VDD1P8 PLLCLK REF	VSSPLL CLKREF	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSTX	VSSFBCLK	VSSFBCLK
17	VDD1P8 FBCLK	VSSFB	VSSTX	VDD1P2 TXENC	VSSTXENC	VSSTX	VDD1P8 TXDAC	VDD1P8 TXDAC	VSS PLLXCM	REFCLK+	REFCLK-	VSS PLLXCM	VDD1P8 TXDAC	VDD1P8 TXDAC	VSSTX	VSSTXENC	VDD1P2 TXENC	VSSTX	VSSFB	VDD1P8 FBCLK
16	NC	VSSFB	VDD1P8FB	VDD1P2FB	VSSTXENC	GTR_7 _SPIB2SEN	GTR_17 _SPIB1SEN	GTR_14 _SPIB1SEN	VSSPLL FBCLK	VDD1P8PLL	VDD1P8PLL	VSSPLL FBCLK	GTL_7 _ALARM1	GTL_15 _GPIO3	GTL_18 _SPIASDO	VSSTXENC	VDD1P2FB	VDD1P8FB	VSSFB	NC
15	NC	VSSFB	VDD1P8FB	VDD1P2FB	VDD1P2FB	GTR_15 _RESETZ	GTR_13 _TRST	GTR_3 _TXDD1	GTR_9 _SPIB2SDO	VDD1P2 PLLXCM	VDD1P2 PLLXCM	GTL_3 _AUX0	GTL_2 _ALARM2	GTL_4 _SPIACLK	GTL_6 _RXTDD2	VDD1P2FB	VDD1P2FB	VDD1P8FB	VSSFB	NC
14	VDD1P8 FBCLK	VSSFB	VSSFB	VDD1P2FB	VDD1P2RX	GTR_5 _TDO	GTR_18 _TDI	GTR_4 _TCLK	GTR_2 _SPIB2CLK	GTR_8 _FBTDD1	GTL_8 _AUX1	GTL_9 _AUX2	GTL_17 _SPIASDIO	GTL_1 _SPEEP	GTL_5 _SPIASEN	VDD1P2RX	VDD1P2FB	VSSFB	VSSFB	VDD1P8 FBCLK
13	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_0 _RXG5WAP	GTR_6 _SPIB2 _SDIO	GND_ESD	DVDD0P9	DVDD0P9	GND_ESD	GTL_0 _GPIO2	GTL_11 _AUX3	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	VDD1P2RX
12	1RXIN+	VSSRX	VSSRX	VSSRX	VDD1P2RX	VDD1P2RX	GTR_11 _SPIB1 _SDO	GTR_1 _GPIO1	DGND	DVDD0P9	DVDD0P9	DGND	GTL_13 _AUX4	GTL_12 _BIST1	VDD1P2RX	VDD1P2RX	VSSRX	VSSRX	VSSRX	3RXIN+
11	1RXIN-	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P2RX	VDD1P2RX	GTR_10 _TMS	GTR_12 _SPIB1 _SDIO	DGND	DVDD0P9	DVDD0P9	DGND	GTL_14 _AUX5	GTL_10 _BIST0	VDD1P2RX	VDD1P2RX	VDD1P8RX	VDD1P8RX	VSSRX	3RXIN-
10	VDD1P2RX	VSSRX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_6 _RXBLNB	GBR_5 _FSPIDB	DGND	DVDD0P9	DVDD0P9	DGND	GBL_9 _GPIO15	GBL_6 _GPIO16	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRX	VDD1P2RX
9	VDD1P8 RXCLK	VSSRXCLK	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	GBR_9 _SYNCB _OUT0-	GBR_7 _SYNCB _OUT0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_7 _SYNCB _OUT1+	GBL_3 _SYNCB _OUT1-	VDD1P8RX	VDD1P8RX	VDD1P8RX	VDD1P8RX	VSSRXCLK	VDD1P8 RXCLK
8	2RXIN-	VSSRX	VSSRXCLK	GND_ESD	GBR_10 _FSPICLKA	VDD1P8RX	GBR_13 _GPIO8	GBR_8 _SYNCB _IN0+	DGND	DVDD0P9	DVDD0P9	DGND	GBL_9 _SYNCB _IN1+	GBL_13 _GPIO19	VDD1P8RX	GBL_10 _GPIO17	GND_ESD	VSSRXCLK	VSSRX	4RXIN-
7	2RXIN+	VSSRX	VSSRXCLK	GND_ESD	GBR_11 _RXTDD1	GBR_14 _FSPIDA	GBR_12 _GPIO7	GBR_17 _SYNCB _IN0-	DGND	DVDD0P9	DVDD0P9	DGND	GBL_17 _SYNCB _IN1-	GBL_12 _FSPICLKD	GBL_14 _FSPID0	GBL_11 _GPIO18	GND_ESD	VSSRXCLK	VSSRX	4RXIN+
6	VDD1P8 RXCLK	VSSRXCLK	GBR_0 _GPIO4	GBR_19 _GPIO12	GBR_16 _GPIO10	GBR_1 _GPIO5	GBR_15 _GPIO9	VDD1P8 GPIO	DGND	DVDD0P9	DVDD0P9	DGND	VDD1P8 GPIO	GBL_15 _FSPIDC	GBL_1 _FBTDD2	GBL_16 _RXCLNB	GBL_19 _GPIO20	GBL_9 _GPIO13	VSSRXCLK	VDD1P8 RXCLK
5	VSSRXCLK	VSSRXCLK	GBR_18 _GPIO11	GBR_2 _RXALNB	GBR_4 _GPIO6	GBR_3 _FSPICLKB	IFORCE	VSSGPIO	DGND	DVDD0P9	DVDD0P9	DGND	VSSGPIO	SENSE	GBL_3 _GPIO14	GBL_4 _RXCLNB	GBL_2 _FSPICLKC	GBL_18 _TXTDD2	VSSRXCLK	VSSRXCLK
4	VSSST	VSSST	1STX+	VDDTOP9	2STX+	VDDA1P8	3STX-	VDDA1P8	4STX-	VSSST	VSSST	5STX-	VDDA1P8	6STX-	VDDA1P8	7STX+	VDDTOP9	8STX+	VSSST	VSSST
3	1SRX+	VSSST	1STX-	VDDTOP9	2STX-	VDDA1P8	3STX+	VDDA1P8	4STX+	SERDES _AMUX1	SERDES _AMUX2	5STX+	VDDA1P8	6STX+	VDDA1P8	7STX-	VDDTOP9	8STX-	VSSST	8SRX+
2	1SRX-	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	DVDD0P9	DVDD0P9	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	VSSST	8SRX-
1	VSSST	2SRX+	2SRX-	VSSST	3SRX+	3SRX-	VSSST	4SRX+	4SRX-	VSSST	VSSST	5SRX-	5SRX+	VSSST	6SRX-	6SRX+	VSSST	7SRX-	7SRX+	VSSST

Figure 6-1. FCBGA Package, 400-Pin (Top View)

Table 6-1. Pin Functions

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
RF INTERFACES			
RXNC	A15, A16, Y15, Y16	I	Do not connect.
1RXIN-	A11	I	Receiver Channel 1 RF input: negative terminal. Unused RX inputs can be left open.
1RXIN+	A12	I	Receiver Channel 1 RF input: positive terminal. Unused RX inputs can be left open.
2RXIN-	A8	I	Receiver Channel 2 RF input: negative terminal. Unused RX inputs can be left open.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
2RXIN+	A7	I	Receiver Channel 2 RF input: positive terminal. Unused RX inputs can be left open.
3RXIN–	Y11	I	Receiver Channel 3 RF input: negative terminal.
3RXIN+	Y12	I	Receiver Channel 3 RF input: positive terminal. Unused RX inputs can be left open.
4RXIN–	Y8	I	Receiver Channel 4 RF input: negative terminal. Unused RX inputs can be left open.
4RXIN+	Y7	I	Receiver Channel 4 RF input: positive terminal. Unused RX inputs can be left open.
1TXOUT–	F20	O	Transmitter Channel 1 RF output: negative terminal. Connect to 1.8 V when not used.
1TXOUT+	G20	O	Transmitter Channel 1 RF output: positive terminal. Connect to 1.8 V when not used.
2TXOUT–	C20	O	Transmitter Channel 2 RF output: negative terminal. Connect to 1.8 V when not used.
2TXOUT+	B20	O	Transmitter Channel 2 RF output: positive terminal. Connect to 1.8 V when not used.
3TXOUT–	R20	O	Transmitter Channel 3 RF output: negative terminal. Connect to 1.8 V when not used.
3TXOUT+	P20	O	Transmitter Channel 3 RF output: positive terminal. Connect to 1.8 V when not used.
4TXOUT–	V20	O	Transmitter Channel 4 RF output: negative terminal. Connect to 1.8 V when not used.
4TXOUT+	W20	O	Transmitter Channel 4 RF output: positive terminal. Connect to 1.8 V when not used.
DIFFERENTIAL CLOCKS INPUTS			
REFCLK–	L17	I	Reference Clock Inputs: negative terminal
REFCLK+	K17	I	Reference Clock Inputs: positive terminal
SYSREF–	L19	I	SYSREEF inputs: negative terminals
SYSREF+	K19	I	SYSREEF inputs: positive terminals
SerDes CML INTERFACE			
1SRX–	A2	I	CML SerDes Interface Lane 1 input: negative terminal. Unused Serdes inputs can be left open.
1SRX+	A3	I	CML SerDes Interface Lane 1 input: positive terminal. Unused Serdes inputs can be left open.
2SRX–	C1	I	CML SerDes Interface Lane 2 input: negative terminal. Unused Serdes inputs can be left open.
2SRX+	B1	I	CML SerDes Interface Lane 2 input: positive terminal. Unused Serdes inputs can be left open.
3SRX–	F1	I	CML SerDes Interface Lane 3 input: negative terminal
3SRX+	E1	I	CML SerDes Interface Lane 3 input: positive terminal. Unused Serdes inputs can be left open.
4SRX–	J1	I	CML SerDes Interface Lane 4 input: negative terminal
4SRX+	H1	I	CML SerDes Interface Lane 4 input: positive terminal
5SRX–	M1	I	CML SerDes Interface Lane 5 input: negative terminal. Unused Serdes inputs can be left open.
5SRX+	N1	I	CML SerDes Interface Lane 5 input: positive terminal
6SRX–	R1	I	CML SerDes Interface Lane 6 input: negative terminal
6SRX+	T1	I	CML SerDes Interface Lane 6 input: positive terminal. Unused Serdes inputs can be left open.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
7SRX–	V1	I	CML SerDes Interface Lane 7 input: negative terminal
7SRX+	W1	I	CML SerDes Interface Lane 7 input: positive terminal. Unused Serdes inputs can be left open.
8SRX–	Y2	I	CML SerDes Interface Lane 8 input: negative terminal
8SRX+	Y3	I	CML SerDes Interface Lane 8 input: positive terminal. Unused Serdes inputs can be left open.
1STX–	C3	O	CML SerDes Interface Lane 1 output: negative terminal. Unused Serdes outputs can be left open.
1STX+	C4	O	CML SerDes Interface Lane 1 output: positive terminal. Unused Serdes outputs can be left open.
2STX–	E3	O	CML SerDes Interface Lane 2 output: negative terminal. Unused Serdes outputs can be left open.
2STX+	E4	O	CML SerDes Interface Lane 2 output: positive terminal. Unused Serdes outputs can be left open.
3STX–	G4	O	CML SerDes Interface Lane 3 output: negative terminal. Unused Serdes outputs can be left open.
3STX+	G3	O	CML SerDes Interface Lane 3 output: positive terminal. Unused Serdes outputs can be left open.
4STX–	J4	O	CML SerDes Interface Lane 4 output: negative terminal. Unused Serdes outputs can be left open.
4STX+	J3	O	CML SerDes Interface Lane 4 output: positive terminal. Unused Serdes outputs can be left open.
5STX–	M4	O	CML SerDes Interface Lane 5 output: negative terminal. Unused Serdes outputs can be left open.
5STX+	M3	O	CML SerDes Interface Lane 5 output: positive terminal. Unused Serdes outputs can be left open.
6STX–	P4	O	CML SerDes Interface Lane 6 output: negative terminal. Unused Serdes outputs can be left open.
6STX+	P3	O	CML SerDes Interface Lane 6 output: positive terminal. Unused Serdes outputs can be left open.
7STX–	T3	O	CML SerDes Interface Lane 7 output: negative terminal. Unused Serdes outputs can be left open.
7STX+	T4	O	CML SerDes Interface Lane 7 output: positive terminal. Unused Serdes outputs can be left open.
8STX–	V3	O	CML SerDes Interface Lane 8 output: negative terminal. Unused Serdes outputs can be left open.
8STX+	V4	O	CML SerDes Interface Lane 8 output: positive terminal. Unused Serdes outputs can be left open.
GPIO FUNCTIONS			
GBL_0_GPIO13	V6	I/O	GPIO.
GBL_1_FBTDD2	R6	I/O	Default location of FB TDD2 input signal.
GBL_2_FSPICLK	U5	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_3_GPIO14	R5	I/O	GPIO.
GBL_4_RXDLNB	T5	I/O	Default location of RX channel D AGC LNA Bypass output signal.
GBL_5_GPIO15	N10	I/O	GPIO.
GBL_6_GPIO16	P10	I/O	GPIO.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
GBL_7_SYNCB_OUT1+	N9	I/O	Default location of JESD Sync\ 1 output differential positive terminal.
GBL_8_SYNCB_IN1+	N8	I/O	Default location of JESD Sync\ 1 input differential positive terminal.
GBL_9_SYNCB_OUT1–	P9	I/O	Default location of JESD Sync\ 1 output differential negative terminal.
GBL_10_GPIO17	T8	I/O	GPIO.
GBL_11_GPIO18	T7	I/O	GPIO.
GBL_12_FSPICLKD	P7	I/O	Default and recommended location of FSPI D clock (FSPI for factory use only, available as generic GPIO).
GBL_13_GPIO19	P8	I/O	GPIO.
GBL_14_FSPIDD	R7	I/O	Default and recommended location of FSPI D data (FSPI for factory use only, available as generic GPIO).
GBL_15_FSPIDC	P6	I/O	Default and recommended location of FSPI C clock (FSPI for factory use only, available as generic GPIO).
GBL_16_RXCLNB	T6	I/O	Default location of RX channel C AGC LNA Bypass output signal.
GBL_17_SYNCB_IN1–	N7	I/O	Default location of JESD Sync\ 1 input differential negative terminal.
GBL_18_TXTDD2	V5	I/O	Default location of TX TDD2 input signal.
GBL_19_GPIO20	U6	I/O	GPIO.
GBR_0_GPIO4	C6	I/O	GPIO.
GBR_1_GPIO5	F6	I/O	GPIO.
GBR_2_RXALNB	D5	I/O	Default location of RX channel A AGC LNA Bypass output signal.
GBR_3_FSPICLKB	F5	I/O	Default and recommended location of FSPI B clock (FSPI for factory use only, available as generic GPIO).
GBR_4_GPIO6	E5	I/O	GPIO.
GBR_5_FSPIDB	H10	I/O	Default and recommended location of FSPI B data (FSPI for factory use only, available as generic GPIO).
GBR_6_RXBLNB	G10	I/O	Default location of RX channel B AGC LNA Bypass output signal.
GBR_7_SYNCB_OUT0+	H9	I/O	Default location of JESD Sync\ 0 output differential positive terminal.
GBR_8_SYNCB_IN0+	H8	I/O	Default location of JESD Sync\ 0 input differential positive terminal.
GBR_9_SYNCB_OUT0–	G9	I/O	Default location of JESD Sync\ 0 output differential negative terminal.
GBR_10_FSPICLKA	E8	I/O	Default location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_11_RXTDD1	E7	I/O	Default location of RX TDD1 input signal.
GBR_12_GPIO7	G7	I/O	GPIO.
GBR_13_GPIO8	G8	I/O	GPIO.
GBR_14_FSPIDA	F7	I/O	Default and recommended location of FSPI A clock (FSPI for factory use only, available as generic GPIO).
GBR_15_GPIO9	G6	I/O	GPIO.
GBR_16_GPIO10	E6	I/O	GPIO.
GBR_17_SYNCB_IN0–	H7	I/O	Default location of JESD Sync\ 0 input differential negative terminal.
GBR_18_GPIO11	C5	I/O	GPIO.
GBR_19_GPIO12	D6	I/O	GPIO.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
GTL_0_GPIO2	N13	I/O	GPIO.
GTL_1_SLEEP	P14	I/O	Default location of Sleep input signal.
GTL_2_ALARM2	N15	I/O	Default location of Alarm 2 output signal.
GTL_3_AUX0	M15	I/O	GPIO or auxiliary low-speed ADC input 0
GTL_4_SPIACLK	P15	I/O	Fixed Location of SPI A Clock.
GTL_5_SPIASEN	R14	I/O	Fixed Location of SPI A Send Enable.
GTL_6_RXTDD2	R15	I/O	Default location of RX TDD2 input signal.
GTL_7_ALARM1	N16	I/O	Default location of Alarm 1 output signal.
GTL_8_AUX1	L14	I/O	GPIO or auxiliary low-speed ADC input 1.
GTL_9_AUX2	M14	I/O	GPIO or auxiliary low-speed ADC input 2.
GTL_10_BIST0	P11	I/O	Fixed Location for BIST0 Function. Set low when using JTAG, set high for normal operation.
GTL_11_AUX3	P13	I/O	GPIO or auxiliary low-speed ADC input 3.
GTL_12_BIST1	P12	I/O	Fixed Location for BIST1 Function. Set high when using JTAG, set low for normal operation.
GTL_13_AUX4	N12	I/O	GPIO or auxiliary low-speed ADC input 4.
GTL_14_AUX5	N11	I/O	GPIO or auxiliary low-speed ADC input 5.
GTL_15_GPIO3	P16	I/O	GPIO.
GTL_17_SPIASDIO	N14	I/O	Fixed Location of SPI A Serial Data Input (3- and 4-wire mode) or Output (3 wire mode only).
GTL_18_SPIASDO	R16	I/O	Fixed Location of SPI A Serial Data Output in 4-wire mode.
GTR_0_RXGSWAP	G13	I/O	Default location of RX gain swap input.
GTR_1_GPIO1	H12	I/O	GPIO.
GTR_2_SPIB2CLK	J14	I/O	Default and recommended location of SPI B2 clock.
GTR_3_TXTDD1	H15	I/O	Default location of TX TDD1 input signal.
GTR_4_TCLK	H14	I/O	Fixed location for JTAG Test Clock.
GTR_5_TDO	F14	I/O	Fixed location for JTAG Test Data Out.
GTR_6_SPIB2_SDIO	H13	I/O	Default and recommended location of SPI B2 serial data input/output.
GTR_7_SPIB2SEN	F16	I/O	Default and recommended location of SPI B2 enable input.
GTR_8_FBTDD1	K14	I/O	Default location of FB TDD1 input signal.
GTR_9_SPIB2SDO	J15	I/O	Default and recommended location of SPI B2 serial data output (4-wire mode)
GTR_10_TMS	G11	I/O	Fixed location for JTAG Test Mode Select.
GTR_11_SPIB1_SDO	G12	I/O	Default and recommended location of SPI B1 serial data output (4-wire mode).
GTR_12_SPIB_SDIO	H11	I/O	Default and recommended location of SPI B1 serial data input/output.
GTR_13_TRST	G15	I/O	Fixed location for JTAG Test Reset. Must be pulled low when the JTAG port is not used.
GTR_14_SPIB1SEN	H16	I/O	Default and recommended location of SPI B1 enable input.
GTR_15_RESETZ	F15	I/O	Fixed Location for reset function. Chip Reset to default register settings.
GTR_17_SPIB1CLK	G16	I/O	Default and recommended location of SPI B1 clock.
GTR_18_TDI	G14	I/O	Fixed location for JTAG Test Data Input.
POWER SUPPLIES			
DVDD	K2, K5, K6, K7, K8, K9, K10, K11, K12, K13, L2, L5, L6, L7, L8, L9, L10, L11, L12, L13	—	0.9-V digital power supply

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
VDD1P2FB	D14, D15, D16, E15, U14, U15, U16, T15	—	1.2-V supply for FB ADCs.
VDD1P8FB	C15, C16, V15, V16	—	1.8-V supply for FB ADC.
VDD1P8FBCLK	A14, A17, Y17, Y14	—	1.8-V supply for FB ADC clock.
VDD1P2PLLCLKREF	K20, K18, L18	—	1.2-V supply for PLL.
VDDPLL1P2FBCML	L15	—	1.2-V supply for PLL clock distribution to FB ADC.
VDDPLL1P2RXCML	K15	—	1.2-V supply for clock distribution to RX ADC.
VDD1P8PLL	K16, L16	—	1.8-V supply for PLL.
VDD1P8PLLVCO	L20	—	1.8-V supply for PLL/VCO. This is a sensitive net and requires extra care in layout.
VDD1P2RX	A10, A13, E11, E12, E13, E14, F11, F12, F13, R11, R12, R13, T11, T12, T13, T14, Y10, Y13	—	1.2-V supply for RX ADCs.
VDD1P8RX	C9, C10, C11, D9, D10, D11, E9, E10, F8, F9, F10, R8, R9, R10, T9, T10, U9, U10, U11, V9, V10, V11	—	1.8-V supply for RX ADCs.
VDD1P8RXCLK	A6, A9, Y6, Y9	—	1.8-V supply for RX ADC clocks.
VDD1P2TXENC	D17, U17	—	1.2-V supply for DAC encoder.
VDD1P2TXCLK	A20, D20, U20, Y20	—	1.2-V supply for DAC clock.
VDD1P8TX	E20, H20, N20, T20	—	1.8-V supply for DAC.
VDD1P8TXDAC	G17, H17, N17, P17	—	1.8-V supply for DAC.
VDD1P8GPIO	H6, N6	—	1.8-V supply for GPIO.
VDDA1P8	F3, F4, H3, H4, R3, R4, N3, N4	—	SerDes analog 1.8-V power supply.
VDDT0P9	D3, D4, U3, U4	—	SerDes digital 0.9-V power supply.
GROUND			
DGND	J5, J6, J7, J8, J9, J10, J11, J12, M5, M6, M7, M8, M9, M10, M11, M12	—	Digital core ground
VSSGPIO	H5, N5	—	GPIO ground.
VSSFB	B14, B15, B16, B17, C14, V14, W14, W15, W16, W17	—	Ground for FB ADC supply.
VSSFBCLK	A18, B18, W18, Y18	—	Ground for FB ADC 1.8-V clock supply.
GND_ESD	D7, D8, J13, M13, U7, U8	—	Ground for ESD protection circuits.
VSSRX	B7, B8, B10, B11, B12, C12, D12, B13, C13, D13, W7, W8, W10, W11, W13, U12, V12, W12, U13, V13	—	Ground for RX ADC.
VSSRXCLK	A5, B5, B6, B9, C7, C8, W5, W6, W9, Y5, V7, V8	—	Ground for RX ADC clocks.
VSSTX	B19, C17, C18, C19, D18, E18, E19, F17, F18, F19, G18, G19, H18, H19, J20, M20, N18, N19, P18, P19, R17, R18, R19, T18, T19, U18, V17, V18, V19, W19	—	Ground for TX DAC.
VSSTXENC	E16, E17, T16, T17	—	Ground for TX DAC encoder.
VSSTXCLK	A19, D19, U19, Y19	—	Ground for TX DAC clock.
VSSPLL	M19	—	Ground for PLL.
VSSPLLFBCML	J16, M16	—	Ground for FB ADC clock.

Table 6-1. Pin Functions (continued)

BALL NAME	BALL NUMBER	TYPE ⁽¹⁾	DESCRIPTION
VSSPLLCLKREF	J18, M18	—	Ground for CLKREF PLL.
VSSPLLRCML	J17, M17	—	Ground for RX ADC clock.
VSST	A1, A4, B2, B3, B4, C2, D1, D2, E2, F2, G1, G2, H2, J2, K1, K4, L1, L4, M2, N2, P1, P2, R2, T2, U1, U2, V2, W2, W3, W4, Y1, Y4	—	SerDes ground.
OTHERS			
IFORCE	G5	—	Reserved for TI use only. Do not connect.
PLL_LDOUT	J19	—	External decoupling ball for PLL LDO. Connect with 100-nF capacitor to GND.
SerDes_AMUX1	K3	—	Analog test pin for SerDes lane 1-4, can be left floating
SerDes_AMUX2	L3	—	Analog test pin for SerDes lane 5-8, can be left floating
VSENSE	P5	—	Process test: sense voltage (TI use only). Do not connect.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Supply Voltage Range	DVDD0P9, VDDT0P9	−0.3	1.2	V
	VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML	−0.3	1.4	V
	VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVC0, VDD1P8FB, VDD1P8FBCML, VDD1P8GPIO, VDDA1P8	−0.5	2.1	V
Pin Volatge Range	{1/2/3/4}RXIN+/-	−0.5	VDDR1P8+0.3	V
	{1/2/3/4}TXOUT+/-	−0.5	VDDTX1P8+0.3	V
	REFCLK+/-, SYSREF+/-	−0.3	1.4	V
	{1:8}SRX+/-	−0.3	1.4	V
	{1:8}STX+/-	−0.3	1.4	V
	GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESET, BISTB0, BISTB1	−0.5	VDD1P8GPIO + 0.3	V
	IFORCE, VSENSE	−0.3	VDDCLK1P8 + 0.3	V
	SRDAMUX1, SRDAMUX2	−0.3	VDDA1P8+0.3	V
Peak Input Current	any input		20	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins ⁽¹⁾	1000	V
		Charged device model (CDM), per ANSI/ESDA/ JEDEC JS-002, all pins	150	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DVDD0P9, VDDT0P9	Supply voltage 0.9V	0.9	0.925	0.95	V
VDD1P2{RX/TXCLK/TXENC/FB/PLL/ PLLCLKREF/FBCML/RXCML}	Supply voltage 1.2V	1.15	1.2	1.25	V
VDD1P8{RX/RXCLK/TX/TXDAC/ TXENC/PLL/PLLVCO/FB/FBCLK/ GPIO}, VDDA1P8	Supply voltage 1.8V	1.75	1.8	1.85	V
T _A	Ambient temperature	–40		85	°C
T _J	Operating Junction Temperature			110 ⁽¹⁾	°C
	Maximum Operating Junction Temperature	125			°C

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

7.4 Thermal Information AFE79xx

THERMAL METRIC ⁽¹⁾		17mmx17mm FC-BGA	UNIT
		400 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	16.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.42	°C/W
R _{θJB}	Junction-to-board thermal resistance	4.85	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	4.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Transmitter Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC _{RES}	DAC resolution			14		bits
f _{RFout}	RF output frequency range	f _{DAC} = 12 GSPS, 1 st Nyquist	600		6000	MHz
		f _{DAC} = 12 GSPS, 2 nd Nyquist	6000		12000	
		f _{DAC} = 9 GSPS, 1 st Nyquist	600		4500	
		f _{DAC} = 9 GSPS, 2 nd Nyquist	4500		9000	
		f _{DAC} = 6 GSPS, 1 st Nyquist	600		3000	
		f _{DAC} = 6 GSPS, 2 nd Nyquist	3000		6000	
P _{max_FS}	Max Full Scale Output Power, max gain 1 tone, at device pins	f _{out} = 850 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.2		dBm
		f _{out} = 1800 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS		4.6		dBm
		f _{out} = 2600 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS		4.0		dBm
		f _{out} = 3500 MHz, -0.5dBFS		3.9		dBm
		f _{out} = 4900 MHz, -0.5dBFS		3.1		dBm
		f _{out} = 3500 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		1.0		dBm
		f _{out} = 4900 MHz, f _{DAC} = 5898.24 MSPS, -0.5dBFS, straight mode		0.1		dBm
		f _{out} = 4900 MHz, f _{DAC} = 8847.36 MSPS, -0.5dBFS, straight mode		-0.7		dBm
		f _{out} = 8100 MHz, -0.1dBFS, mixed mode		-2.8		dBm
		f _{out} = 9600 MHz, -0.1dBFS, mixed mode		-4.3		dBm
R _{TERM}	Output termination resistor	Default setting		50		Ω
ATT _{range}	DSA Attenuation range			40		dB
ATT _{step}	DSA Analog Attenuation step			1.0		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, before calibration		±0.2		dB
	DSA Attenuation step accuracy (DNL)	0 < Atten < 40dB, after calibration		±0.1		dB
ATT _{phase-err}	DSA Gain Steps Phase accuracy, any 8dB range	f _{out} = 850MHz ⁽²⁾		±1		deg
		f _{out} = 1800MHz ⁽²⁾		±1		deg
		f _{out} = 2600MHz ⁽²⁾		±1		deg
		f _{out} = 3500MHz ⁽²⁾		±1		deg
		f _{out} = 4900MHz ⁽²⁾		±1		deg
		f _{out} = 8100MHz ⁽²⁾		±2		deg
		f _{out} = 9600MHz ⁽²⁾		±2		deg
G _{flat}	Gain flatness	any 20MHz		0.1		dB
		600MHz BW, F _{out} < 4.9G		1.2		

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IMD3	3rd Order Intermodulation distortion, 2 tones at $f_{\text{IF}} \pm 10\text{ MHz}$	$f_{\text{out}} = 850\text{MHz}$, -7dBFS each tone		-66		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -7dBFS each tone		-63		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -7dBFS each tone		-62		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -7dBFS each tone		-61		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -7dBFS each tone		-57		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -7dBFS each tone		-55		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -7dBFS each tone		-52		dBc
		$f_{\text{out}} = 850\text{MHz}$, -13dBFS each tone		-74.4		dBc
		$f_{\text{out}} = 1800\text{MHz}$, -13dBFS each tone		-71.1		dBc
		$f_{\text{out}} = 2600\text{MHz}$, -13dBFS each tone		-73		dBc
		$f_{\text{out}} = 3500\text{MHz}$, -13dBFS each tone		-72		dBc
		$f_{\text{out}} = 4900\text{MHz}$, -13dBFS each tone		-67.8		dBc
		$f_{\text{out}} = 8100\text{MHz}$, -13dBFS each tone		-64		dBc
		$f_{\text{out}} = 9600\text{MHz}$, -13dBFS each tone		-68		dBc
SFDR	Spurious Free Dynamic Range (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		50.8		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		51.9		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		42		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		44		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		46.1		dBc
$f_s/2 - f_{\text{OUT}}$	Interleaving Image	$f_{\text{DAC}} = 5898.24\text{MSPS}$, interleave mode		-51.9		dBc
		$f_{\text{DAC}} = 8847.36\text{ MSPS}$, interleave mode		-46.0		dBc
		$f_{\text{DAC}} = 11796.48\text{MSPS}$, interleave mode		-41		dBc
HD2	2nd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-49		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-48		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-47		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-50		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-53		dBc
		$f_{\text{out}} = 850\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 1800\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-64		dBc
		$f_{\text{out}} = 2600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-45		dBc
		$f_{\text{out}} = 3500\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-57		dBc
		$f_{\text{out}} = 4900\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-58		dBc
		$f_{\text{out}} = 8100\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-60		dBc
		$f_{\text{out}} = 9600\text{ MHz}$, $A_{\text{OUT}} = -12\text{dBFS}$		-62		dBc

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD3	3rd Harmonic Distortion (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-62		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-55		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-57		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-60		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-54		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-56		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-79		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-77		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-78		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-82		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-80		dBc
HDn, n >= 4	Harmonic Distortion n >= 4 (within Nyquist zone)	$f_{\text{out}} = 850\text{ MHz}$		-81		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		-88		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		-79		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		-86		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		-85		dBc
		$f_{\text{out}} = 850\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-93		dBc
		$f_{\text{out}} = 1800\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-98		dBc
		$f_{\text{out}} = 2600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-84		dBc
		$f_{\text{out}} = 3500\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 4900\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 8100\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
		$f_{\text{out}} = 9600\text{ MHz}, A_{\text{OUT}} = -12\text{dBFS}$		-87		dBc
SFDR +/- 250 MHz	Spurious Free Dynamic Range within +/- 250 MHz	$f_{\text{out}} = 850\text{ MHz}$		68.5		dBc
		$f_{\text{out}} = 1800\text{ MHz}$		79.4		dBc
		$f_{\text{out}} = 2600\text{ MHz}$		77		dBc
		$f_{\text{out}} = 3500\text{ MHz}$		75		dBc
		$f_{\text{out}} = 4900\text{ MHz}$		76		dBc
		$f_{\text{out}} = 8100\text{ MHz}$		61		dBc
		$f_{\text{out}} = 9600\text{ MHz}$		64		dBc
$f_s/4$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-64		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-75		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-67		dBFS
$f_s/2$	Fixed Spur	$f_{\text{DAC}} = 5898.24\text{MSPS}$		-49		dBFS
		$f_{\text{DAC}} = 8847.36\text{MSPS}$		-48		dBFS
		$f_{\text{DAC}} = 11796.48\text{MSPS}$		-48		dBFS

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$3*f_s/4$	Fixed Spur	2nd Nyquist, $f_{\text{DAC}} = 5898.24\text{MSPS}$		-76		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 8847.36\text{MSPS}$		-89		dBFS
		2nd Nyquist, $f_{\text{DAC}} = 11796.48\text{MSPS}$		-63		dBFS
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 0.85\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-68.5		dBc
		Atten=20dB, Pout=-13dBFS		-67.2		dBc
		Atten=28dB, Pout=-13dBFS		-64.5		dBc
		Atten=39dB, Pout=-13dBFS		-53.9		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 1.8425\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-70.7		dBc
		Atten=20dB, Pout=-13dBFS		-68.3		dBc
		Atten=28dB, Pout=-13dBFS		-62.9		dBc
		Atten=39dB, Pout=-13dBFS		-52.0		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-71		dBc
		Atten=20dB, Pout=-13dBFS		-68		dBc
		Atten=28dB, Pout=-13dBFS		-62		dBc
		Atten=39dB, Pout=-13dBFS		-51.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-70		dBc
		Atten=20dB, Pout=-13dBFS		-67		dBc
		Atten=28dB, Pout=-13dBFS		-60		dBc
		Atten=39dB, Pout=-13dBFS		-49.8		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, LTE 20MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-68.8		dBc
		Atten=20dB, Pout=-13dBFS		-65.9		dBc
		Atten=28dB, Pout=-13dBFS		-60.6		dBc
		Atten=39dB, Pout=-13dBFS		-49.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 2.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-65		dBc
		Atten=20dB, Pout=-13dBFS		-62		dBc
		Atten=20dB, Pout=-13dBFS		-55		dBc
		Atten=39dB, Pout=-13dBFS		-44.3		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-64		dBc
		Atten=20dB, Pout=-13dBFS		-59		dBc
		Atten=28dB, Pout=-13dBFS		-52		dBc
		Atten=39dB, Pout=-13dBFS		-41.1		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-64.1		dBc
		Atten=20dB, Pout=-13dBFS		-60.4		dBc
		Atten=28dB, Pout=-13dBFS		-53.5		dBc
		Atten=39dB, Pout=-13dBFS		-42.5		dBc
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-58		dBc
		Atten=20dB, Pout=-13dBFS		-53		dBc
		Atten=28dB, Pout=-13dBFS		-46		dBc
		Atten=39dB, Pout=-13dBFS		-36		dBc

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACPR _{1xcarr}	ACPR - 1 carrier, NR 100MHz E-TM1.1 carrier $f_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-57		dBc
		Atten=20dB, Pout=-13dBFS		-50		dBc
		Atten=28dB, Pout=-13dBFS		-42		dBc
		Atten=39dB, Pout=-13dBFS		-31		dBc
EVM	Error Vector Magnitude, 1x 20MHz E-TM3.1/3.1a, no ref. clock noise	$F_{\text{out}} = 0.85\text{ GHz}$, $P_{\text{OUT}} = -13\text{dBFS}$		0.2		%
		$F_{\text{out}} = 1.8425\text{ GHz}$, $P_{\text{OUT}} = -13\text{dBFS}$		0.3		%
		$F_{\text{out}} = 2.6\text{ GHz}$, $P_{\text{OUT}} = -13\text{dBFS}$		0.28		%
		$F_{\text{out}} = 3.5\text{ GHz}$, $P_{\text{OUT}} = -13\text{dBFS}$		0.38		%
		$F_{\text{out}} = 4.9\text{ GHz}$, $P_{\text{OUT}} = -13\text{dBFS}$		0.4		%
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 0.85\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-157.6		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-153.3		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-147.9		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-136.9		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 1.8\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-158.4		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-152.2		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-145.6		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 5898.24\text{MSPS}$, Pout=-13dBFS		-134.6		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $f_{\text{OUT}} = 2.6\text{ GHz}$	Atten=0dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-157		dBFS/Hz
		Atten=20dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-151		dBFS/Hz
		Atten=28dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-144		dBFS/Hz
		Atten=39dB, $f_{\text{DAC}} = 8847.36\text{MSPS}$, Pout=-13dBFS		-133.0		dBFS/Hz
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 3.5\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-158		dBFS/Hz
		Atten=20dB, Pout=-13dBFS		-150		dBFS/Hz
		Atten=28dB, Pout=-13dBFS		-143		dBFS/Hz
		Atten=39dB, Pout=-13dBFS		-131.8		dBFS/Hz

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD _{dBFS}	Noise Spectral Density 20MHz offset $F_{\text{out}} = 4.9\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-155.5		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147.8		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140.8		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129.6		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 8.1\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-153		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
NSD _{dBFS}	Noise Spectral Density 50MHz offset $F_{\text{out}} = 9.6\text{ GHz}$	Atten=0dB, Pout=-13dBFS		-152		dBFS/ Hz
		Atten=20dB, Pout=-13dBFS		-147		dBFS/ Hz
		Atten=28dB, Pout=-13dBFS		-140		dBFS/ Hz
		Atten=39dB, Pout=-13dBFS		-129		dBFS/ Hz
S22	Output Return Loss, <6GHz, +/- fc * 10%	with matching		-17		dB
	Output Return Loss, >8GHz, +/- fc * 10%	with matching		-10		dB
Isolation	Near Channel: 1TXOUT to 2TXOUT or 3TXOUT to 4TXOUT ⁽¹⁾	$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-49		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-59		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-65		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-66		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-60		dB
		$f_{\text{out}} = 900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-90		dB
		$f_{\text{out}} = 1850\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-91		dB
		$f_{\text{out}} = 2600\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-93		dB
		$f_{\text{out}} = 3500\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-94		dB
		$f_{\text{out}} = 4900\text{ MHz}$, $f_{\text{DAC}} = 8847.36\text{MSPS}$, straight mode		-83		dB

7.5 Transmitter Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{DAC}} = 11796.48\text{MSPS}$; PLL clock mode below 6GHz output frequency and External clock mode above 6GHz output frequency; interleave mode for 1st Nyquist, non-interleave mix mode for 2nd Nyquist, nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 16.22Gbps; TX clock dither enabled, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN _{TXADD}	Additive Phase Noise External Clock Mode ⁽³⁾	$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{Hz}$		-88		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{kHz}$		-102		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{kHz}$		-110		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{kHz}$		-123		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 1\text{MHz}$		-136		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 10\text{MHz}$		-143		dBc/Hz
		$f_{\text{out}} = 9.6\text{GHz}$, $f_{\text{OFFSET}} = 100\text{MHz}$		-146		dBc/Hz

- (1) Measured with differential 50 ohm across TxP/M. The DC bias to 1.8V to each TxP/M at each pin remains and is not removed. Other external components on the TX paths are disconnected.
- (2) After DSA calibration procedure
- (3) Single side band, input clock phase noise subtracted.

7.6 RF ADC Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC _{RES}	ADC resolution			14		bits
F _{RFin}	RF input frequency range		600		12000	MHz
P _{FS_CW,min}	Min Full scale input power, at device pins ⁽¹⁾	$f_{\text{IN}} = 830\text{ MHz}$, DSA=0dB		-2.9		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA=0dB		-2.8		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA=0dB		-1.8		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA=0dB		-0.4		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA=0dB		0.1		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA=0dB		2.1		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA=0dB		4.3		dBm
P _{FS_CW,MAX}	MAX Full scale input power - reliability limited, at device pins	$f_{\text{IN}} = 830\text{ MHz}$, DSA = 20dB		16.7		dBm
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA = 20dB		17.0		dBm
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA = 20dB		18		dBm
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA = 20dB		18.5		dBm
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA = 20dB		19.3		dBm
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA = 20dB		21.3		dBm
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA = 20dB		23.5		dBm
S ₁₁	Input Return Loss	with matching network		-12.0		dB
ATT _{range}	DSA Attenuation range			25.0		dB
ATT _{step}	DSA Attenuation step			0.5		dB
	DSA Attenuation step accuracy	Delta=Gatt(X)-Gatt(X-1), $F_{\text{in}}=3610\text{MHz}$, after calibration		±0.1		dB
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}}=3610\text{MHz}$, after calibration		±0.9		deg
	DSA Gain Steps Phase accuracy any 8dB range	$F_{\text{in}}=4910\text{MHz}$, after calibration		±1.8		deg
NSD	Noise Density (small signal)	$f_{\text{IN}} = 830\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.2		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.0		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, DSA = 3dB ⁽³⁾		-154.4		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, DSA = 3dB ⁽³⁾		-154.1		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, DSA = 3dB ⁽³⁾		-155.1		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$, DSA = 3dB ⁽³⁾		-150		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$, DSA = 3dB ⁽³⁾		-151		dBFS/Hz
		$f_{\text{IN}} = 830\text{ MHz}$, 3<=Atten<=22		-156.0		dBFS/Hz
		$f_{\text{IN}} = 1760\text{ MHz}$, 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 2610\text{ MHz}$, 3<=Atten<=25		-155.7		dBFS/Hz
		$f_{\text{IN}} = 3610\text{ MHz}$, 3<=Atten<=25		-155.4		dBFS/Hz
		$f_{\text{IN}} = 4910\text{ MHz}$, 3<=Atten<=25		-155.8		dBFS/Hz
		$f_{\text{IN}} = 8150\text{ MHz}$, 3<=Atten<=25		-152.5		dBFS/Hz
		$f_{\text{IN}} = 9610\text{ MHz}$, 3<=Atten<=25		-152.5		dBFS/Hz

7.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF _{min}	Noise Figure min DSA Atten=0 - 3dB	$f_{\text{IN}} = 830\text{ MHz}$		19.1		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		19.0		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		20.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		22.8		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		22.4		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		27.3		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		30		dB
NF	Noise Figure DSA Atten=4dB	$f_{\text{IN}} = 830\text{ MHz}^{(4)}$		20.0		dB
		$f_{\text{IN}} = 1760\text{ MHz}^{(4)}$		20.6		dB
		$f_{\text{IN}} = 2610\text{ MHz}^{(4)}$		21.9		dB
		$f_{\text{IN}} = 3610\text{ MHz}^{(4)}$		23.5		dB
		$f_{\text{IN}} = 4910\text{ MHz}^{(4)}$		22.3		dB
		$f_{\text{IN}} = 8150\text{ MHz}^{(4)}$		27.9		dB
		$f_{\text{IN}} = 9610\text{ MHz}^{(4)}$		30.7		dB
NF _{max}	Noise Figure DSA Atten=20dB	$f_{\text{IN}} = 830\text{ MHz}$		34.7		dB
		$f_{\text{IN}} = 1760\text{ MHz}$		35.2		dB
		$f_{\text{IN}} = 2610\text{ MHz}$		36.0		dB
		$f_{\text{IN}} = 3610\text{ MHz}$		37.3		dB
		$f_{\text{IN}} = 4910\text{ MHz}$		37.6		dB
		$f_{\text{IN}} = 8150\text{ MHz}$		42.8		dB
		$f_{\text{IN}} = 9610\text{ MHz}$		45		dB
IMD3	3 rd order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$ -7dBFS each tone	$f_{\text{IN}} = 840\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-82.4		dBc
		$f_{\text{IN}} = 1770\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-84.1		dBc
		$f_{\text{IN}} = 2610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-74		dBc
		$f_{\text{IN}} = 3610\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-77		dBc
		$f_{\text{IN}} = 4920\text{ MHz}, 3 \leq \text{Atten} \leq 12$		-75.9		dBc
		$f_{\text{IN}} = 8150\text{ MHz}, 3 \leq \text{Atten} \leq 12$, 25MHz tone spacing		-55		dBc
		$f_{\text{IN}} = 9610\text{ MHz}, 3 \leq \text{Atten} \leq 12$, 25MHz tone spacing		-60		dBc
SFDR	Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3$ dBFS	$f_{\text{IN}} = 830\text{ MHz}$		88.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		80.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		78.9		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		71		dBFS

7.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(2) (5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-85.5		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-90.5		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-87		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-84.2		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -3\text{ dBFS}^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-80.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-85.3		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-86		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-75.4		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-70		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-70		dBFS
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -3\text{ dBFS}^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-88.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-80.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-88		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-84		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-81.7		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-78		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-71		dBFS
SFDR	Spurious Free Dynamic Range $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16$	$f_{\text{IN}} = 830\text{ MHz}$		89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		89.8		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		80		dBFS
HD2	2nd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$, with board trim		-79.0		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$, with board trim		-101.6		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$, with board trim		-100		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$, with board trim		-101		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$, with board trim		-99.1		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$, with board trim		-107		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$, with board trim		-107		dBFS
HD3	3rd Harmonic Distortion $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-95.4		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-95.2		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-98		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-97		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-94		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-100		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-102		dBFS

7.6 RF ADC Electrical Characteristics (continued)

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; RX Output Rate = 491.52MSPS below 6GHz, 500MSPS above 6GHz, $f_{\text{ADC}} = 2949.12\text{MSPS}$; PLL clock mode with $f_{\text{REF}} = 491.52\text{MHz}$ below 6GHz input frequency and External clock mode with $f_{\text{CLK}} = 11796.48\text{MHz}$ above 6GHz input frequency; nominal power supplies; DSA Setting = 4dB below 6GHz and 3dB above 6GHz; SerDes rate = 24.33Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HDn, n>3	SFDR excl. HD2 and HD3 $A_{\text{IN}} = -13\text{ dBFS}$ $0 \leq \text{Atten} \leq 16^{(5)}$	$f_{\text{IN}} = 830\text{ MHz}$		-89.2		dBFS
		$f_{\text{IN}} = 1760\text{ MHz}$		-88.8		dBFS
		$f_{\text{IN}} = 2610\text{ MHz}$		-95		dBFS
		$f_{\text{IN}} = 3610\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 4910\text{ MHz}$		-90		dBFS
		$f_{\text{IN}} = 8150\text{ MHz}$		-83		dBFS
		$f_{\text{IN}} = 9610\text{ MHz}$		-80		dBFS
RX-RX Isolation	Near Channel: 1RXIN to 2RXIN 3RXIN to 4RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-76.6		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-70.9		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-73.5		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-76.9		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-65.3		dBc
TX-RX Isolation	Far Channel: 2TXOUT to 1RXIN 4TXOUT to 3RXIN	$f_{\text{IN}} = 830\text{ MHz}$		-85.9		dBc
		$f_{\text{IN}} = 1760\text{ MHz}$		-86.9		dBc
		$f_{\text{IN}} = 2610\text{ MHz}$		-91		dBc
		$f_{\text{IN}} = 3610\text{ MHz}$		-83		dBc
		$f_{\text{IN}} = 4910\text{ MHz}$		-81.9		dBc
		$f_{\text{IN}} = 8150\text{ MHz}$		-68		dBc
		$f_{\text{IN}} = 9610\text{ MHz}$		-68		dBc

- (1) The input fullscale at minimum attenuation can be reduce by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) NLE correction of HD2
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB
- (5) DDC Bypass (TI only test mode)

7.7 PLL/VCO/Clock Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; Reference clock input frequency 491.52MHz (unless otherwise noted), $f_{\text{DAC}} = f_{\text{VCO}}$, $f_{\text{OUT}} = f_{\text{DAC}}/4$, normalized to f_{VCO} .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VCO1}	VCO1 min frequency				7.2	GHz
	VCO1 max frequency		7.68			GHz
f_{VCO2}	VCO2 min frequency				8.8	GHz
	VCO2 max frequency		9.1			GHz
f_{VCO3}	VCO3 min frequency				9.7	GHz
	VCO3 max frequency		10.24			GHz
f_{VCO4}	VCO4 min frequency				11.6	GHz
	VCO4 max frequency		12.08			GHz
DIV_{DAC}	DAC sample rate divider			1, 2 or 3		
$\text{DIV}_{\text{FBAD C}}$	ADC sample rate divider from DAC sample rate			1, 2, 3, 4, 6 or 8		
$\text{DIV}_{\text{RXAD C}}$	ADC sample rate divider			1, 2, 3, 4, 6 or 8		
PN_{VCO}	Closed Loop Phase Noise $F_{\text{PLL}} = 11.79848 \text{ GHz}$ $F_{\text{REF}} = 491.52\text{MHz}$	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-133		dBc/Hz
		50MHz		-141		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 8.84736 \text{ GHz}$ $F_{\text{REF}} = 491.52\text{MHz}$	600kHz		-114		dBc/Hz
		800kHz		-118		dBc/Hz
		1MHz		-120		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-135		dBc/Hz
		50MHz		-142		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 9.8403 \text{ GHz}$ $F_{\text{REF}} = 491.52\text{MHz}$	600kHz		-113		dBc/Hz
		800kHz		-116		dBc/Hz
		1MHz		-119		dBc/Hz
		1.8MHz		-125		dBc/Hz
		5MHz		-134		dBc/Hz
		50MHz		-140		dBc/Hz
	Closed Loop Phase Noise $F_{\text{PLL}} = 7.86432\text{GHz}$ $F_{\text{REF}} = 491.52\text{MHz}$	600kHz		-116		dBc/Hz
		800kHz		-119		dBc/Hz
		1MHz		-122		dBc/Hz
		1.8MHz		-127		dBc/Hz
		5MHz		-136		dBc/Hz
		50MHz		-143		dBc/Hz
F_{rms}	Clock PLL integrated phase error ⁽¹⁾	$f_{\text{PLL}} = 11.79848 \text{ GHz}$, [1KHz, 100MHz]		-43.4		dBc/Hz
		$f_{\text{PLL}} = 8.8536 \text{ GHz}$, [1KHz, 100MHz]		-47.6		dBc/Hz
		$f_{\text{PLL}} = 9.8304 \text{ GHz}$, [1KHz, 100MHz]		-46.2		dBc/Hz
f_{PFD}	PFD frequency		100		500	MHz
$\text{PN}_{\text{pll_flat}}$	Normalized PLL flat Noise	$f_{\text{VCO}} = 11796.48\text{MHz}$		-226.5		dBc/Hz
F_{REF}	Input Clock frequency		0.1		12	GHz
V_{SS}	Input Clock level		0.6		1.8	Vppdiff

7.7 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C; Reference clock input frequency 491.52MHz (unless otherwise noted), f_{DAC} = f_{VCO}, f_{OUT} = f_{DAC}/4, normalized to f_{VCO}.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Coupling				AC Coupling Only		
	REFCLK input impedance ⁽²⁾	Parallel resistance		100		Ω
		Parallel capacitance		0.5		pF

- (1) Single Sideband, not including the reference clock contribution
(2) Refer to S11 data available from TI for impedance vs frequency

7.8 Digital Electrical Characteristics

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CML SerDes Inputs [8:1]SRX+/-						
V _{SRDIFF}	SerDes Receiver Input Amplitude	differential	100		1200	mVpp
V _{SRCOM}	SerDes Input Common Mode		0.4	0.5	0.6	V
Z _{SRdiff}	SerDes Internal Differential Termination ⁽¹⁾			100		Ω
F _{SerDes}	SerDes Bit Rate	Full rate mode	19		29.5	Gbps
		Half rate mode	9.5		16.25	Gbps
		Quarter rate mode	4.75		8.125	Gbps
	Insertion Loss Tolerance ⁽²⁾	Serdes supply = 1.8V		25		dB
TJ	Total Jitter Tolerance				0.42	UI
CML SerDes Outputs [8:1]STX+/-						
V _{STDIFF}	SerDes Transmitter Output Amplitude	differential	500		1000	mVpp
V _{STCOM}	SerDes Output Common Mode		0.4	0.45	0.55	V
Z _{STdiff}	SerDes Output Impedance			100		Ω
TRF	Output rise and fall time	20-80%	8			ps
TEQS	Equalization range				7	dB
TTJ	Output total jitter				0.21	UI
CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1						
V _{IH}	High-Level Input Voltage		0.6×VDD1 P8GPIO			V
V _{IL}	Low-Level Input Voltage		0.4×VDD1 P8GPIO			V
I _{IH}	High-Level Input Current		-250		250	μA
I _{IL}	Low-Level Input Current		-250		250	μA
C _L	CMOS input capacitance			2		pF
V _{OH}	High-Level Output Voltage		VDD1P8G PIO-0.2			V
V _{OL}	Low-Level Output Voltage				0.2	V
Differential Inputs: SYSREF+/- Mode A						
Clock _{MODE}				PLL Clock Mode Only		
F _{SYSREFMAX}	SYSREF Input Frequency Maximum			40		MHz
V _{SWINGSRMAX}	SYSREF Input Swing Maximum			1.8		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} < 500MHz		0.3		Vppdiff ⁽³⁾
V _{SWINGSRMIN}	SYSREF Input Swing Minimum	f _{REF} > 500MHz		0.6		Vppdiff ⁽³⁾
V _{COMSRMAX}	SYSREF Input Common Mode Voltage Maximum			0.8		V
V _{COMSRMIN}	SYSREF Input Common Mode Voltage Minimum			0.6		V
Z _T	Input termination	differential		100 ⁽¹⁾		Ω
C _L	Input capacitance	Each pin to GND		0.5		pF
LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-						
V _{ICOM}	Input Common Voltage			1.2		V
V _{ID}	Differential Input Voltage swing			450		Vppdiff ⁽³⁾
Z _T	Input termination	differential		100		Ω

7.8 Digital Electrical Characteristics (continued)

Typical values at TA = +25°C, full temperature range is T_{A,MIN} = -40°C to T_{J,MAX} = +110°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-						
V _{OCOM}	Output Common Voltage			1.2		V
V _{OD}	Differential Output Voltage swing			500		V _{ppdiff} ⁽³⁾
Z _T	Internal Termination			100		Ω

- (1) SYSREF termination is programmable between 100Ω, 150Ω and 300Ω
- (2) Loss tolerance is bump to bump from STX to SRX
- (3) V_{ppdiff} is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

7.9 Power Supply Electrical Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{A,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 3000\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 1: 4T4R - TDD with TX 75%, RX 25% TX Dual Band: 72x Int, TX Rate 125 MSPS RX Dual Band: 24x Dec, RX Rate 125 MSPS		765		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			395		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			69		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF	$f_{\text{DAC}} = 9000\text{MSPS}$, $f_{\text{OUT}} = f_{\text{IN}} = 1.9, 2.6\text{ GHz}$ $f_{\text{ADC}} = 3000\text{MSPS}$ JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		1151		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2001		mA
P_{diss}	Power Dissipation			5446		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 2: 4T4R - FDD TX Dual Band: 96x Int, TX Rate 125 MSPS RX Dual Band: RX 24x, RX Rate 125 MSPS		1338		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			506		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF	$f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{ADC}} = 3\text{ GSPS}$, $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 2-16-16-1, RX: 2-16-16-1		2109		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3311		mA
P_{diss}	Power Dissipation			9041		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 3: 4T4R - FDD TX Single Band: 96x Int, TX Rate 125 MSPS RX Single Band: RX 24x, RX Rate 125 MSPS		1332		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			496		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLVC0			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF	$f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{ADC}} = 3\text{ GSPS}$, $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 1-8-16-1, RX: 1-8-16-1		2099		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			2950		mA
P_{diss}	Power Dissipation			8667		mW

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 500MSPS, RX Output Rate = 500MSPS, $f_{\text{DAC}} = 9000\text{MSPS}$ interleave mode; $f_{\text{ADC}} = 3000\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 20Gbps; unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 4: 4T4R - FDD TX Single Band: 24x Int, TX Rate 500 MSPS RX Single Band: RX 6x, RX Rate 500 MSPS $f_{\text{DAC}} = 12\text{ GSPS}$, $f_{\text{TX}} = 1.85 + 2.15\text{ GHz}$ $f_{\text{ADC}} = 3\text{ GSPS}$, $f_{\text{RX}} = 1.75 + 1.88\text{ GHz}$ JESD: 8/10 coding, 20Gbps TX: 4-8-4-1, RX: 4-8-4-1		1331		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			648		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			72		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			2096		mA
I_{VDD0P9}	Group 1A: DVDD0P9 + VDDT0P9			3269		mA
P_{diss}	Power Dissipation			9230		mW
I_{VDD1P8}	Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX	Mode 5: same configuration as Mode 4 Sleep Mode. SLEEP pin is pull high.		98		mA
	Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC + VDD1P8GPIO + VDDA1P8			330		mA
	Group 3C: VDD1P8PLL + VDD1P8PLLCO			16		mA
I_{VDD1P2}	Group 2: VDD1P2FB, VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2FBCML, VDD1P2RXCML and VDD1P2PLLCLKREF			48		mA
	Group 1A: DVDD0P9 + VDDT0P9			305		mA
	Power Dissipation			1140		mW

7.10 Timing Requirements

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

		MIN	NOM	MAX	UNIT
Timing: SYSREF+/-					
$t_{\text{s}}(\text{SYSREF})$	Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-		50		ps
$t_{\text{h}}(\text{SYSREF})$	Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-		50		ps
Timing: Serial ports					
$t_{\text{s}}(\text{SENB})$	Setup Time, SENB to Rising Edge of SCLK			15	ns
$t_{\text{h}}(\text{SENB})$	Hold Time, SENB after last Rising Edge of SCLK ⁽¹⁾		$5 + t_{\text{SCLK}}$		ns
$t_{\text{s}}(\text{SDIO})$	Setup Time, SDIO valid to Rising Edge of SCLK			15	ns
$t_{\text{h}}(\text{SDIO})$	Hold Time, SDIO valid after Rising Edge of SCLK			5	ns
$t_{\text{(SCLK)_W}}$	Minimum SCLK period: registers write			25	ns
$t_{\text{(SCLK)_R}}$	Minimum SCLK period: registers read			50	ns
$t_{\text{d}}(\text{data_out})$	Minimum Data Output delay after Falling Edge of SCLK			0	ns
	Maximum Data Output delay after Falling Edge of SCLK			15	ns
t_{RESET}	Minimum RESET Pulse Width		1		ms

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

7.11 Switching Characteristics

Typical values at $T_A = +25^\circ\text{C}$, full temperature range is $T_{A,\text{MIN}} = -40^\circ\text{C}$ to $T_{J,\text{MAX}} = +110^\circ\text{C}$; TX Input Rate = 491.52MSPS, $f_{\text{DAC}} = 8847.36\text{MSPS}$; $f_{\text{ADC}} = 2949.12\text{MSPS}$; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation = 0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

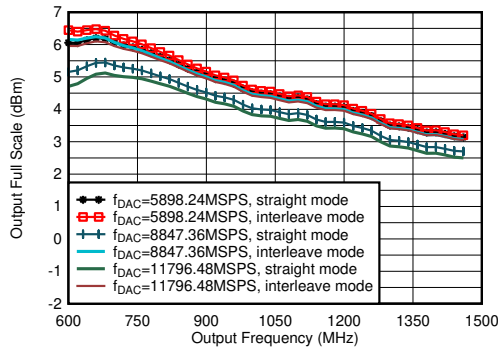
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TX Channel Latency						
	SerDes Receiver Analog Delay	Full rate		2.8		ns
t _{JESD} TX	JESD to TX output Latency	LMFSHd=2-8-8-1, 368.64 MSPS input rate, 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		152		interface clock cycles ⁽¹⁾
		LMFSHd=8-16-4-1, 491.52 MSPS 24x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		176		
		LMFSHd=4-16-8-1, 245.76 MSPS 48x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		124		
		LMFSHd=2-16-16-1, 122.88 MSPS 96x Interpolation, Serdes rate = 16.22Gbps (JESD204C)		97		
RX Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD} RX	RX input to JESD output Latency	LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C)		92		interface clock cycles ⁽¹⁾
		LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)		108		
		LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)		153		
FB Channel Latency						
	SerDes Transmitter Analog Delay			3.6		ns
t _{JESD} FB	FB input to JESD output Latency	LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation		151		interface clock cycles ⁽¹⁾
		LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation		177		

(1) Interface clock cycles is the period of the digital interface sample rate, e.g. 1GSPS = 1ns.

7.12 Typical Characteristics

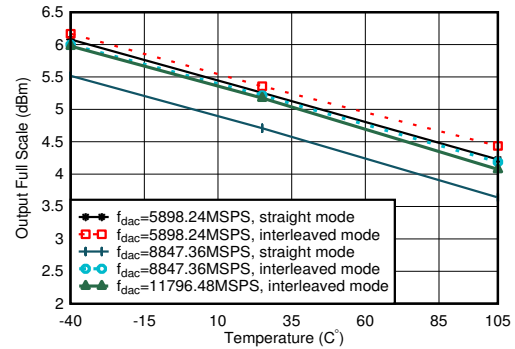
7.12.1 TX Typical Characteristics 800 MHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



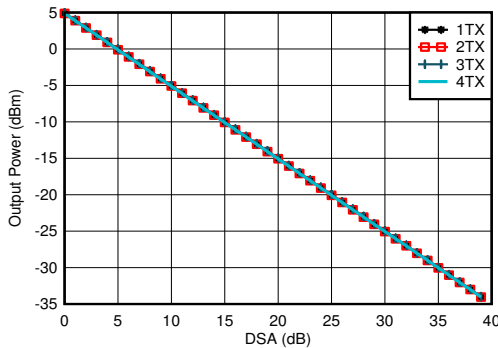
including PCB and cable losses, $A_{\text{out}} = -0.5\text{d FBS}$, DSA = 0, 0.8 GHz matching

Figure 7-1. TX Output Fullscale vs Output Frequency



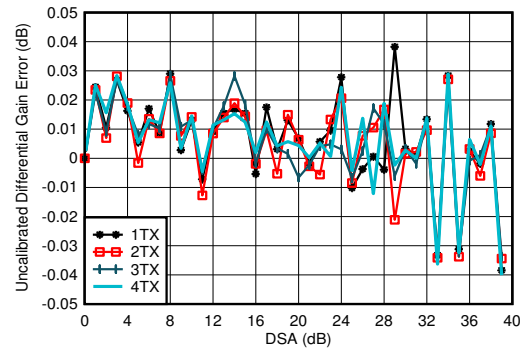
including PCB and cable losses, $A_{\text{out}} = -0.5\text{d FBS}$, DSA = 0, 0.8 GHz matching

Figure 7-2. TX Output Fullscale vs Temperature



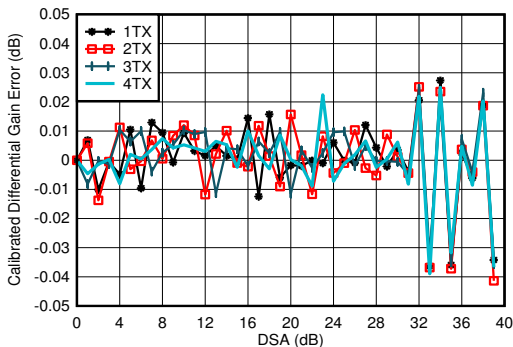
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $A_{\text{out}} = -0.5$ dBFS, matching 0.8 GHz

Figure 7-3. TX Output Power vs DSA Setting and Channel at 0.85 GHz



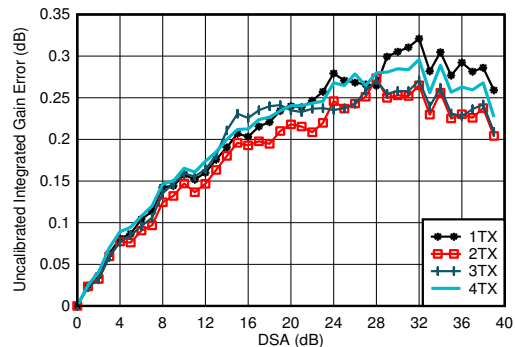
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-4. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-5. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 0.85 GHz

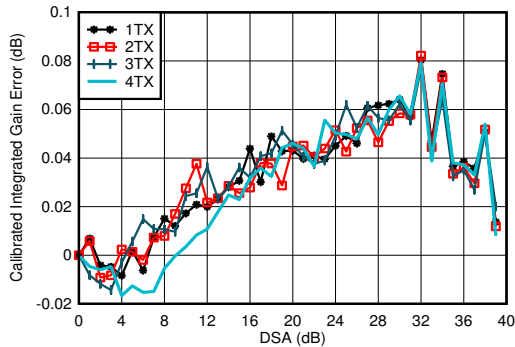


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Settings}$

Figure 7-6. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz

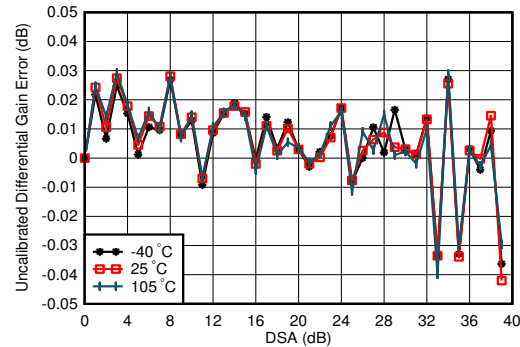
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



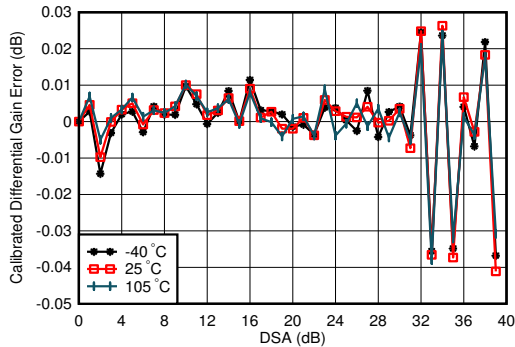
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 7-7. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 0.85 GHz



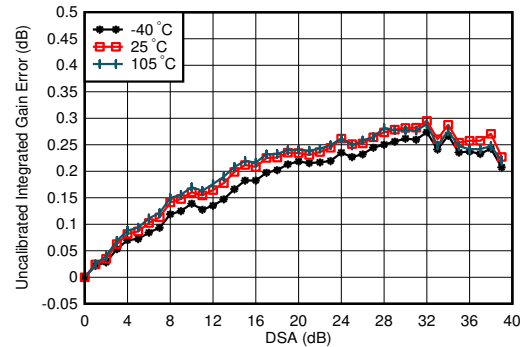
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-8. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



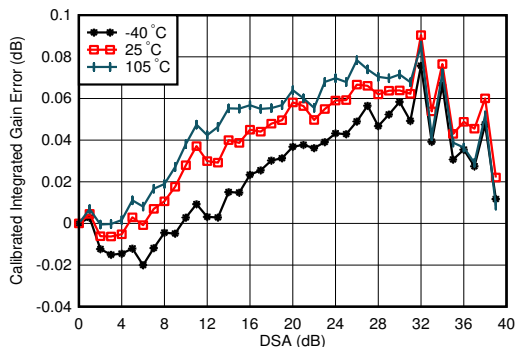
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-9. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 0.85 GHz



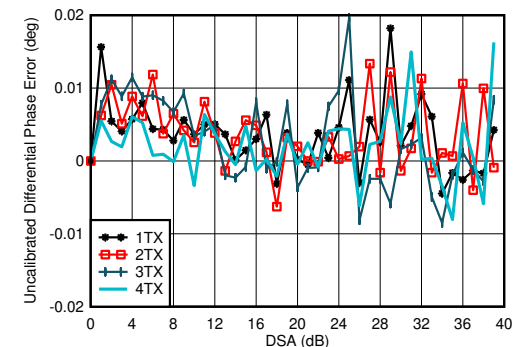
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 7-10. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + \text{DSA Setting}$

Figure 7-11. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 0.85 GHz

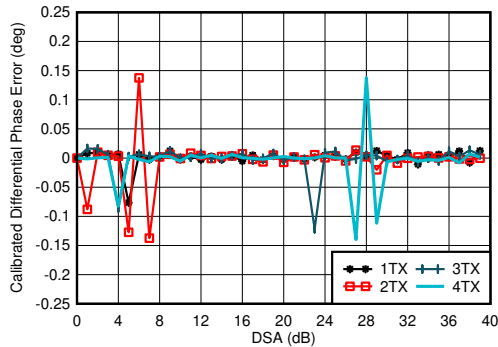


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-12. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz

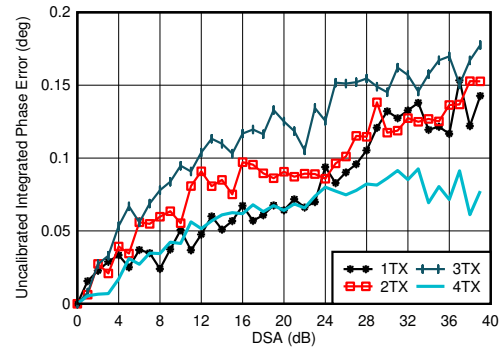
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



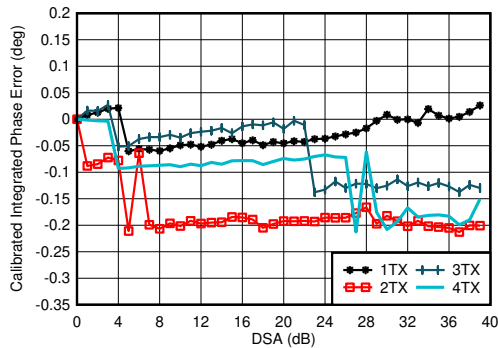
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

Figure 7-13. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 0.85 GHz



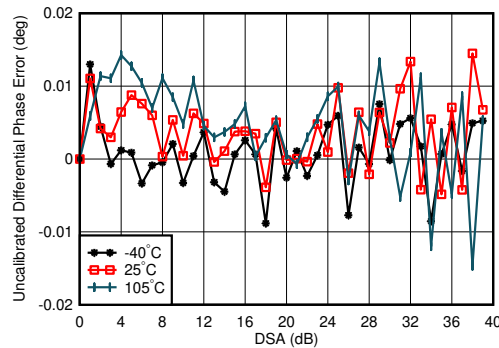
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-14. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-15. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 0.85 GHz

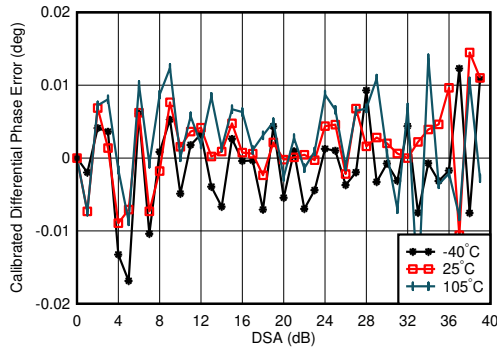


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-16. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz

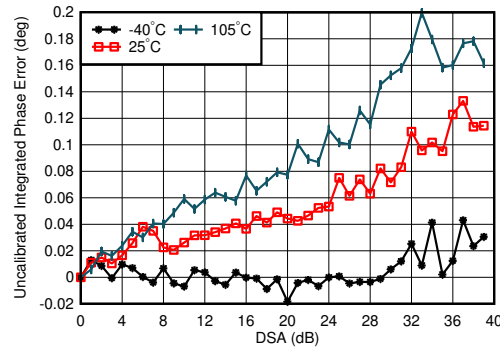
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



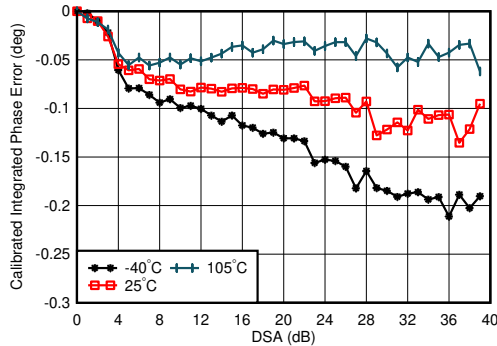
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} + 1)$

Figure 7-17. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 0.85 GHz



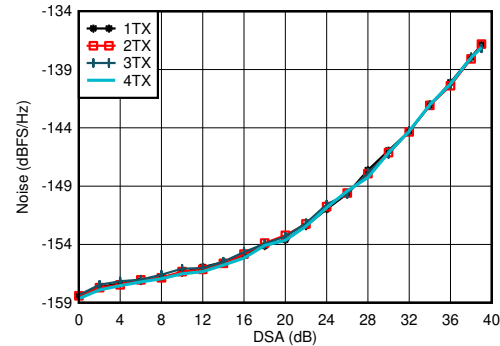
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-18. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



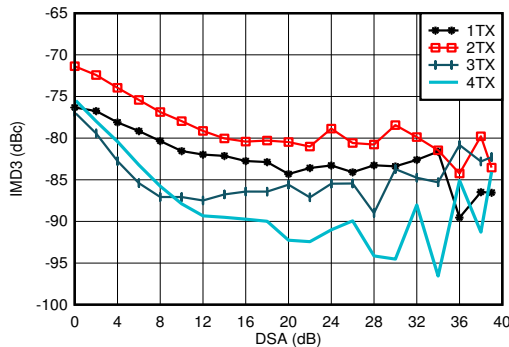
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz
Integrated Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting}) - \text{Phase}_{\text{OUT}}(\text{DSA Setting} = 0)$

Figure 7-19. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 0.85 GHz



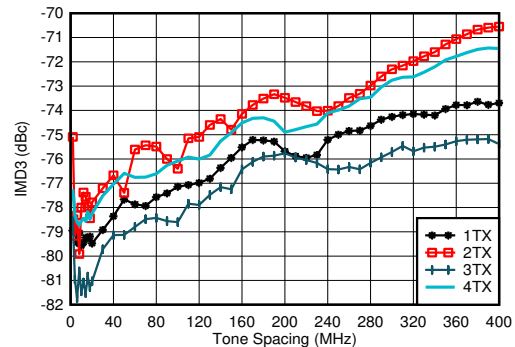
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 0.8 GHz,
 $P_{\text{OUT}} = -13$ dBFS

Figure 7-20. TX Output Noise vs Channel and Attenuation at 0.85 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

Figure 7-21. TX IMD3 vs DSA Setting at 0.85 GHz

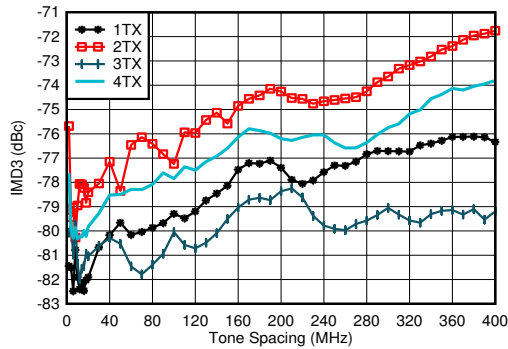


$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

Figure 7-22. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz

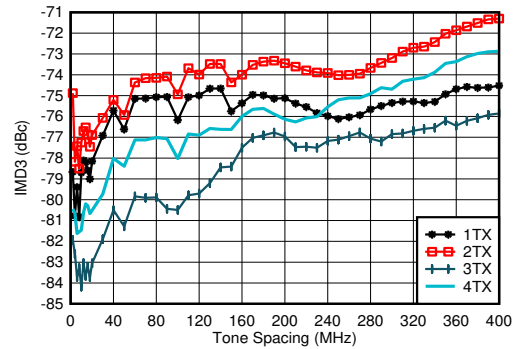
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



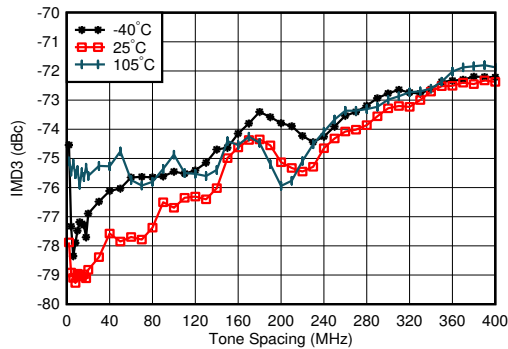
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

Figure 7-23. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



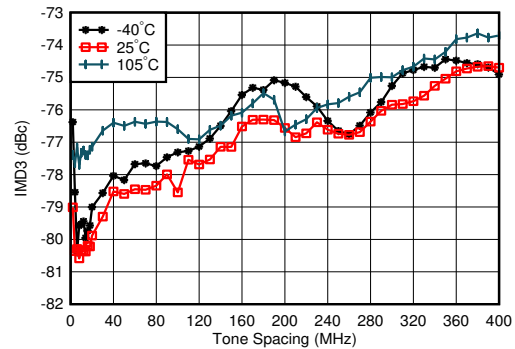
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone

Figure 7-24. TX IMD3 vs Tone Spacing and Channel at 0.85 GHz



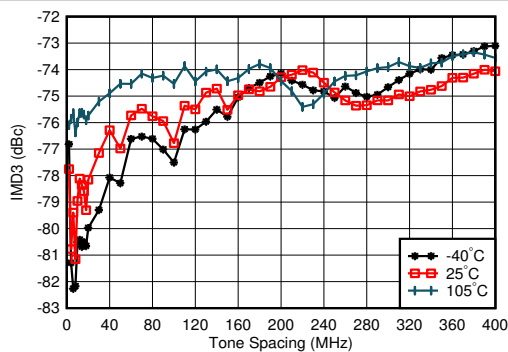
$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-25. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



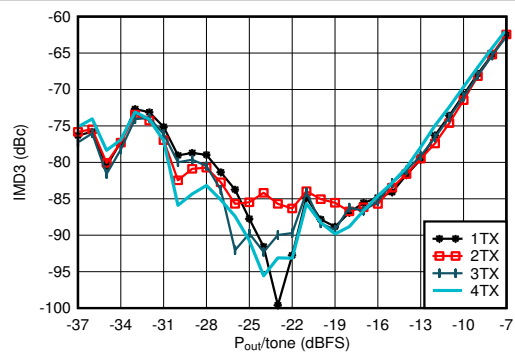
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-26. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, matching at 0.8 GHz, -13 dBFS each tone, worst channel

Figure 7-27. TX IMD3 vs Tone Spacing and Temperature at 0.85 GHz

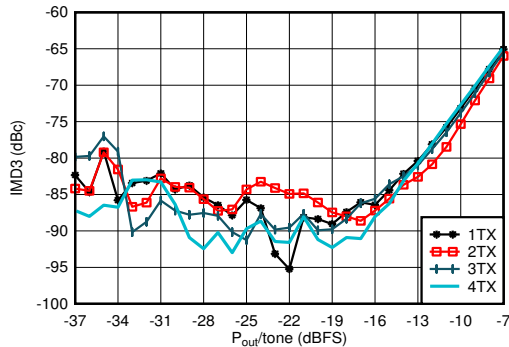


$f_{\text{DAC}} = 5898.24$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz, $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

Figure 7-28. TX IMD3 vs Digital Level at 0.85 GHz

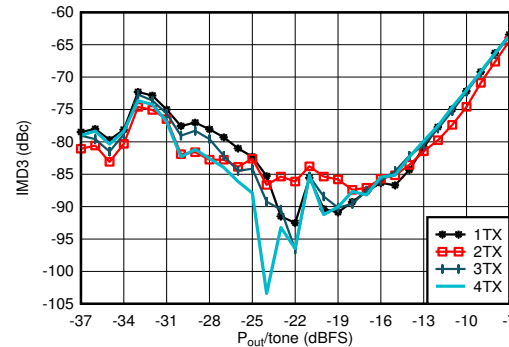
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



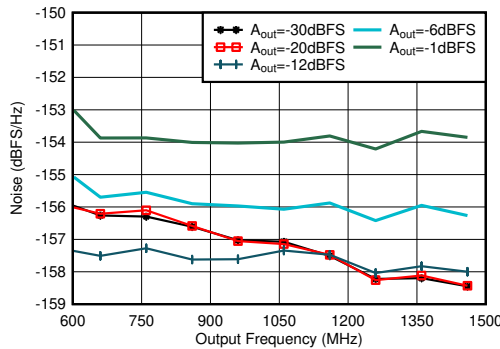
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 0.85$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

Figure 7-29. TX IMD3 vs Digital Level at 0.85 GHz



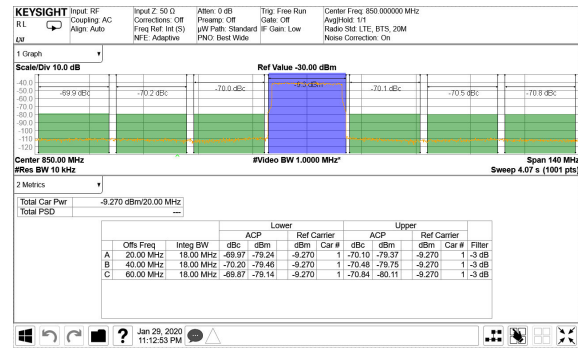
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 0.85$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 0.8 GHz

Figure 7-30. TX IMD3 vs Digital Level at 0.85 GHz



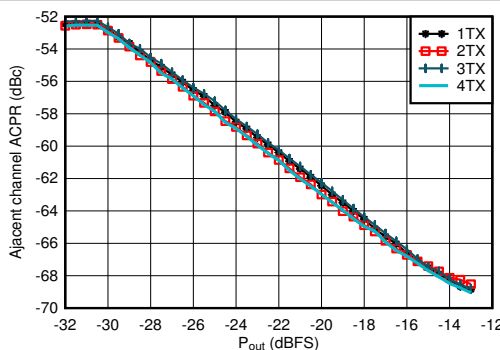
Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSPS,
interleave mode, 40-MHz offset, DSA = 0dB

Figure 7-31. TX Single Tone Output Noise vs Frequency and Amplitude at 0.85 GHz



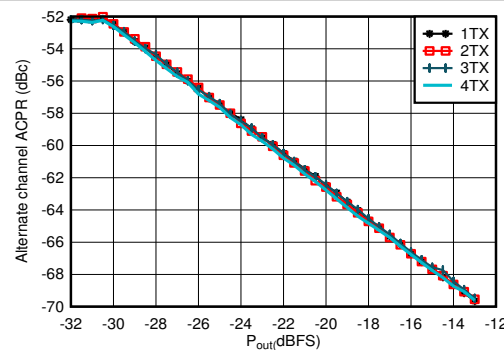
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

Figure 7-32. TX 20-MHz LTE Output Spectrum at 0.85 GHz



Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-33. TX 20-MHz LTE ACPR vs Digital Level at 0.85 GHz

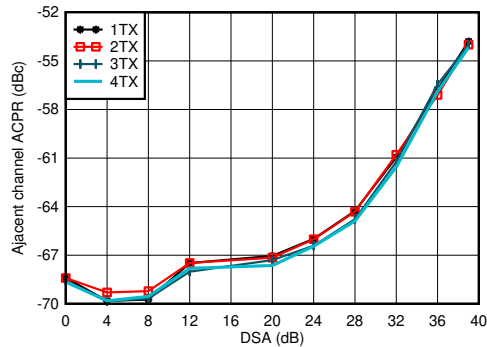


Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-34. TX 20-MHz LTE alt-ACPR vs Digital Level at 0.85 GHz

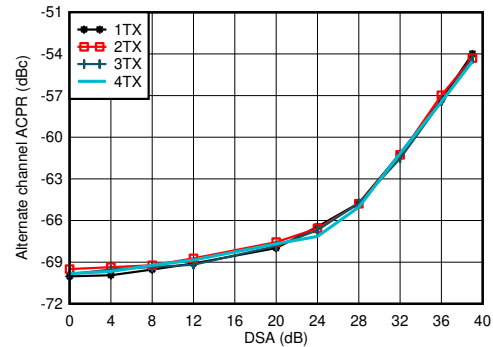
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



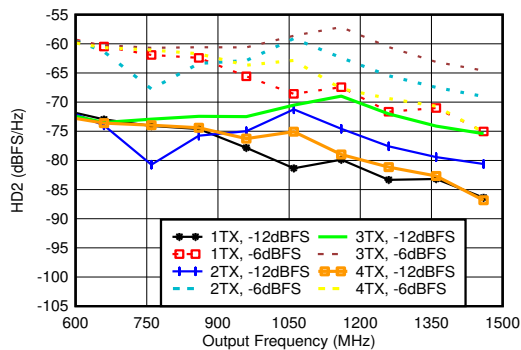
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-35. TX 20-MHz LTE ACPR vs DSA at 0.85 GHz



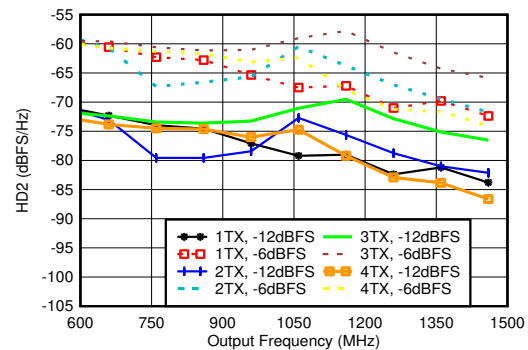
Matching at 0.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-36. TX 20-MHz LTE alt-ACPR vs DSA at 0.85 GHz



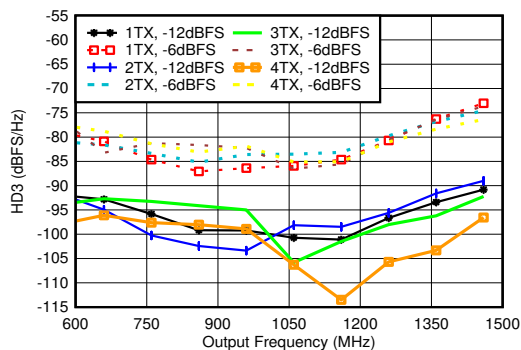
Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24$ GSPS, straight mode

Figure 7-37. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



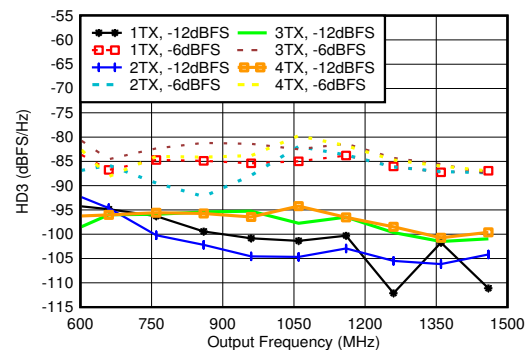
Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36$ GSPS, straight mode

Figure 7-38. TX HD2 vs Digital Amplitude and Output Frequency at 0.85 GHz



Matching at 0.8 GHz, $f_{\text{DAC}} = 5898.24$ MSPS, straight mode, normalized to output power at harmonic frequency

Figure 7-39. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

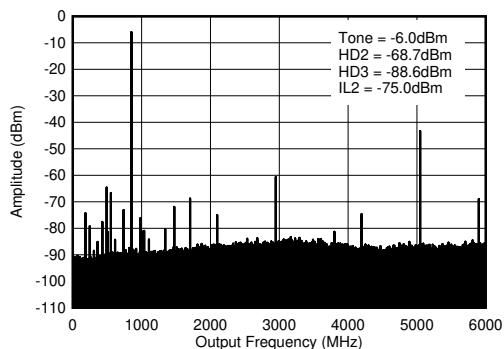


Matching at 0.8 GHz, $f_{\text{DAC}} = 8847.36$ MSPS, straight mode, normalized to output power at harmonic frequency

Figure 7-40. TX HD3 vs Digital Amplitude and Output Frequency at 0.85 GHz

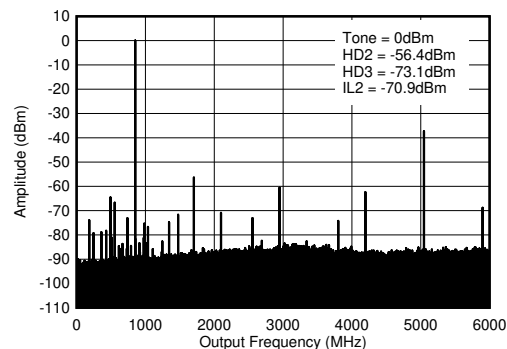
7.12.1 TX Typical Characteristics 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ M SPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



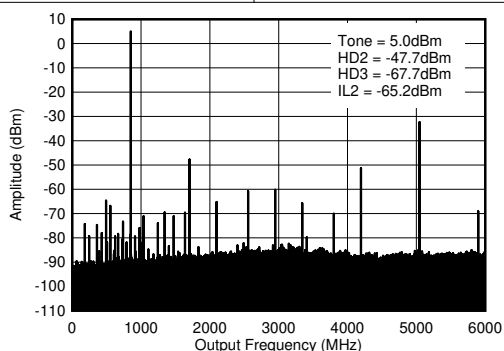
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-41. TX Single Tone (-12 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-42. TX Single Tone (-6 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

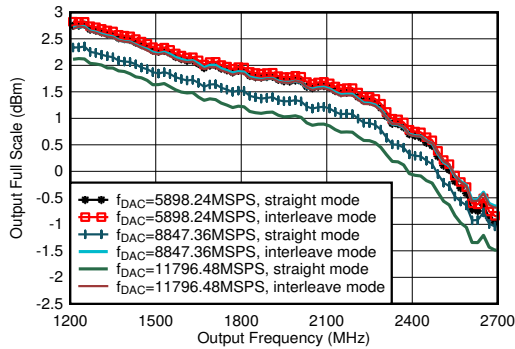


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, 0.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$.

Figure 7-43. TX Single Tone (-1 dBFS) Output Spectrum at 0.85 GHz ($0-f_{\text{DAC}}$)

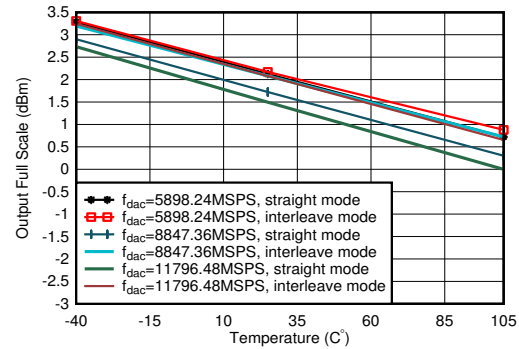
7.12.2 TX Typical Characteristics at 1.8 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



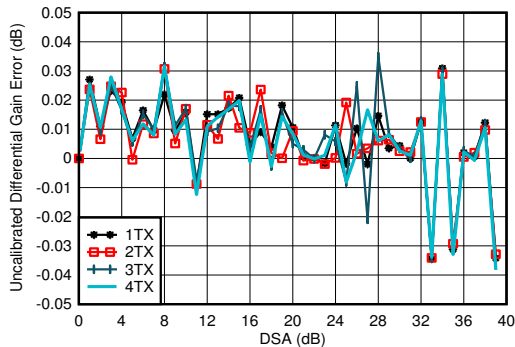
including PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 1.8 GHz matching

Figure 7-44. TX Output Fullscale vs Output Frequency



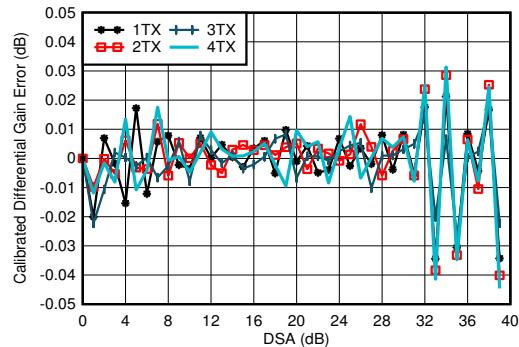
$A_{\text{out}} = -0.5$ dBFS, matching 1.8 GHz

Figure 7-45. TX Output Power vs Temperature at 1.8 GHz



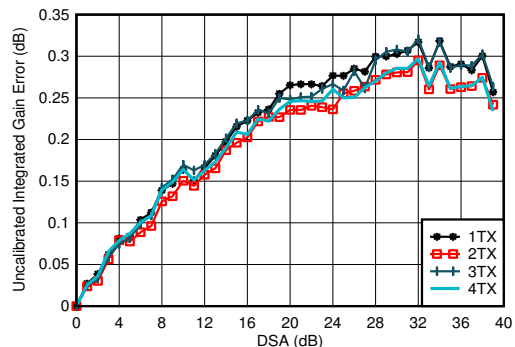
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-46. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



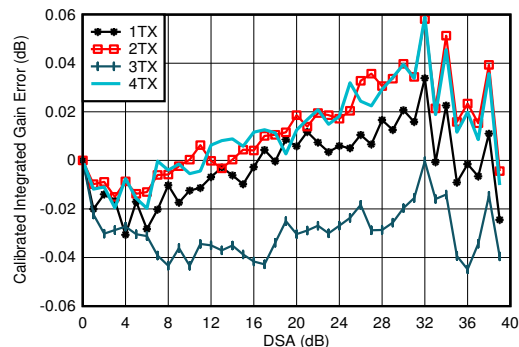
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-47. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-48. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

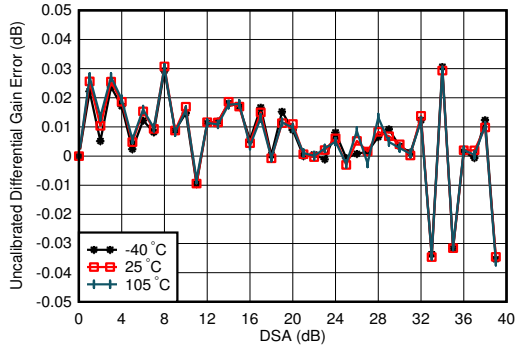


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-49. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 1.8 GHz

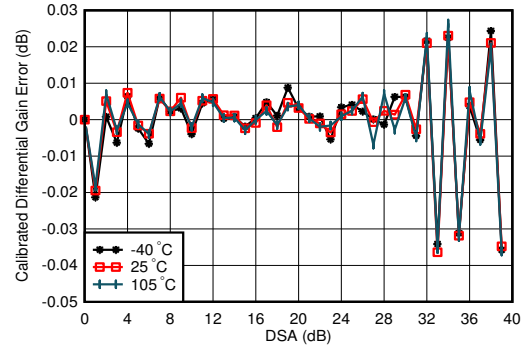
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



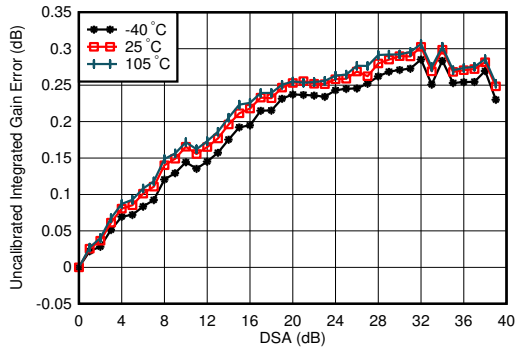
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-50. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



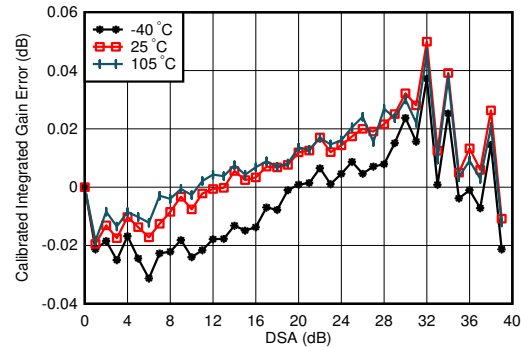
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-51. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 1.8 GHz



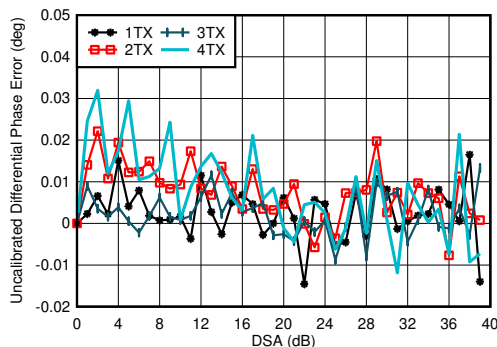
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-52. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



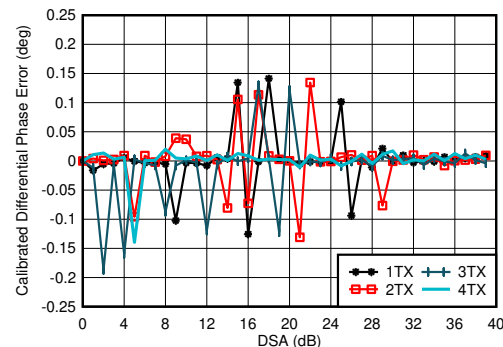
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-53. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-54. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

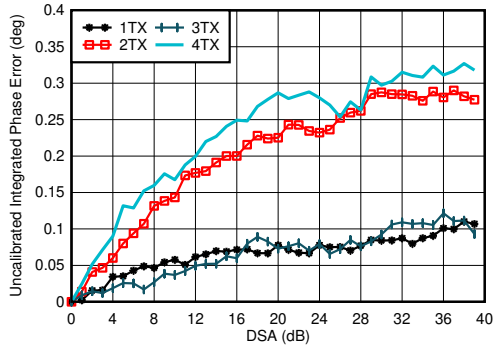


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
Phase DNL spike may occur at any DSA setting.

Figure 7-55. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 1.8 GHz

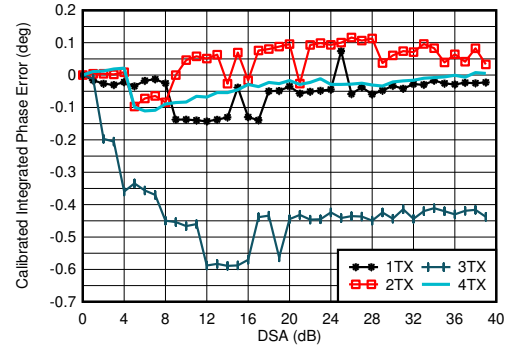
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



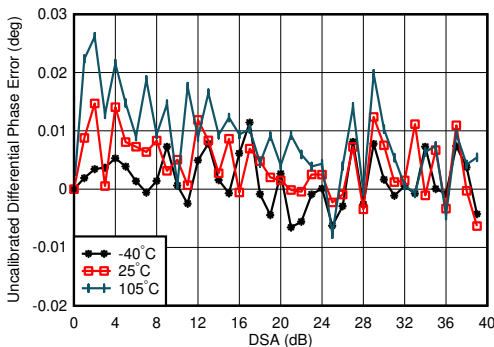
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-56. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



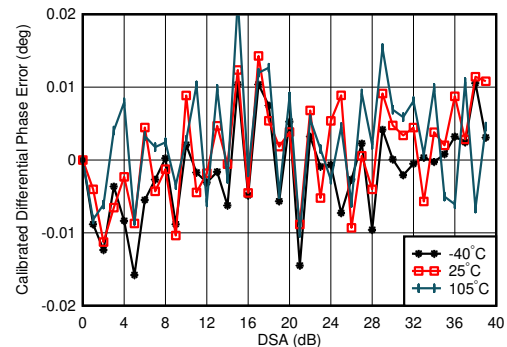
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-57. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 1.8 GHz



$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-58. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz

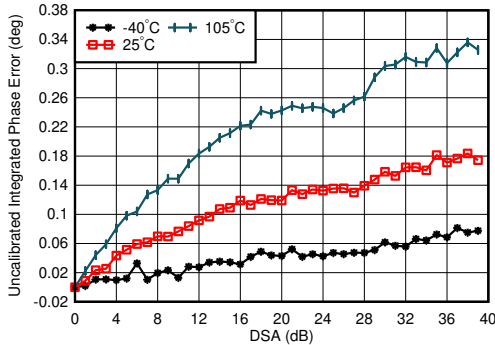


$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-59. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 1.8 GHz

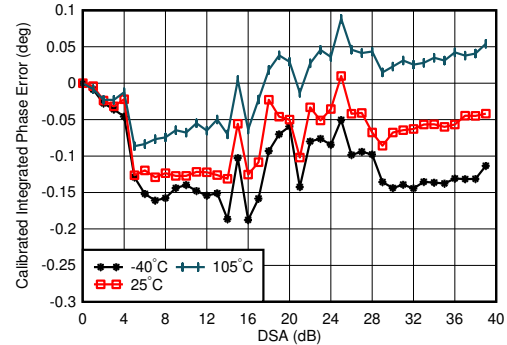
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



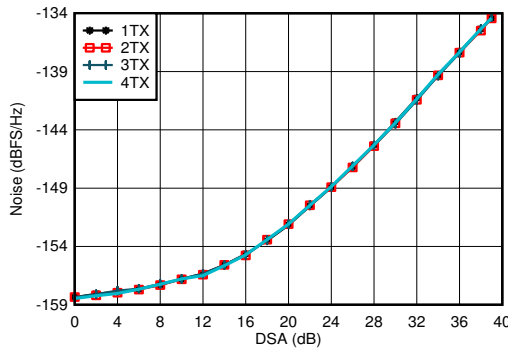
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-60. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



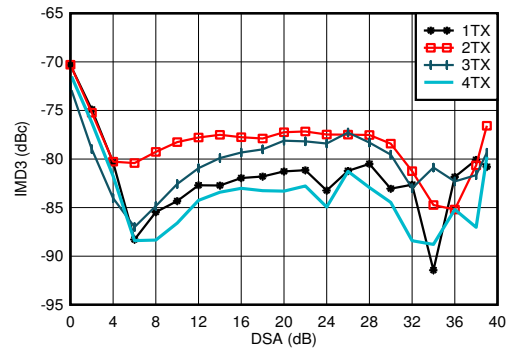
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-61. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 1.8 GHz



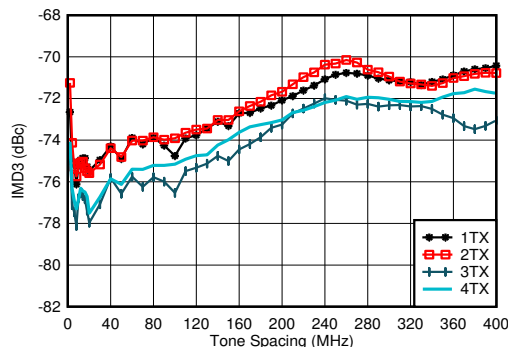
$f_{\text{DAC}} = 5898.24$ MSPS, interleave mode, matching at 1.8 GHz, $P_{\text{OUT}} = -13$ dBFS

Figure 7-62. TX Output Noise vs Channel and Attenuation at 1.8 GHz



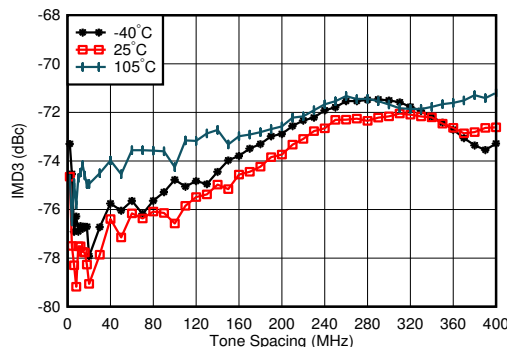
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone

Figure 7-63. TX IMD3 vs DSA Setting at 1.8 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone

Figure 7-64. TX IMD3 vs Tone Spacing and Channel at 1.8 GHz

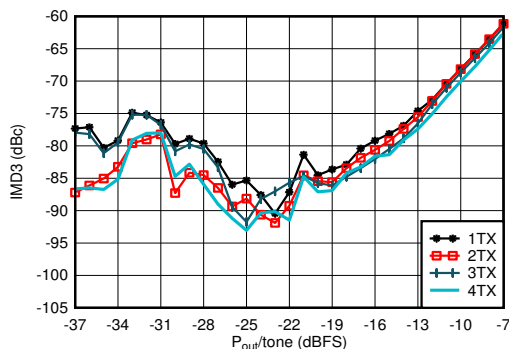


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz, matching at 1.8 GHz, -13 dBFS each tone, worst channel

Figure 7-65. TX IMD3 vs Tone Spacing and Temperature at 1.8 GHz

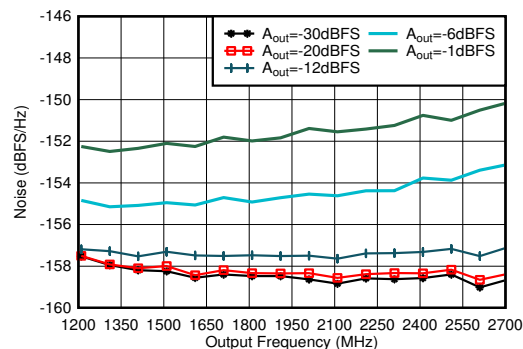
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



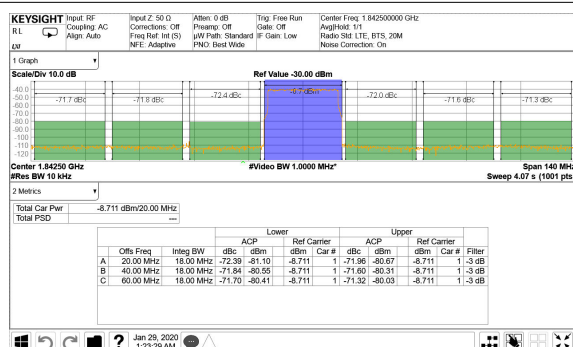
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, $f_{\text{CENTER}} = 1.8$ GHz,
 $f_{\text{SPACING}} = 20$ MHz, matching at 1.8 GHz

Figure 7-66. TX IMD3 vs Digital Level at 1.8 GHz



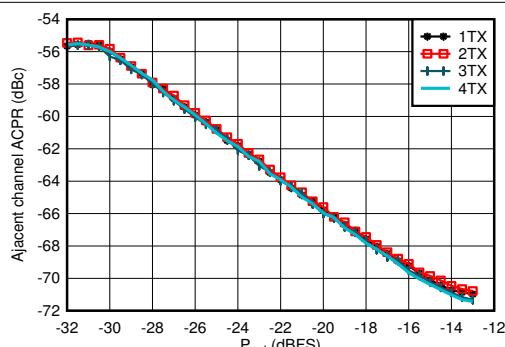
Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSPS,
interleave mode, 40-MHz offset

Figure 7-67. TX Single Tone Output Noise vs Frequency and Amplitude at 1.8 GHz



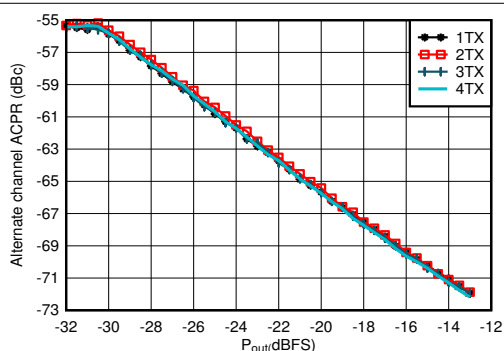
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

Figure 7-68. TX 20-MHz LTE Output Spectrum at 1.8425 GHz



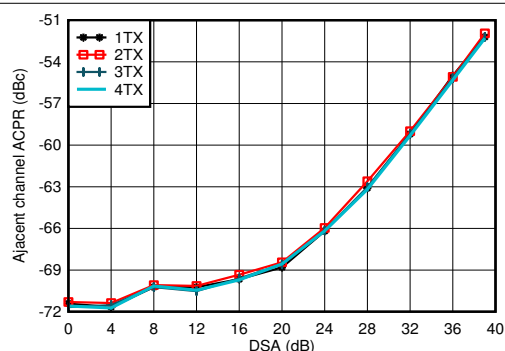
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-69. TX 20-MHz LTE ACPR vs Digital Level at 1.8425 GHz



Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-70. TX 20-MHz LTE alt-ACPR vs Digital Level at 1.8425 GHz

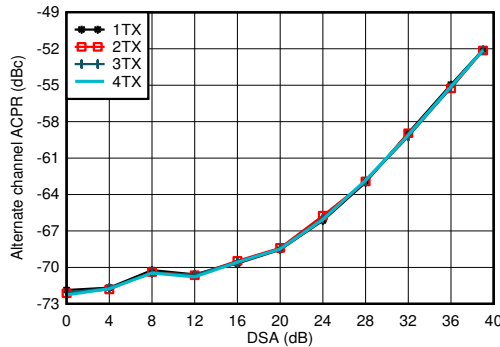


Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-71. TX 20-MHz LTE ACPR vs DSA at 1.8 GHz

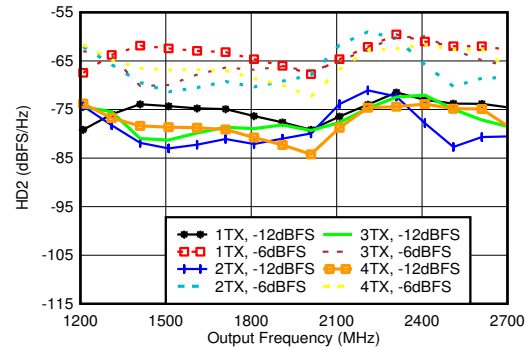
7.12.2 TX Typical Characteristics at 1.8 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



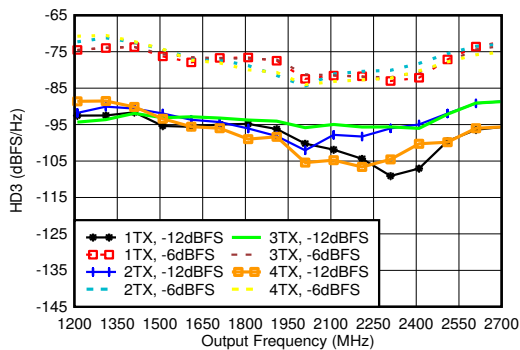
Matching at 1.8 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-72. TX 20-MHz LTE alt-ACPR vs DSA at 1.8 GHz



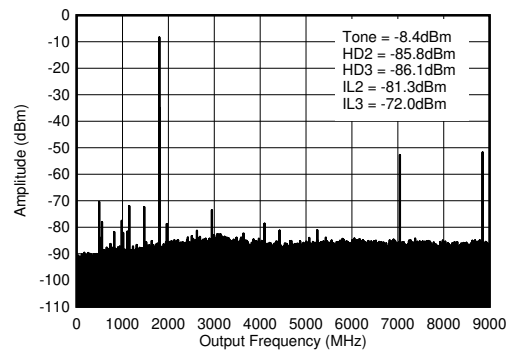
Matching at 1.8 GHz, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-73. TX HD2 vs Digital Amplitude and Output Frequency at 1.8 GHz



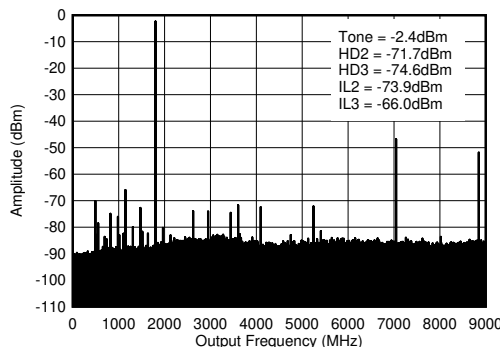
Matching at 1.8 GHz, $f_{\text{DAC}} = 11.7964$ GSPPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-74. TX HD3 vs Digital Amplitude and Output Frequency at 1.8 GHz



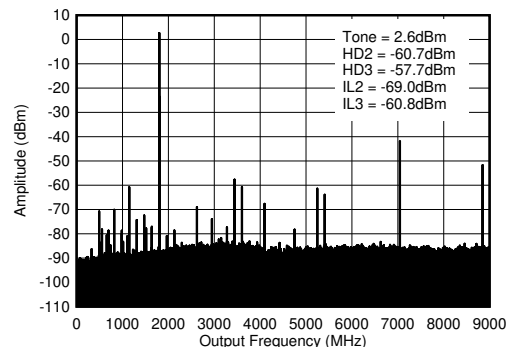
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-75. TX Single Tone (-12 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-76. TX Single Tone (-6 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

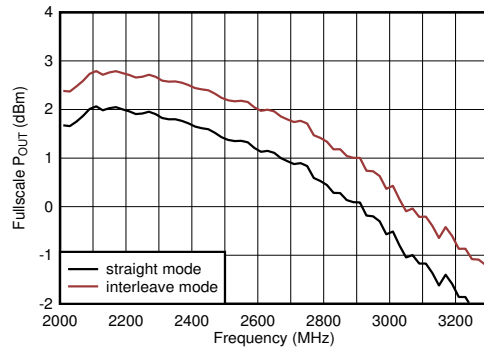


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 1.8 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-77. TX Single Tone (-1 dBFS) Output Spectrum at 1.8 GHz ($0-f_{\text{DAC}}$)

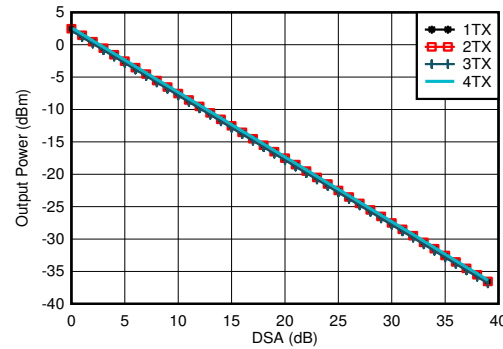
7.12.3 TX Typical Characteristics at 2.6 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, TX Clock Dither Enabled



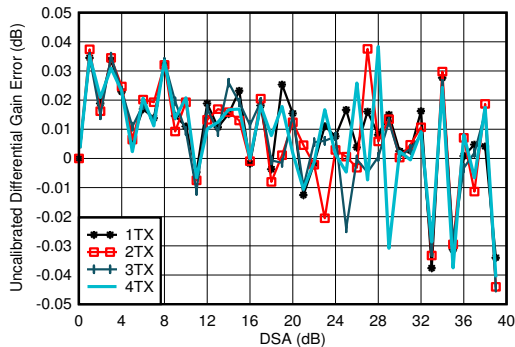
Including PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 2.6 GHz matching

Figure 7-78. TX Full Scale vs RF Frequency at 11796.48 MSPS



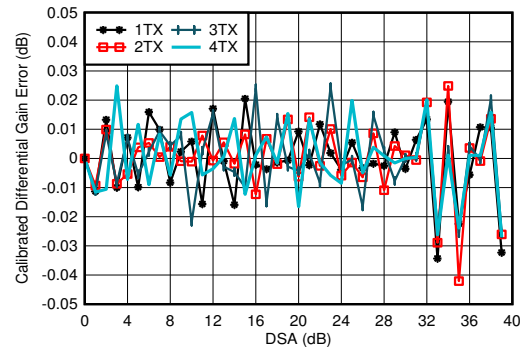
$f_{\text{DAC}} = 8847.36$ MSPS, $A_{\text{out}} = -0.5$ dBFS, matching 2.6 GHz

Figure 7-79. TX Output Power vs DSA Setting and Channel at 2.6 GHz



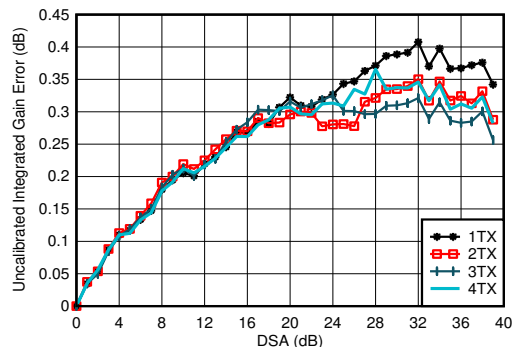
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-80. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



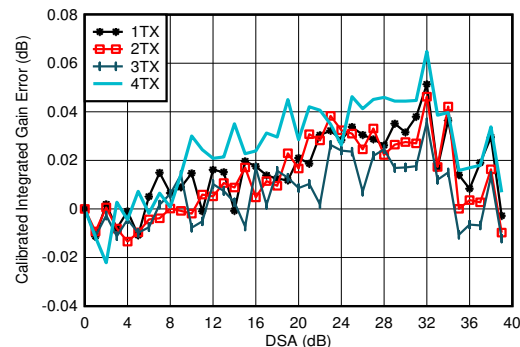
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-81. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-82. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

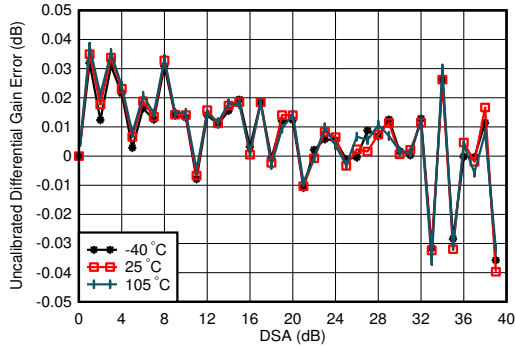


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-83. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 2.6 GHz

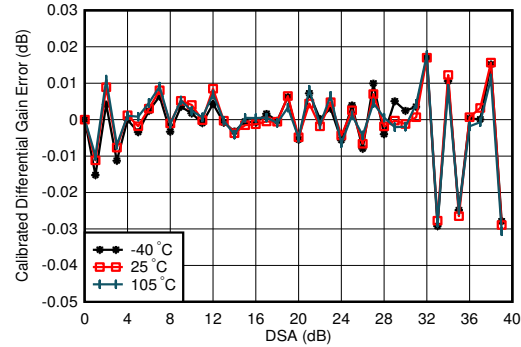
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



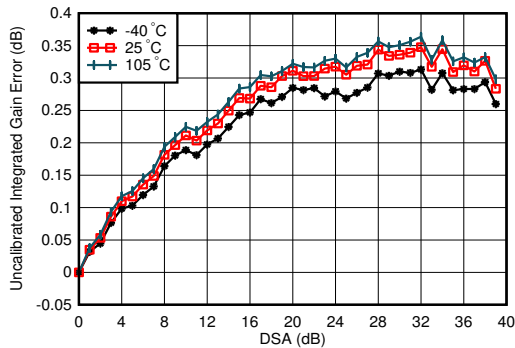
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-84. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



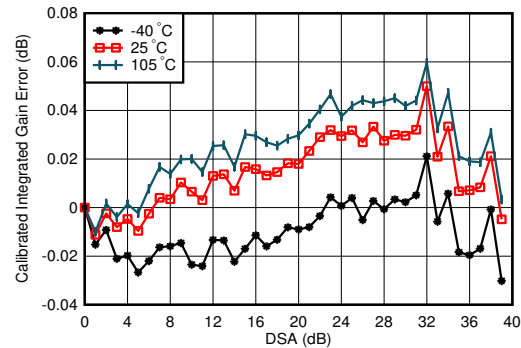
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-85. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-86. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

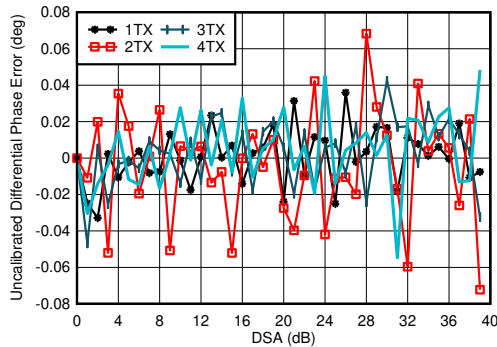


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-87. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 2.6 GHz

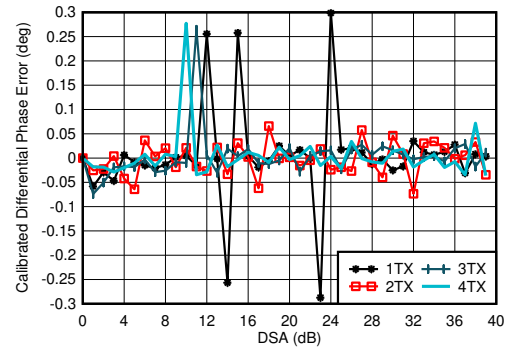
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



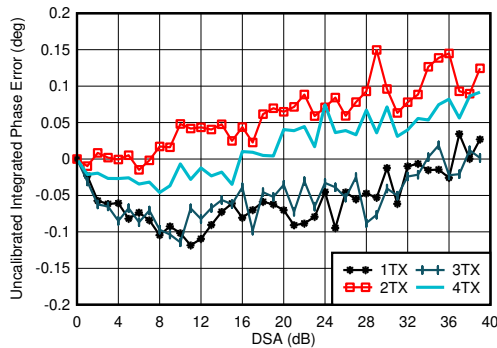
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-88. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



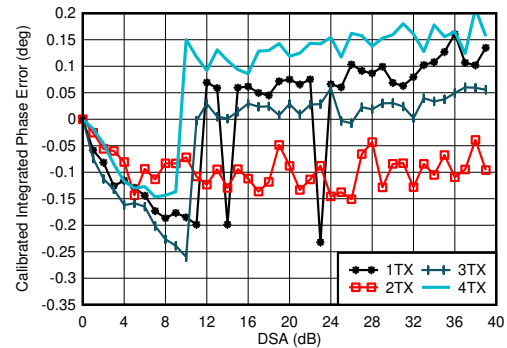
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
 Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$
 Phase DNL spike may occur at any DSA setting.

Figure 7-89. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
 Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-90. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

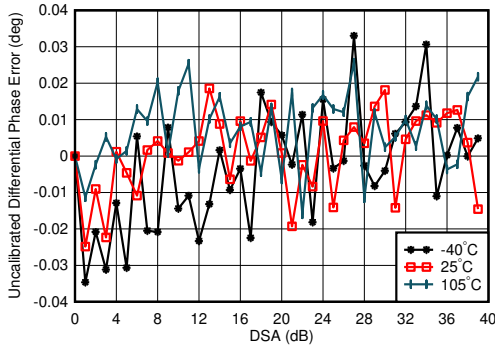


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz
 Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-91. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 2.6 GHz

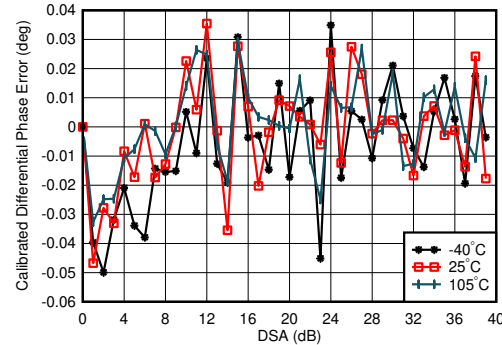
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



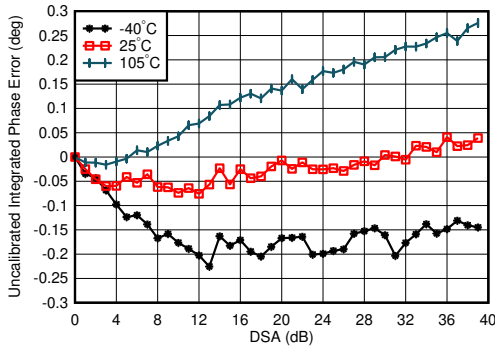
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-92. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



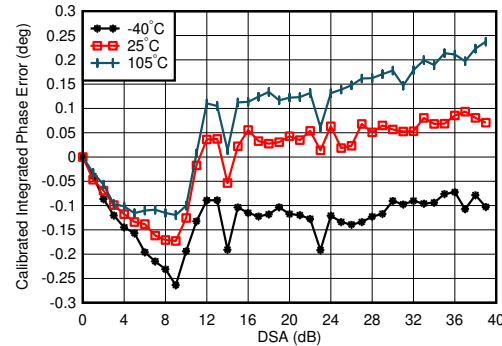
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-93. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 2.6 GHz



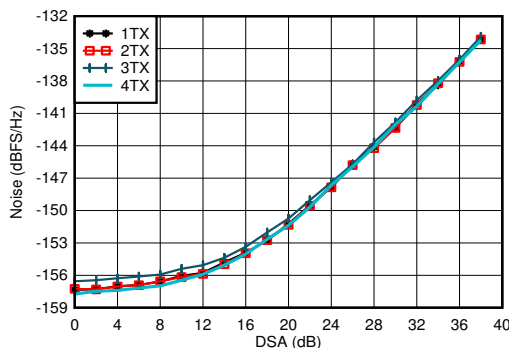
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-94. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



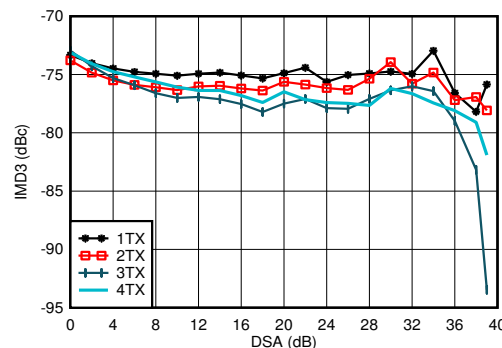
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, channel with the median variation over DSA setting at 25°C
Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-95. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, matching at 2.6 GHz, $P_{\text{OUT}} = -13$ dBFS

Figure 7-96. TX Output Noise vs Channel and Attenuation at 2.6 GHz

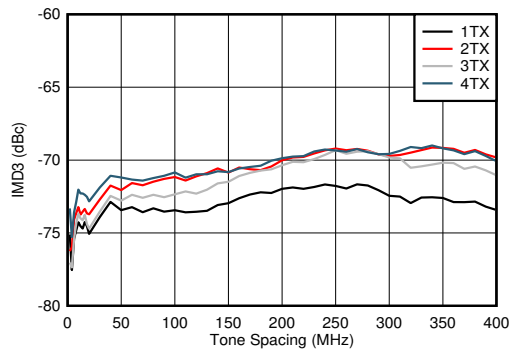


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-97. TX IMD3 vs DSA Setting at 2.6 GHz

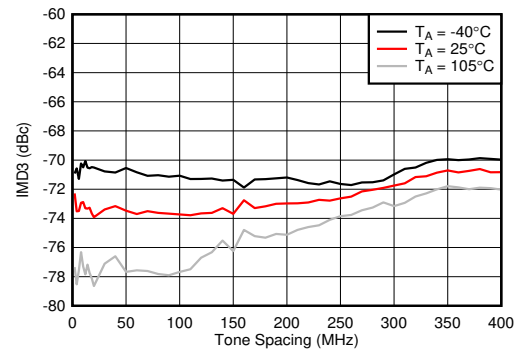
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



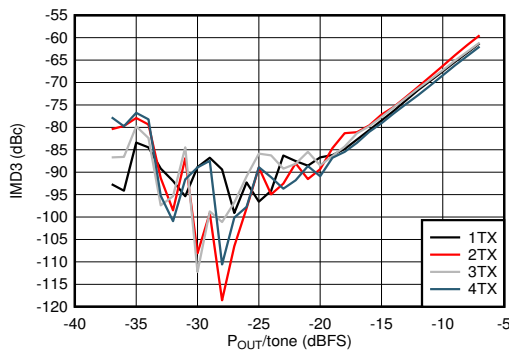
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-98. TX IMD3 vs Tone Spacing and Channel at 2.6 GHz



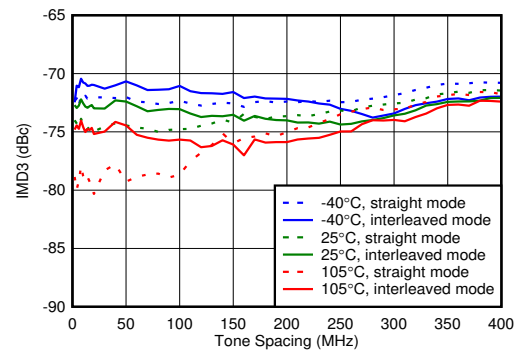
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz, matching at 2.6 GHz, -13 dBFS each tone, worst channel.

Figure 7-99. TX IMD3 vs Tone Spacing and Temperature at 2.6 GHz



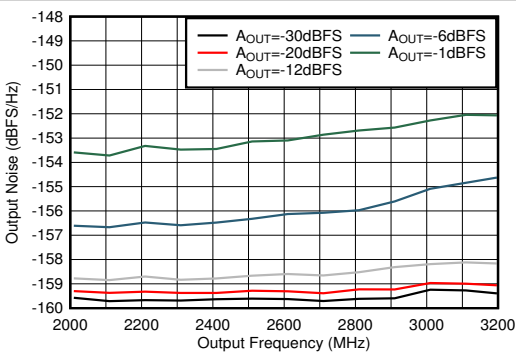
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz, $f_{\text{SPACING}} = 20$ MHz, matching at 2.6 GHz

Figure 7-100. TX IMD3 vs Digital Level at 2.6 GHz



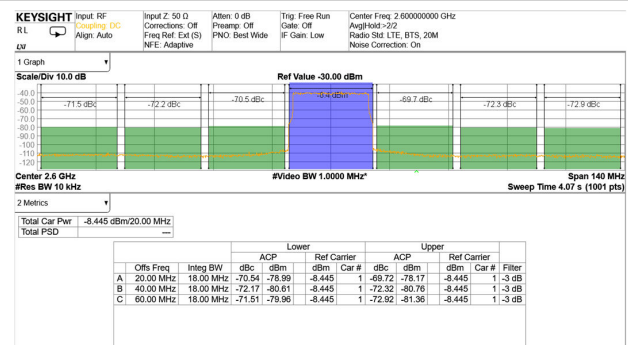
$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, $f_{\text{CENTER}} = 2.6$ GHz, matching at 2.6 GHz, -13 dBFS each tone

Figure 7-101. TX IMD3 vs Tone Spacing and Temperature



Matching at 2.6 GHz, Single tone, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, 40-MHz offset

Figure 7-102. TX Single Tone Output Noise vs Frequency and Amplitude at 2.6 GHz

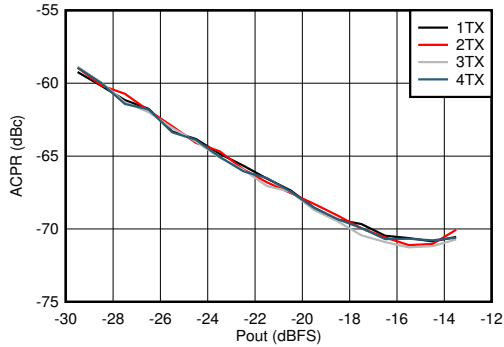


TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

Figure 7-103. TX 20-MHz LTE Output Spectrum at 2.6 GHz (Band 41)

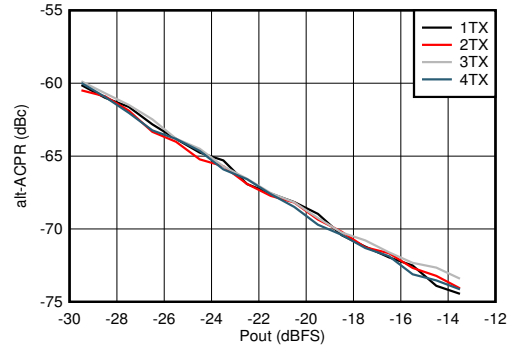
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, TX Clock Dither Enabled



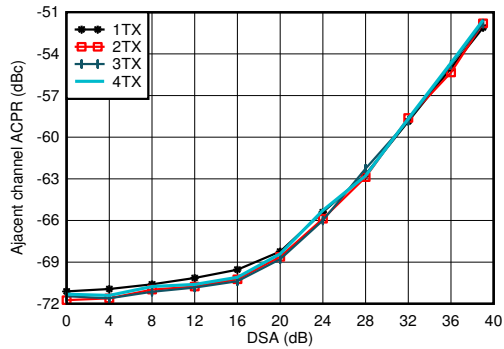
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-104. TX 20-MHz LTE ACPR vs Digital Level at 2.6 GHz



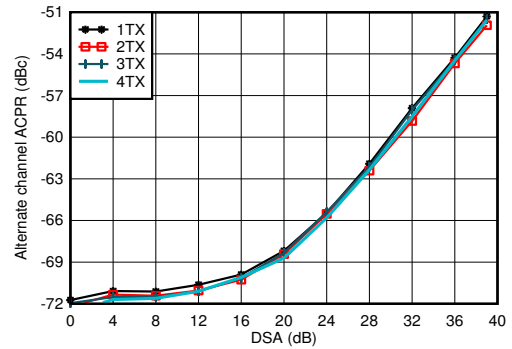
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-105. TX 20-MHz LTE alt-ACPR vs Digital Level at 2.6 GHz



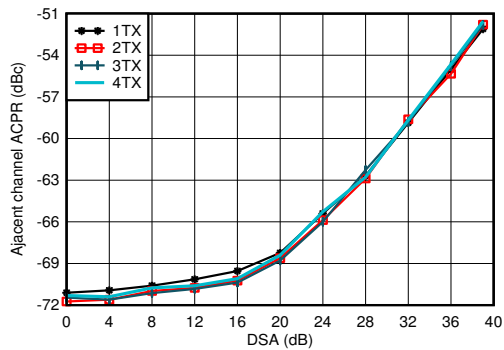
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-106. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz



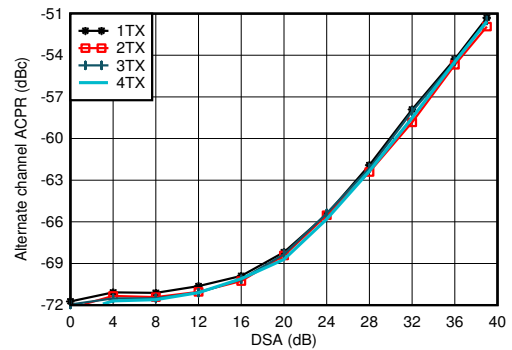
Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-107. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz



Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-108. TX 20-MHz LTE ACPR vs DSA at 2.6 GHz

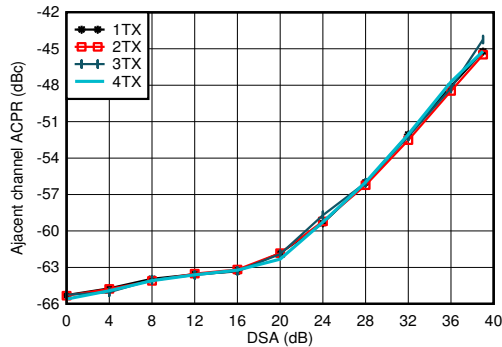


Matching at 2.6 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-109. TX 20-MHz LTE alt-ACPR vs DSA at 2.6 GHz

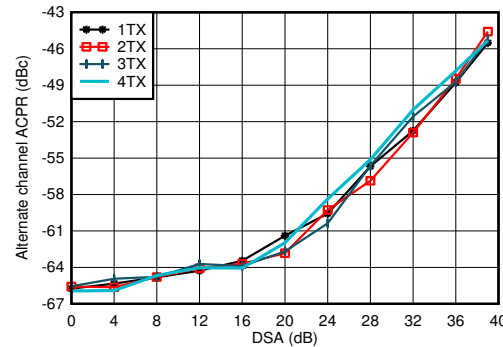
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, $\text{Sin}(x)/x$ enabled, DSA calibrated, TX Clock Dither Enabled



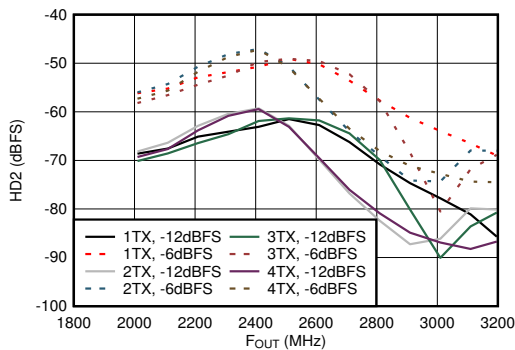
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-110. TX 100-MHz NR ACPR vs DSA at 2.6 GHz



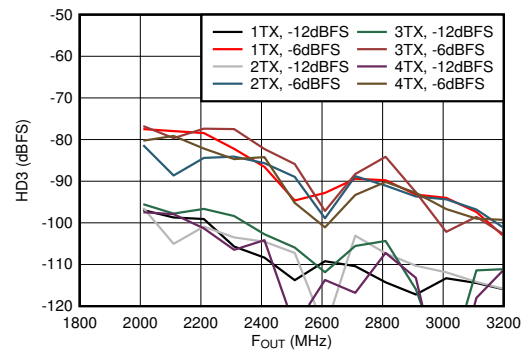
Matching at 2.6 GHz, single carrier 100-MHz BW TM1.1 NR

Figure 7-111. TX 100-MHz NR alt-ACPR vs DSA at 2.6 GHz



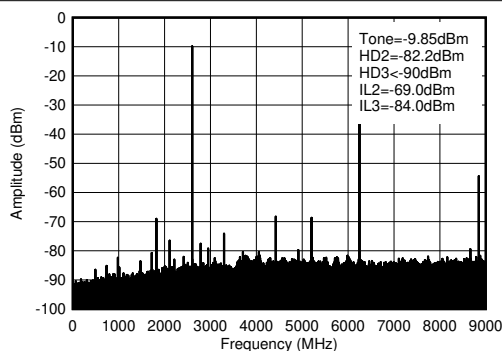
Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-112. TX HD2 vs Digital Amplitude and Output Frequency at 2.6 GHz



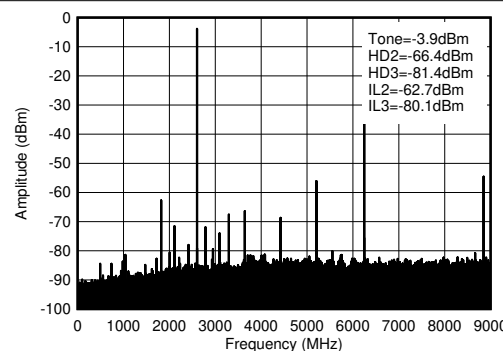
Matching at 2.6 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-113. TX HD3 vs Digital Amplitude and Output Frequency at 2.6 GHz



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-114. TX Single Tone (-12 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)

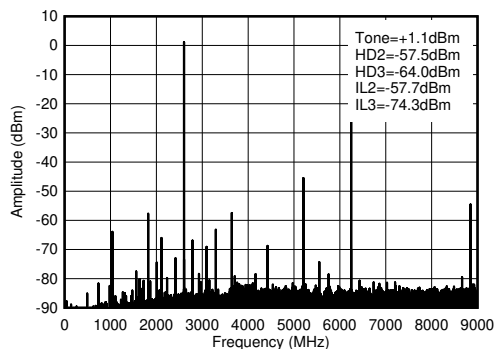


$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-115. TX Single Tone (-6 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)

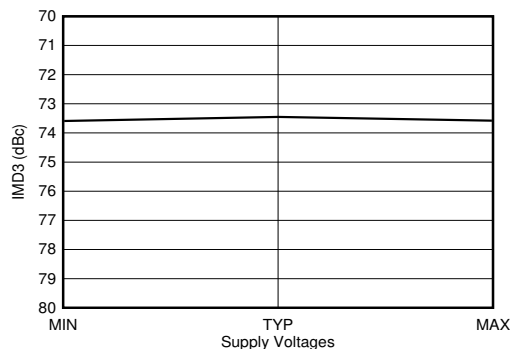
7.12.3 TX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 8847.36$ MSPS, straight mode, 2.6 GHz matching, includes PCB and cable losses. $\text{ILn} = f_{\text{S}}/n \pm f_{\text{OUT}}$ and is due to mixing with digital clocks.

Figure 7-116. TX Single Tone (-1 dBFS) Output Spectrum at 2.6 GHz ($0-f_{\text{DAC}}$)

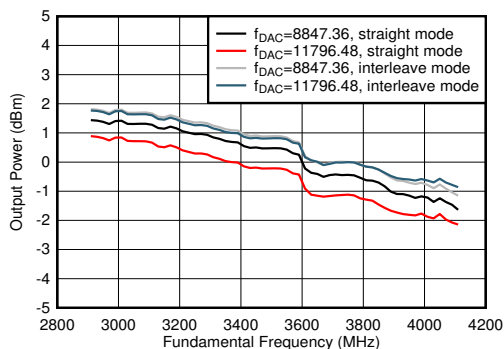


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 2.6 GHz matching. 40-MHz offset from tone. Output Power = -13 dBFS. All supplies simultaneously at MIN, TYP, or MAX voltages.

Figure 7-117. TX IMD3 vs Supply Voltage at 2.6 GHz

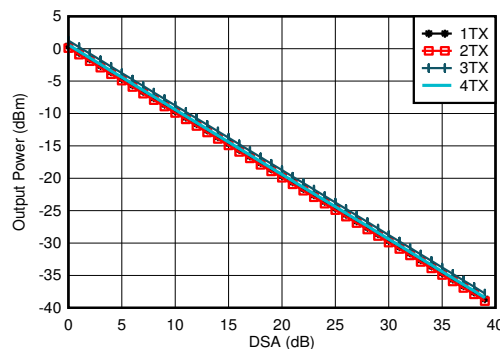
7.12.4 TX Typical Characteristics at 3.5 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



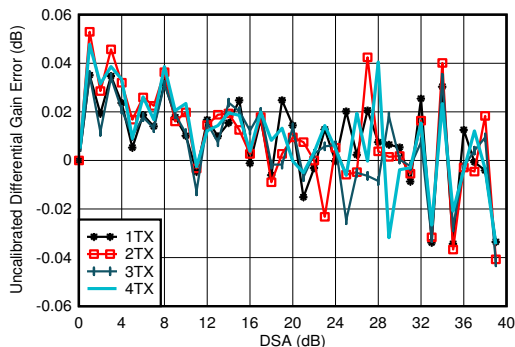
$A_{\text{out}} = -0.5$ dBFS, 3.5 GHz Matching, included PCB and cable losses

Figure 7-118. TX Output Power vs Frequency



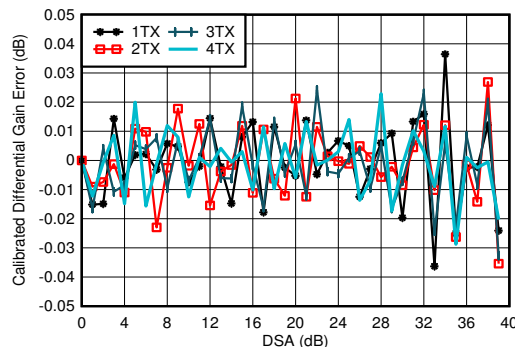
$A_{\text{out}} = -0.5$ dBFS, 3.5 GHz Matching, included PCB and cable losses

Figure 7-119. TX Output Power vs DSA Setting at 3.5 GHz



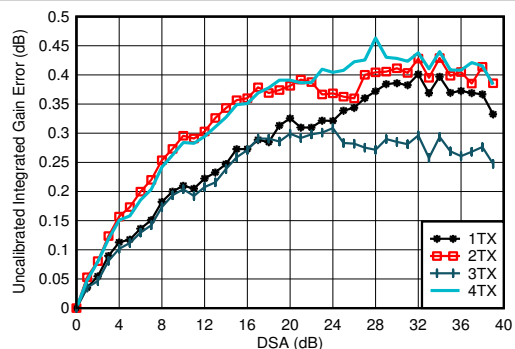
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-120. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



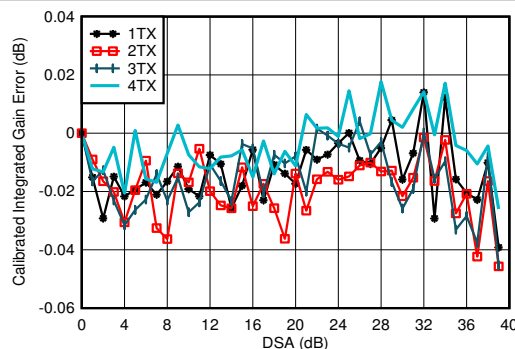
3.5 GHz Matching, included PCB and cable losses
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-121. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-122. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

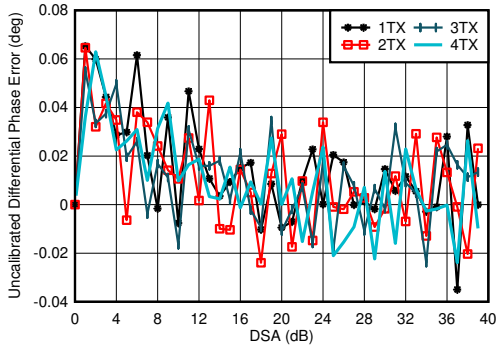


3.5 GHz Matching, included PCB and cable losses
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-123. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 3.5 GHz

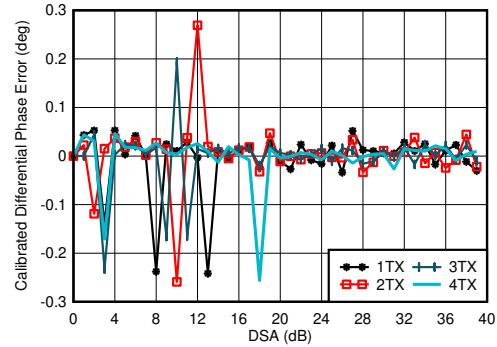
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



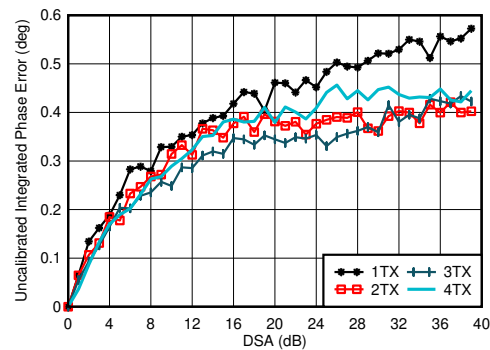
3.5 GHz Matching, included PCB and cable losses

Figure 7-124. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



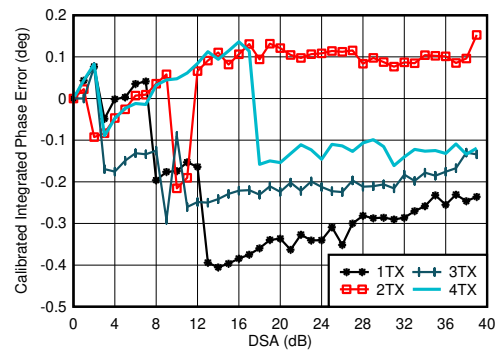
3.5 GHz Matching, included PCB and cable losses
Phase DNL spike may occur at any DSA setting.

Figure 7-125. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 3.5 GHz



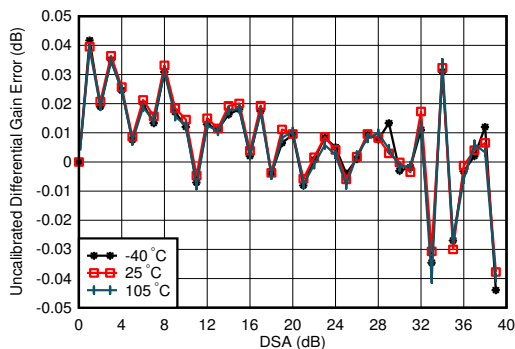
3.5 GHz Matching, included PCB and cable losses

Figure 7-126. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



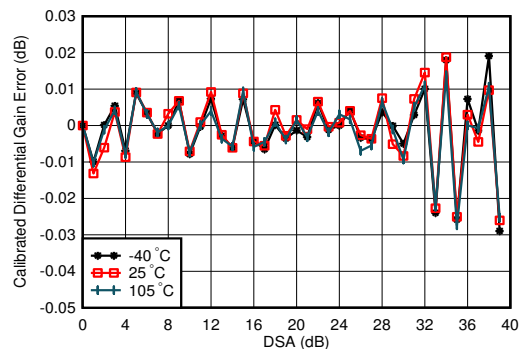
3.5 GHz Matching, included PCB and cable losses

Figure 7-127. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 3.5 GHz



3.5 GHz Matching, 1TX

Figure 7-128. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

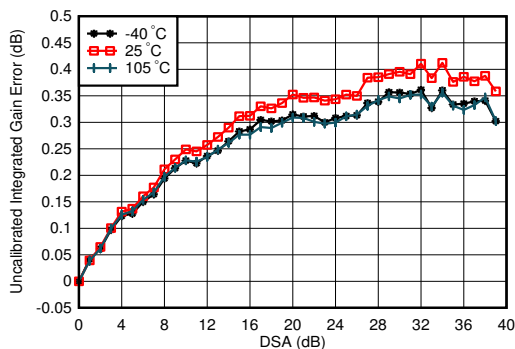


3.5 GHz Matching, 1TX, Calibrated at 25°C

Figure 7-129. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 3.5 GHz

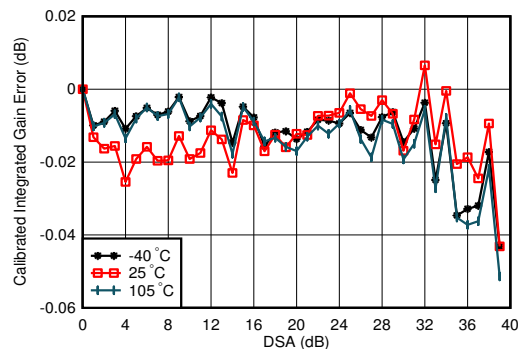
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



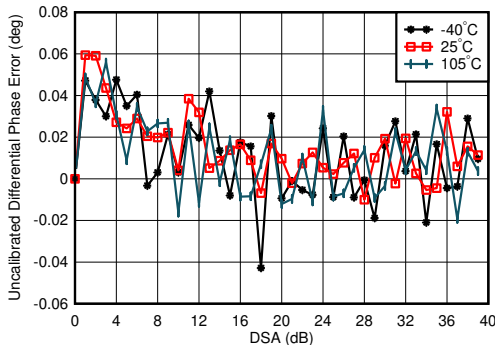
3.5 GHz Matching, 1TX

Figure 7-130. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

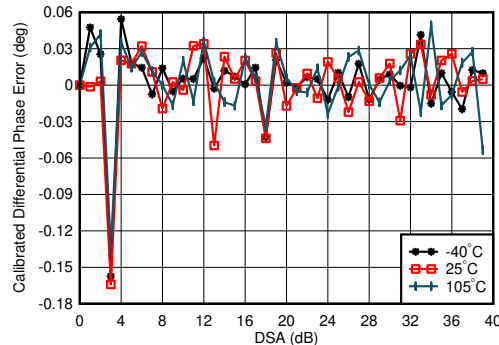
Figure 7-131. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

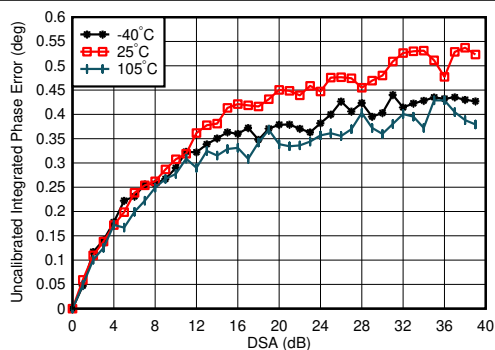
Figure 7-132. TX Uncalibrated Differential Phase Error vs DSA setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX, Calibrated at 25°C

$$\text{Differential Phase Error} = \text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$$

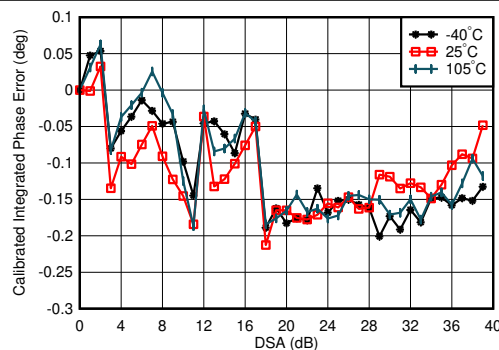
Figure 7-133. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 3.5 GHz



3.5 GHz Matching, 1TX

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-134. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz



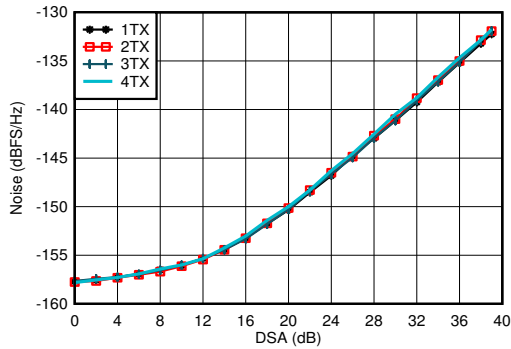
3.5 GHz Matching, 1TX, Calibrated at 25°C

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-135. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 3.5 GHz

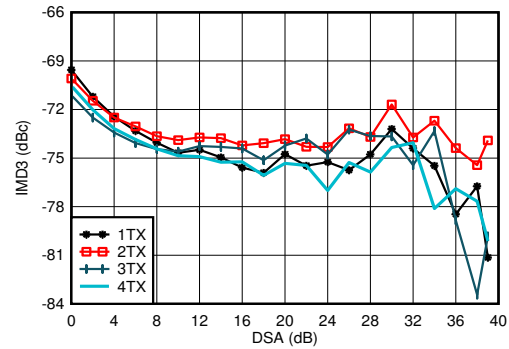
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



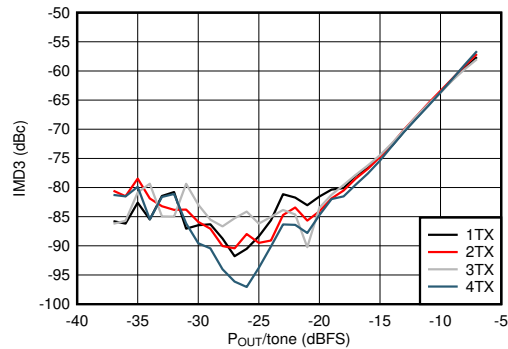
A. $f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 3.5 GHz, $A_{\text{out}} = -13$ dBFS.

Figure 7-136. TX NSD vs DSA Setting at 3.5 GHz



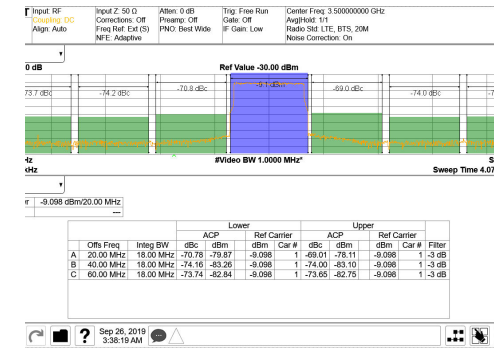
20-MHz tone spacing, 3.5 GHz Matching, -13 dBFS each tone, included PCB and cable losses

Figure 7-137. TX IMD3 vs DSA Setting at 3.5 GHz



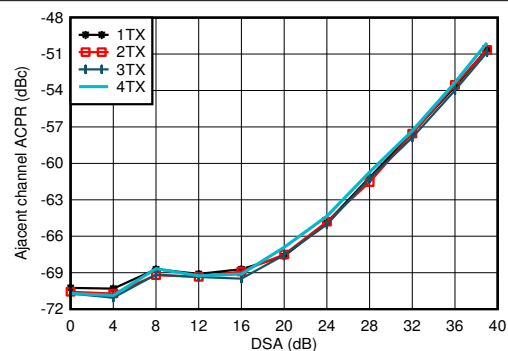
20-MHz tone spacing, 3.5 GHz Matching

Figure 7-138. TX IMD3 vs Digital Amplitude and Channel at 3.5 GHz



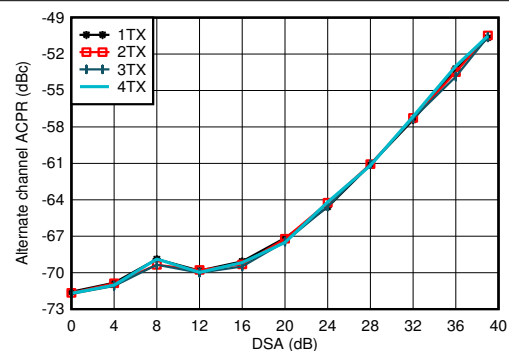
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-139. TX 20-MHz LTE Output Spectrum at 3.5 GHz (Band 42)



3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-140. TX 20-MHz LTE ACPR vs DSA Setting at 3.5 GHz

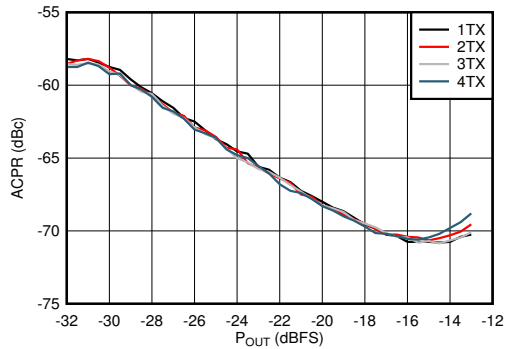


3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-141. TX 20-MHz LTE alt-ACPR vs DSA Setting at 3.5 GHz

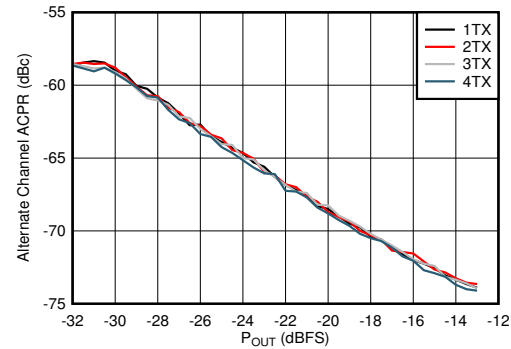
7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



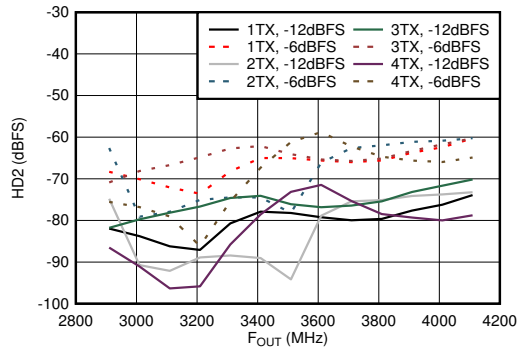
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-142. TX 20-MHz LTE ACPR vs Digital Level at 3.5 GHz



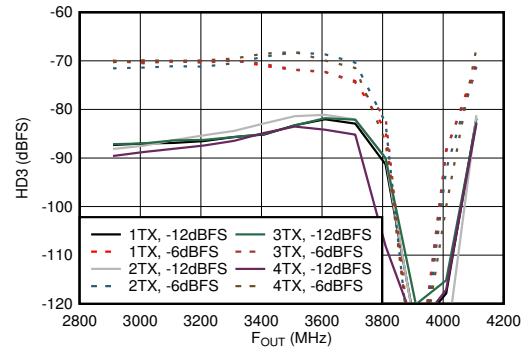
3.5 GHz Matching, single carrier 20-MHz BW TM1.1 LTE

Figure 7-143. TX 20-MHz LTE alt-ACPR vs Digital Level at 3.5 GHz



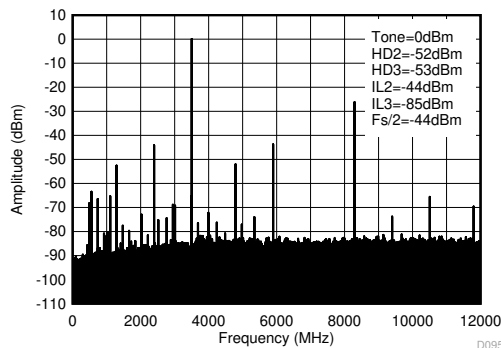
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-144. TX Single Tone HD2 vs Frequency and Digital Level at 3.5 GHz



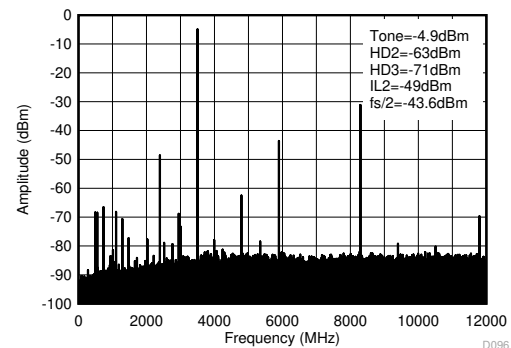
Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode, normalized to output power at harmonic frequency. Dip is due to HD3 falling near DC.

Figure 7-145. TX Single Tone HD3 vs Frequency and Digital Level at 3.5 GHz



Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

Figure 7-146. TX Single Tone (-1 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

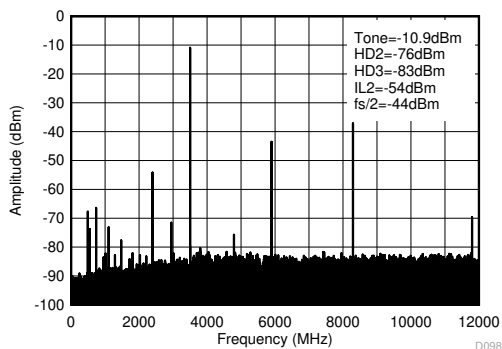


Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

Figure 7-147. TX Single Tone (-6 dBFS) Output Spectrum at 3.5 GHz (0 - f_{DAC})

7.12.4 TX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled

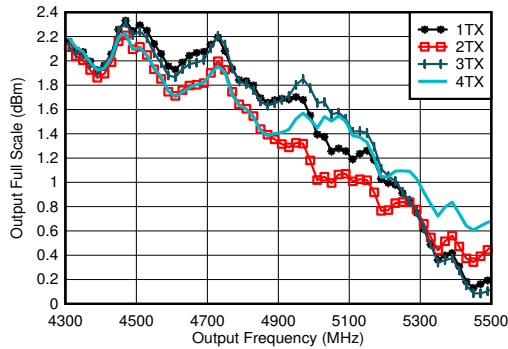


Matching at 3.5 GHz, $f_{\text{DAC}} = 11.79648$ GSPS, interleave mode.

Figure 7-148. TX Single Tone (-12 dBFS) Output Spectrum at 3.5 GHz (0- f_{DAC})

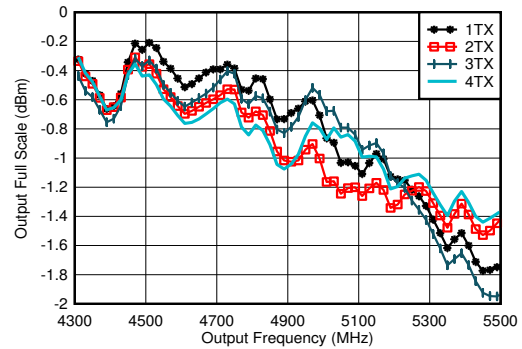
7.12.5 TX Typical Characteristics at 4.9 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



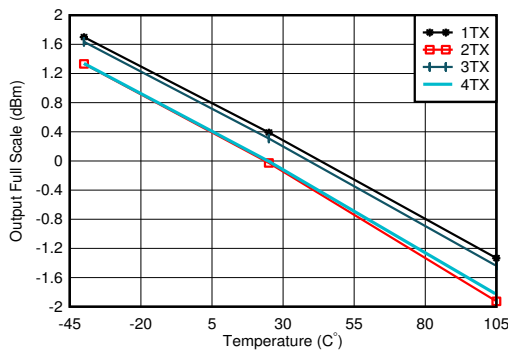
Excluding PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 4.9 GHz matching

Figure 7-149. TX Full Scale vs RF Frequency and Channel at 11796.48 MSPS



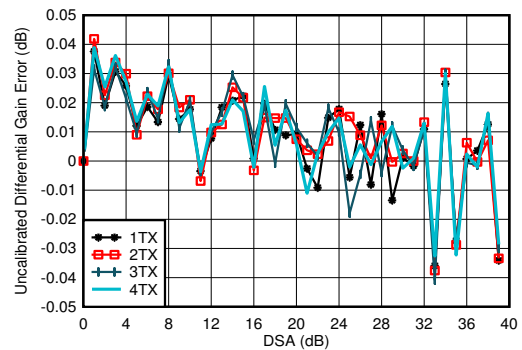
Excluding PCB and cable losses, $A_{\text{out}} = -0.5$ dBFS, DSA = 0, 4.9 GHz matching

Figure 7-150. TX Full Scale vs RF Frequency and Channel at 5898.24 MSPS, Straight Mode, 2nd Nyquist Zone



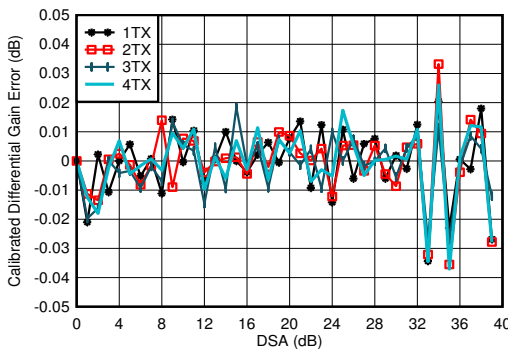
$f_{\text{DAC}} = 11796.48$ MSPS, $A_{\text{out}} = -0.5$ dBFS, matching 4.9 GHz

Figure 7-151. TX Output Power vs DSA Setting and Channel at 4.9 GHz



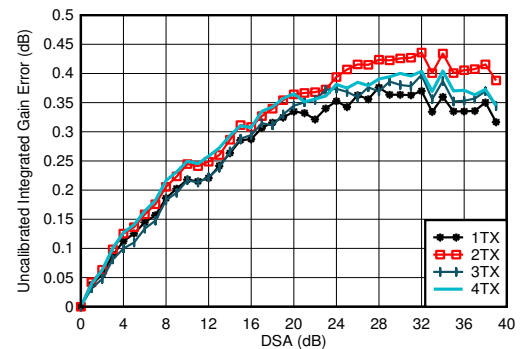
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-152. TX Uncalibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-153. TX Calibrated Differential Gain Error vs DSA Setting and Channel at 4.9 GHz

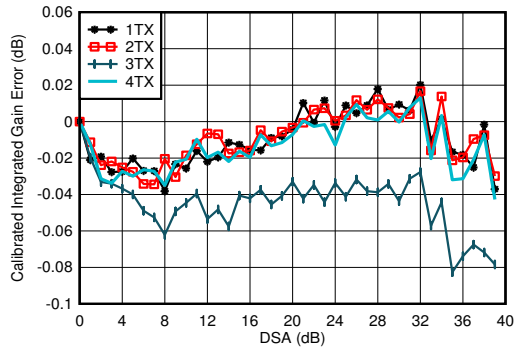


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-154. TX Uncalibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz

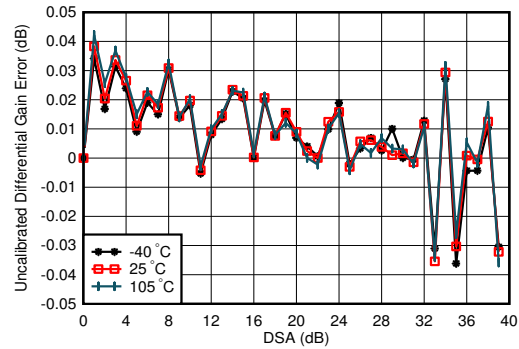
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



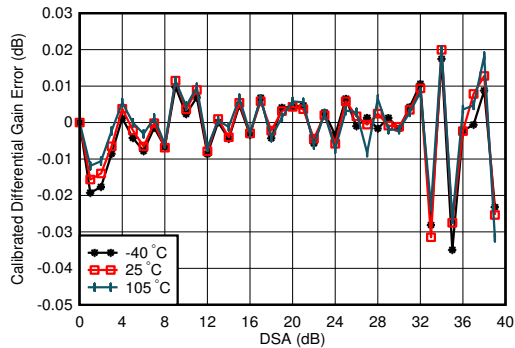
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-155. TX Calibrated Integrated Gain Error vs DSA Setting and Channel at 4.9 GHz



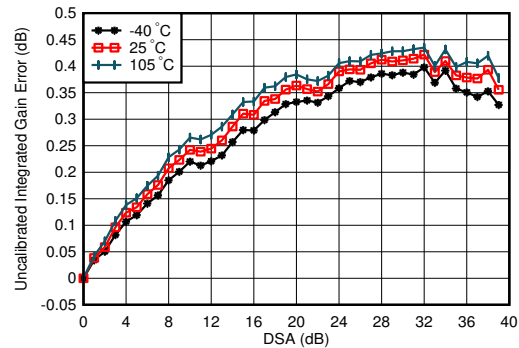
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-156. TX Uncalibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Gain Error = $P_{\text{OUT}}(\text{DSA Setting} - 1) - P_{\text{OUT}}(\text{DSA Setting}) + 1$

Figure 7-157. TX Calibrated Differential Gain Error vs DSA Setting and Temperature at 4.9 GHz

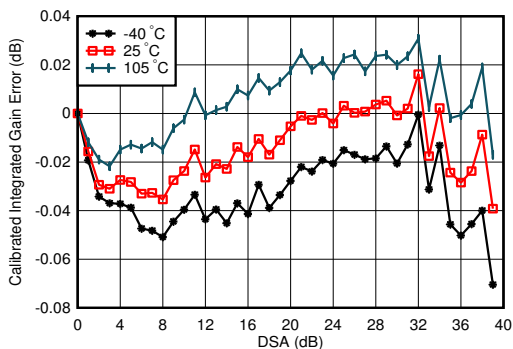


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-158. TX Uncalibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz

7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

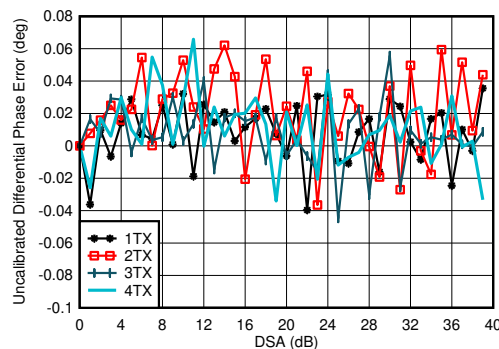
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Integrated Gain Error = $P_{\text{OUT}}(\text{DSA Setting}) - P_{\text{OUT}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

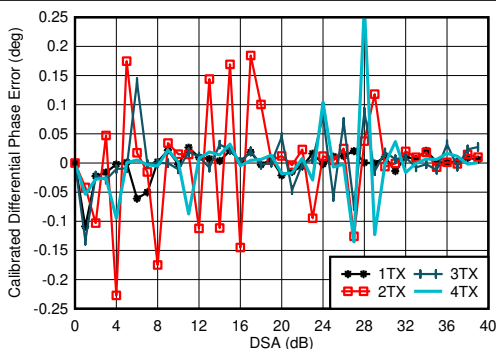
Figure 7-159. TX Calibrated Integrated Gain Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Figure 7-160. TX Uncalibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz

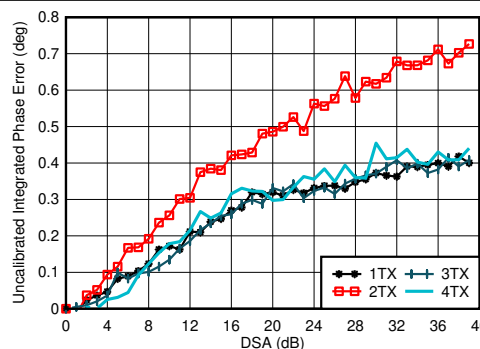


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Differential Phase Error = $\text{Phase}_{\text{OUT}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{OUT}}(\text{DSA Setting})$

Phase DNL spike may occur at any DSA setting.

Figure 7-161. TX Calibrated Differential Phase Error vs DSA Setting and Channel at 4.9 GHz



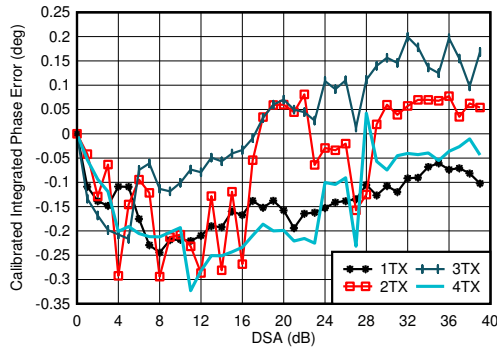
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-162. TX Uncalibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz

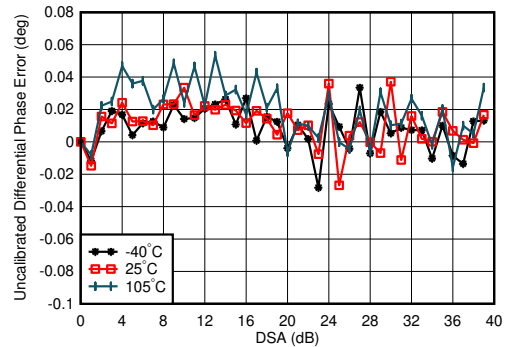
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



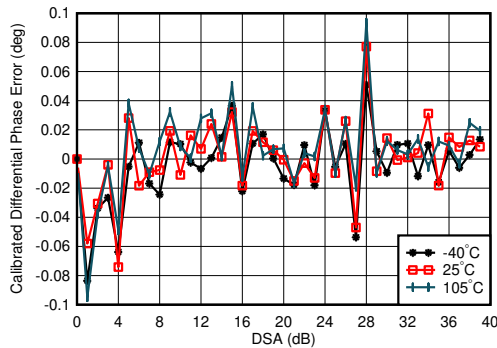
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-163. TX Calibrated Integrated Phase Error vs DSA Setting and Channel at 4.9 GHz



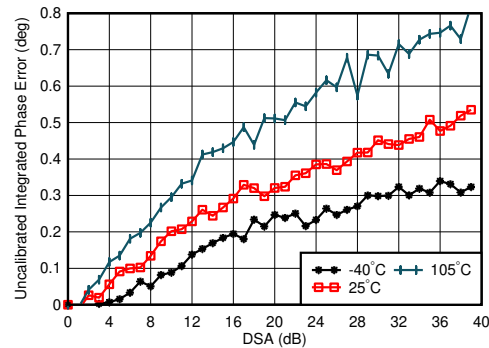
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

Figure 7-164. TX Uncalibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Differential Phase Error = Phase_{OUT}(DSA Setting – 1) – Phase_{OUT}(DSA Setting)

Figure 7-165. TX Calibrated Differential Phase Error vs DSA Setting and Temperature at 4.9 GHz

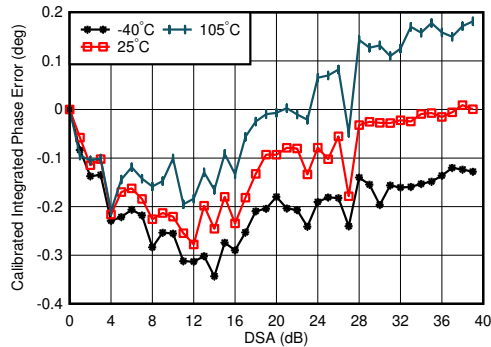


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-166. TX Uncalibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz

7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

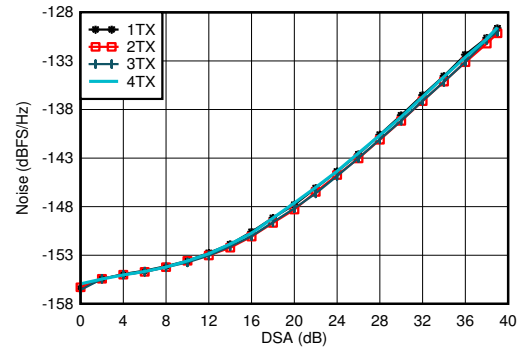
Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, TX Clock Dither Enabled



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, channel with the median variation over DSA setting at 25°C

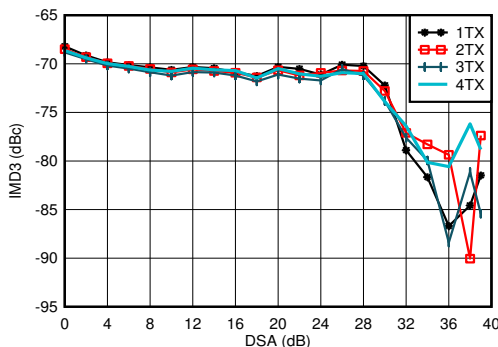
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-167. TX Calibrated Integrated Phase Error vs DSA Setting and Temperature at 4.9 GHz



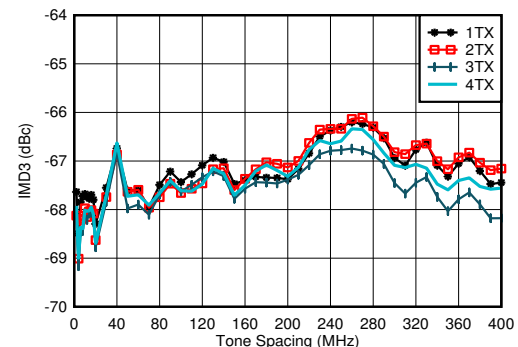
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $P_{\text{OUT}} = -13$ dBFS

Figure 7-168. TX Output Noise vs Channel and Attenuation at 2.6 GHz



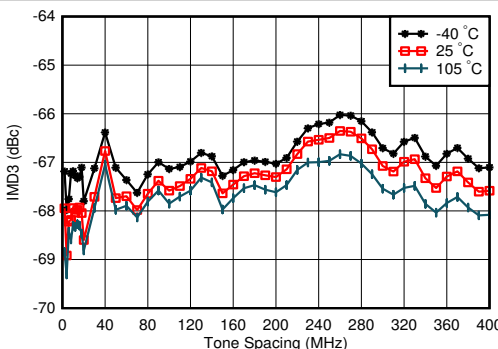
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9$ GHz, -13 dBFS each tone

Figure 7-169. TX IMD3 vs DSA Setting at 4.9 GHz



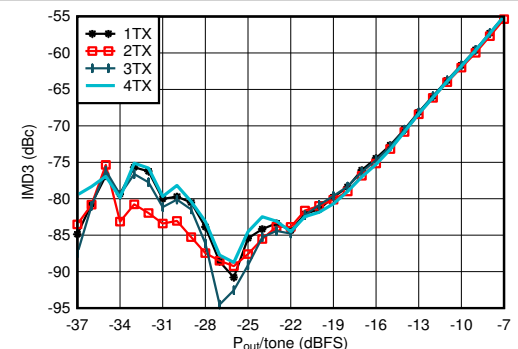
$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9$ GHz, -13 dBFS each tone

Figure 7-170. TX IMD3 vs Tone Spacing and Channel at 4.9 GHz



$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9$ GHz, -13 dBFS each tone, worst channel

Figure 7-171. TX IMD3 vs Tone Spacing and Temperature at 4.9 GHz

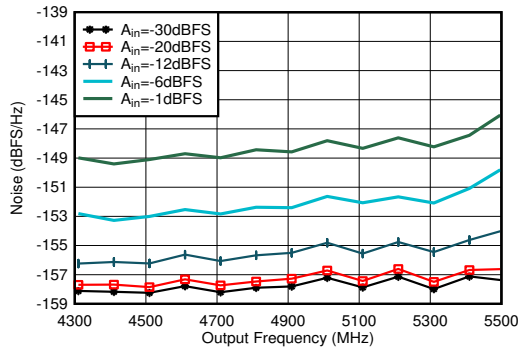


$f_{\text{DAC}} = 11796.48$ MSPS, interleaved mode, matching at 4.9 GHz, $f_{\text{CENTER}} = 4.9$ GHz, $f_{\text{SPACING}} = 20$ MHz

Figure 7-172. TX IMD3 vs Digital Level at 4.9 GHz

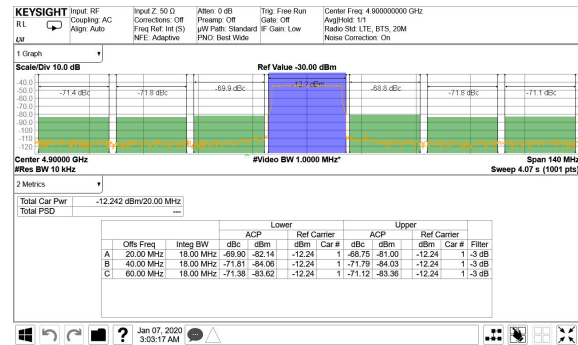
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



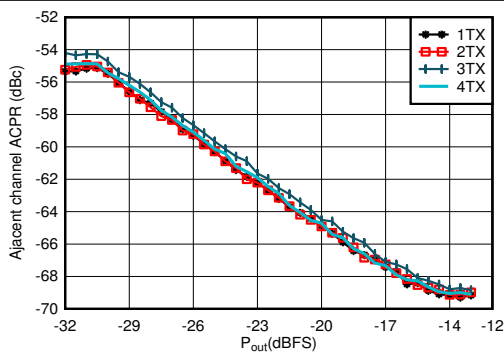
Matching at 4.9 GHz, Single tone, $f_{\text{DAC}} = 11.7964$ 8GSPS, interleave mode, 40-MHz offset, DSA=0dB

Figure 7-173. TX Single Tone Output Noise vs Frequency and Amplitude at 4.9 GHz



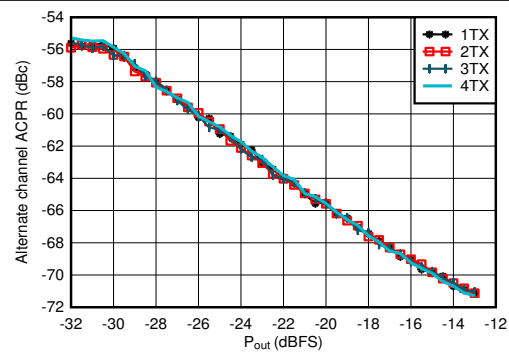
TM1.1, $P_{\text{OUT_RMS}} = -13$ dBFS

Figure 7-174. TX 20-MHz LTE Output Spectrum at 4.9 GHz



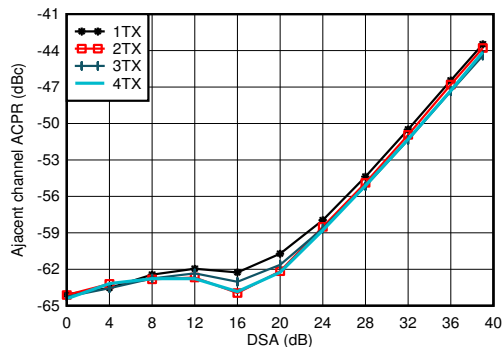
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-175. TX 20-MHz LTE ACPR vs Digital Level at 4.9 GHz



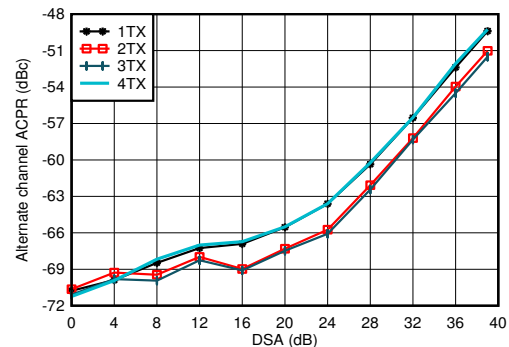
Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-176. TX 20-MHz LTE alt-ACPR vs Digital Level at 4.9 GHz



Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-177. TX 20-MHz LTE ACPR vs DSA at 4.9 GHz

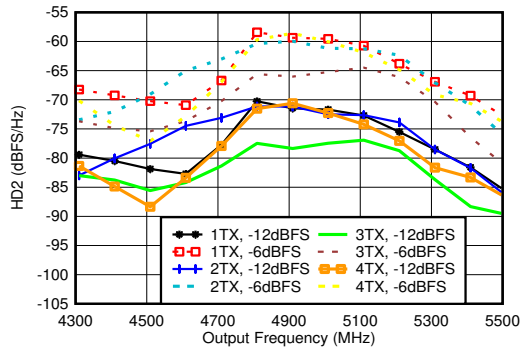


Matching at 4.9 GHz, single carrier 20-MHz BW TM1.1 LTE

Figure 7-178. TX 20-MHz LTE alt-ACPR vs DSA at 4.9 GHz

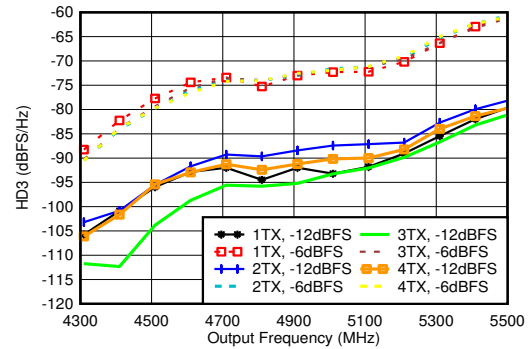
7.12.5 TX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), interleave mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled



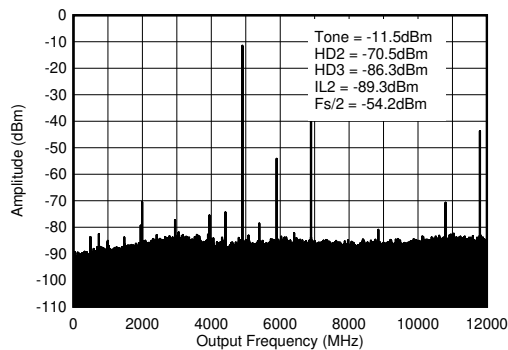
Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-179. TX HD2 vs Digital Amplitude and Output Frequency at 4.9 GHz



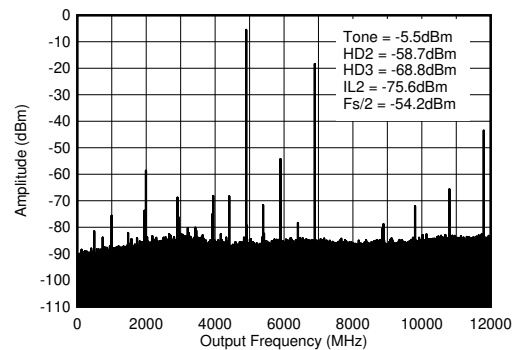
Matching at 4.9 GHz, $f_{\text{DAC}} = 11.79648$ GSPPS, interleave mode, normalized to output power at harmonic frequency

Figure 7-180. TX HD3 vs Digital Amplitude and Output Frequency at 4.9 GHz



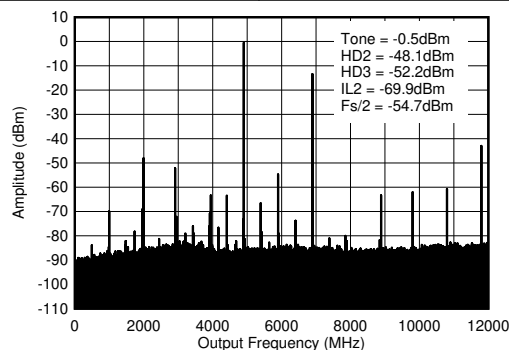
$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-181. TX Single Tone (-12 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)



$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-182. TX Single Tone (-6 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)

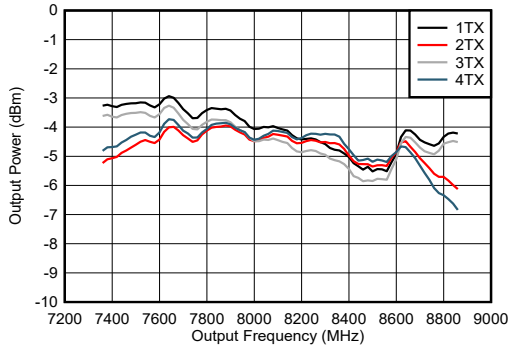


$f_{\text{DAC}} = 11796.48$ MSPS, interleave mode, 4.9 GHz matching, includes PCB and cable losses. $\text{ILn} = f_s/n \pm f_{\text{OUT}}$.

Figure 7-183. TX Single Tone (-1 dBFS) Output Spectrum at 4.9 GHz ($0-f_{\text{DAC}}$)

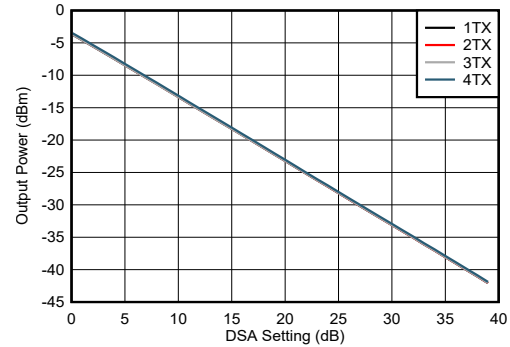
7.12.6 TX Typical Characteristics at 8.1 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



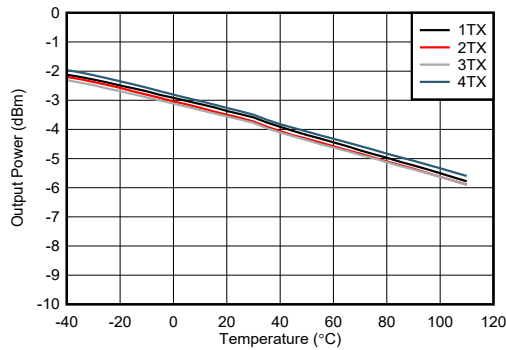
includes PCB and cable losses.

Figure 7-184. TX Output Power vs Frequency at 8.11 GHz



includes PCB and cable losses.

Figure 7-185. TX Output Power vs DSA Setting at 8.11 GHz



includes PCB and cable losses.

Figure 7-186. TX Output Power vs Temperature at 8.11 GHz

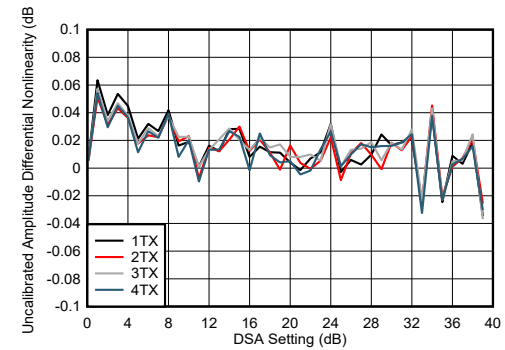


Figure 7-187. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

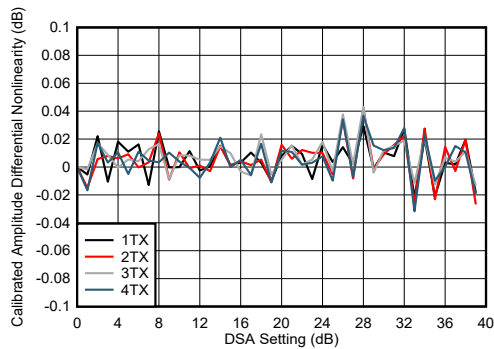


Figure 7-188. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

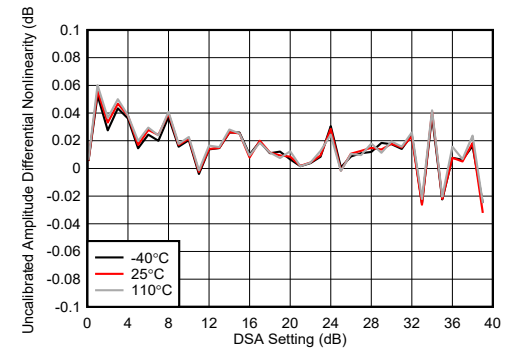


Figure 7-189. TX DSA Uncalibrated Amplitude Differential Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

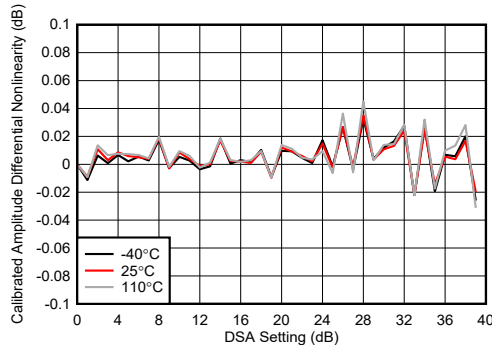


Figure 7-190. TX DSA Calibrated Amplitude Differential Nonlinearity at 8.11 GHz

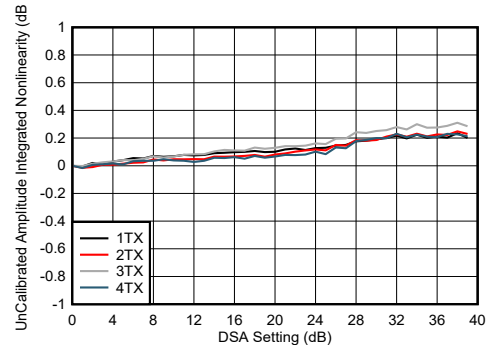


Figure 7-191. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

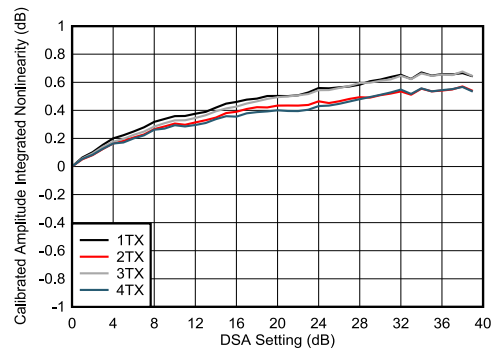


Figure 7-192. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

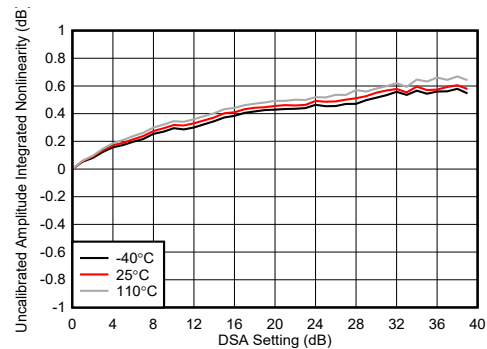


Figure 7-193. TX DSA Uncalibrated Amplitude Integrated Nonlinearity at 8.11 GHz

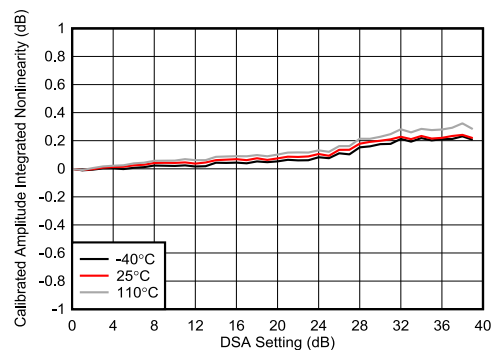


Figure 7-194. TX DSA Calibrated Amplitude Integrated Nonlinearity at 8.11 GHz

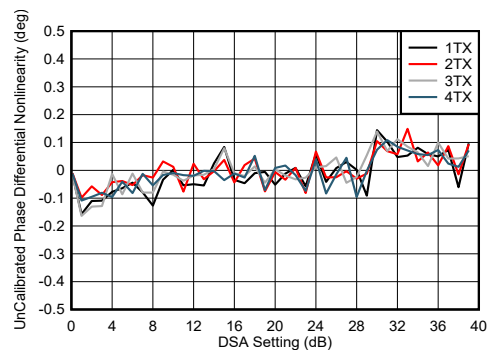


Figure 7-195. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

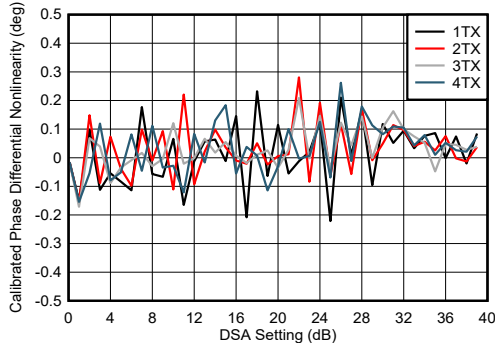


Figure 7-196. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

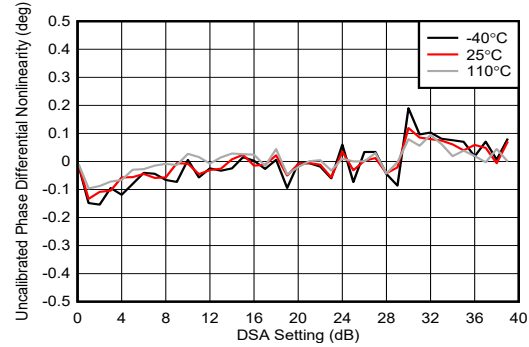


Figure 7-197. TX DSA Uncalibrated Phase Differential Nonlinearity at 8.11 GHz

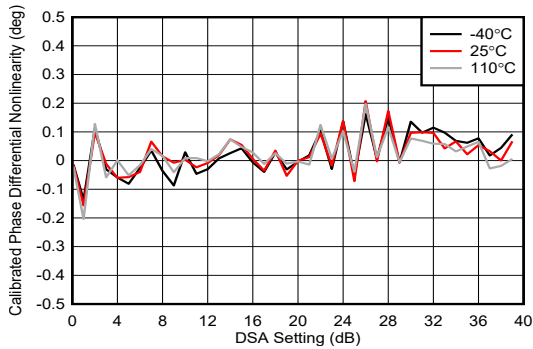


Figure 7-198. TX DSA Calibrated Phase Differential Nonlinearity at 8.11 GHz

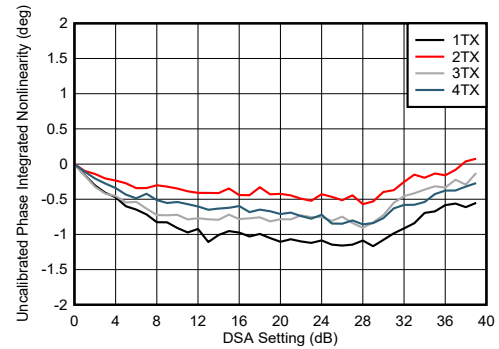


Figure 7-199. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

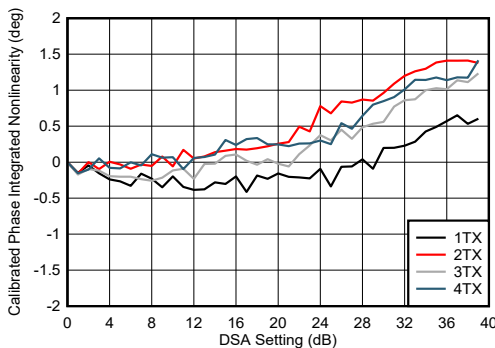


Figure 7-200. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz

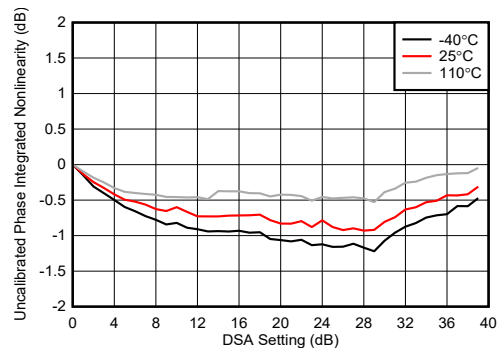


Figure 7-201. TX DSA Uncalibrated Phase Integrated Nonlinearity at 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

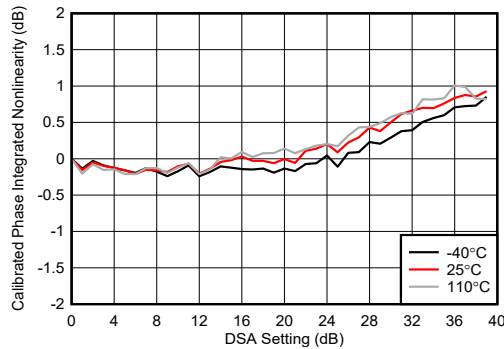
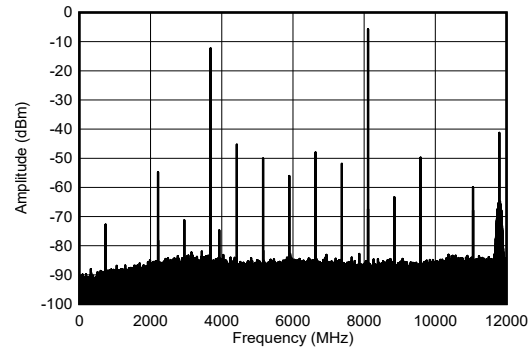
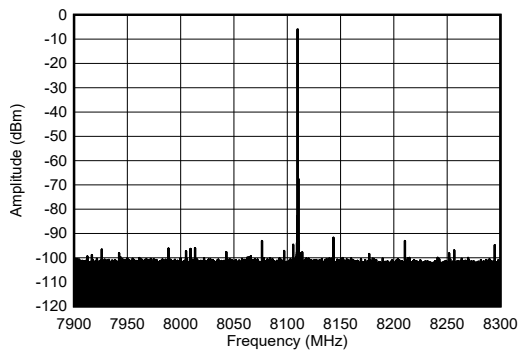


Figure 7-202. TX DSA Calibrated Phase Integrated Nonlinearity at 8.11 GHz



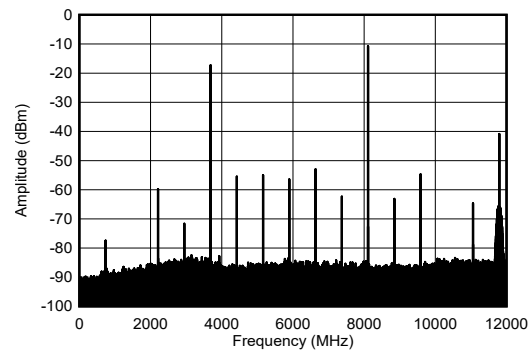
-1 dBFS

Figure 7-203. TX Single Tone Output Spectrum at 8.11 GHz



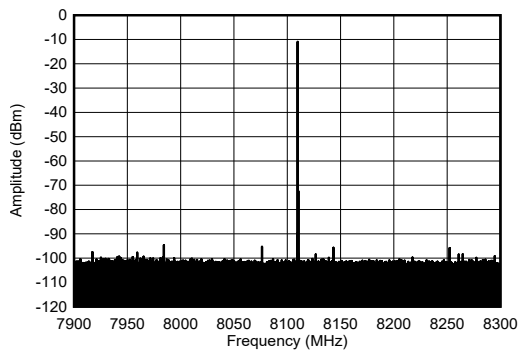
-1 dBFS

Figure 7-204. TX Single Tone Output Spectrum at 8.11 GHz



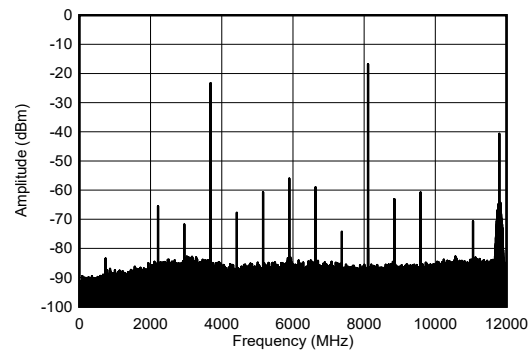
-6 dBFS

Figure 7-205. TX Single Tone Output Spectrum at 8.11 GHz



-6 dBFS

Figure 7-206. TX Single Tone Output Spectrum at 8.11 GHz

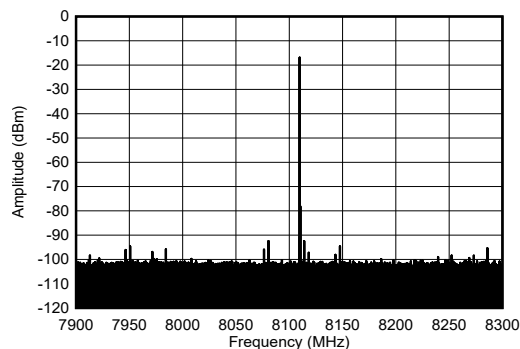


-12 dBFS

Figure 7-207. TX Single Tone Output Spectrum at 8.11 GHz

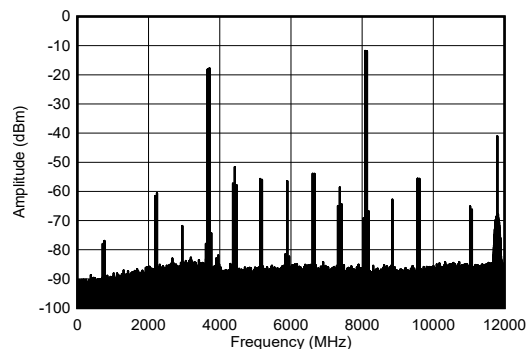
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



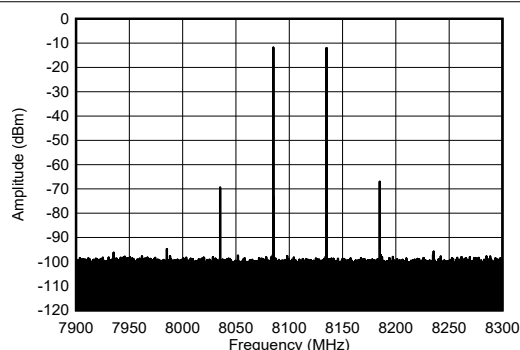
-12 dBFS

Figure 7-208. TX Single Tone Output Spectrum at 8.11 GHz



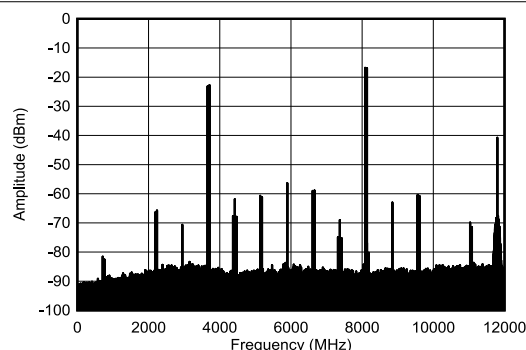
50 MHz tone spacing, -7 dBFS each tone

Figure 7-209. TX Dual Tone Output Spectrum at 8.11 GHz



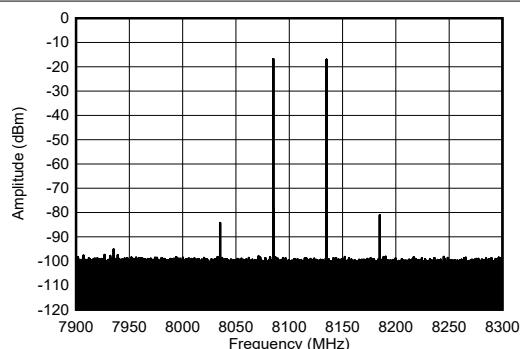
50 MHz tone spacing, -7d BFS each tone

Figure 7-210. TX Dual Tone Output Spectrum at 8.11 GHz



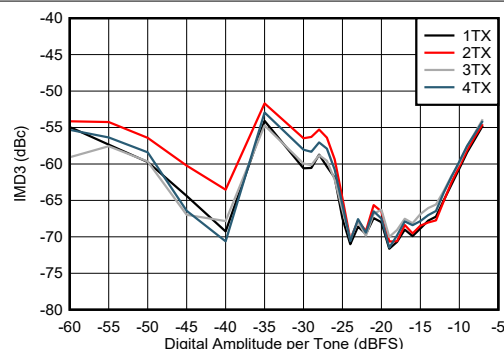
50 MHz tone spacing, -12 dBFS each tone

Figure 7-211. TX Dual Tone Output Spectrum at 8.11 GHz



50MHz tone spacing, -12dBFS each tone

Figure 7-212. TX Dual Tone Output Spectrum at 8.11 GHz

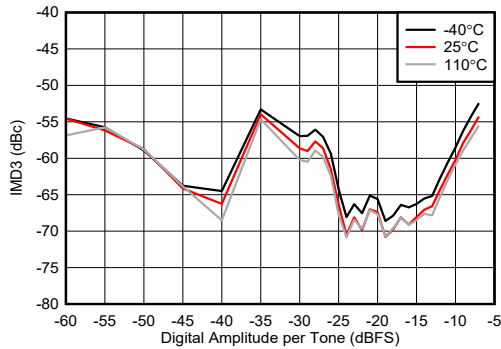


-7 dBFS each tone, 50 MHz tone spacing

Figure 7-213. TX IMD3 vs Digital Amplitude at 8.11 GHz

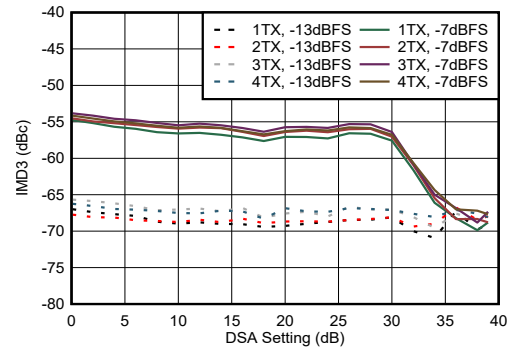
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



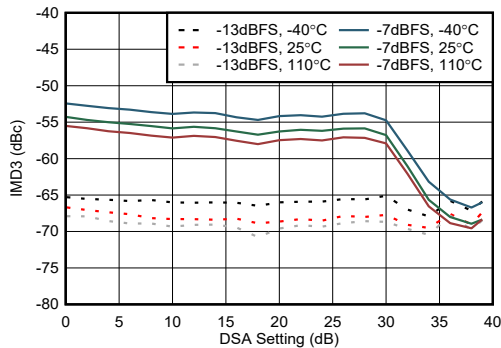
-7 dBFS each tone, 50 MHz tone spacing

Figure 7-214. TX IMD3 vs Digital Amplitude at 8.11 GHz



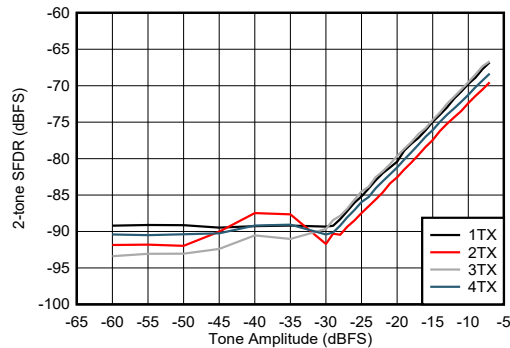
50 MHz tone spacing

Figure 7-215. TX IMD3 vs DSA Setting at 8.11 GHz



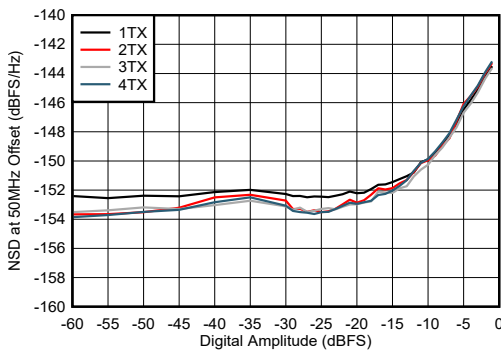
50 MHz tone spacing

Figure 7-216. TX IMD3 vs DSA Setting at 8.11 GHz



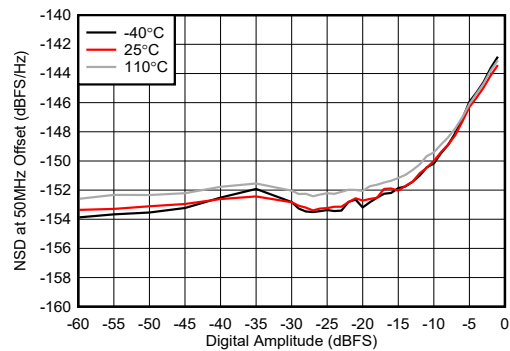
50 MHz tone spacing

Figure 7-217. TX 2-Tone SFDR vs Digital Amplitude at 8.11 GHz



50 MHz offset

Figure 7-218. TX NSD vs Digital Amplitude at 8.11 GHz

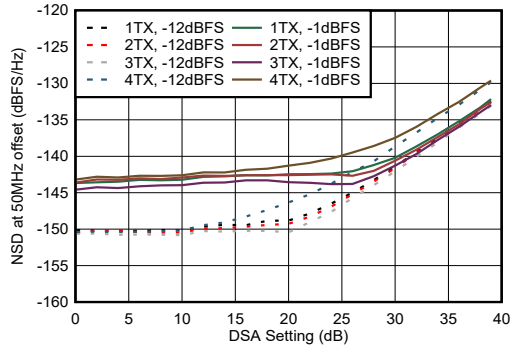


50 MHz offset

Figure 7-219. TX NSD vs Digital Amplitude at 8.11 GHz

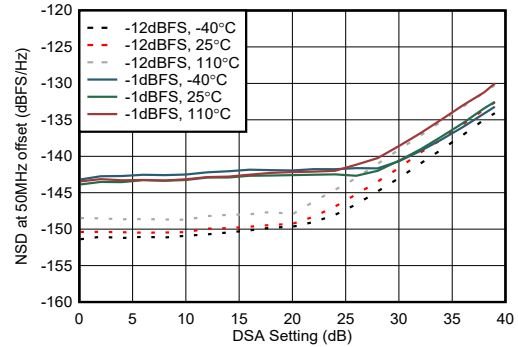
7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching



50 MHz offset

Figure 7-220. TX NSD vs DSA Setting at 8.11 GHz



50 MHz offset

Figure 7-221. TX NSD vs DSA Setting at 8.11 GHz

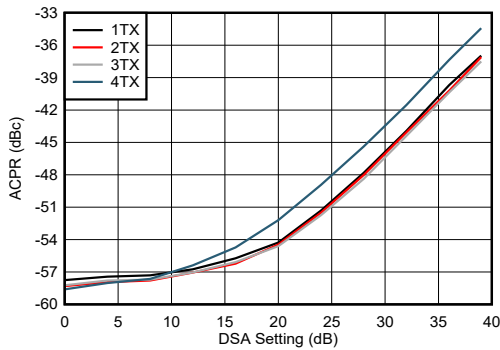


Figure 7-222. TX NR100MHz ACPR vs DSA Setting 8.11 GHz

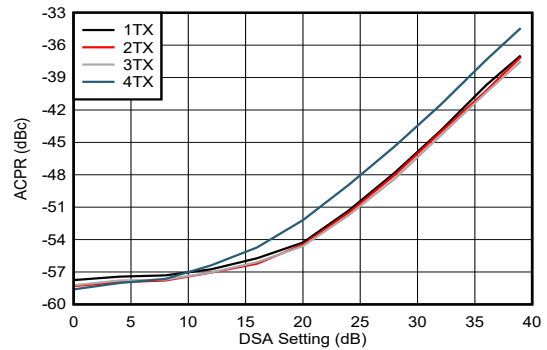


Figure 7-223. TX NR100MHz alt-ACPR vs DSA Setting 8.11 GHz

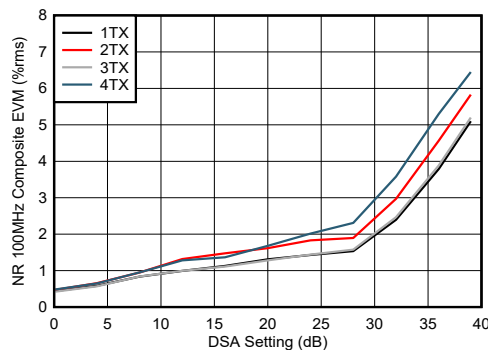


Figure 7-224. TX NR100MHz EVM vs DSA Setting 8.11 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

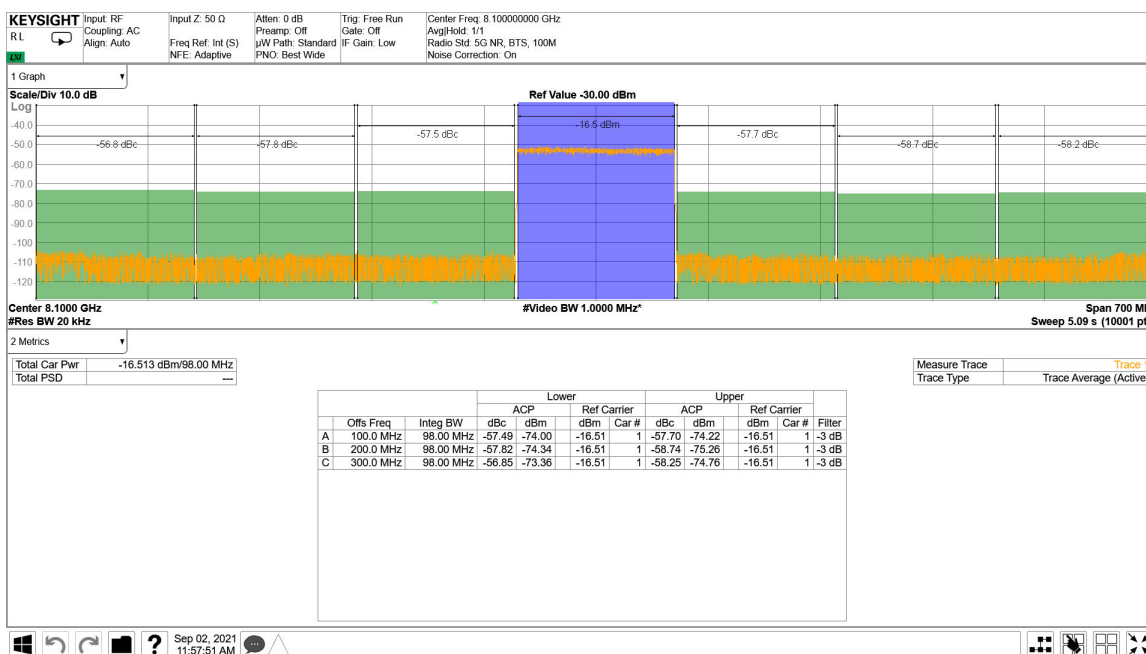


Figure 7-225. TX 100 MHz NR Output Spectrum at 8.1 GHz

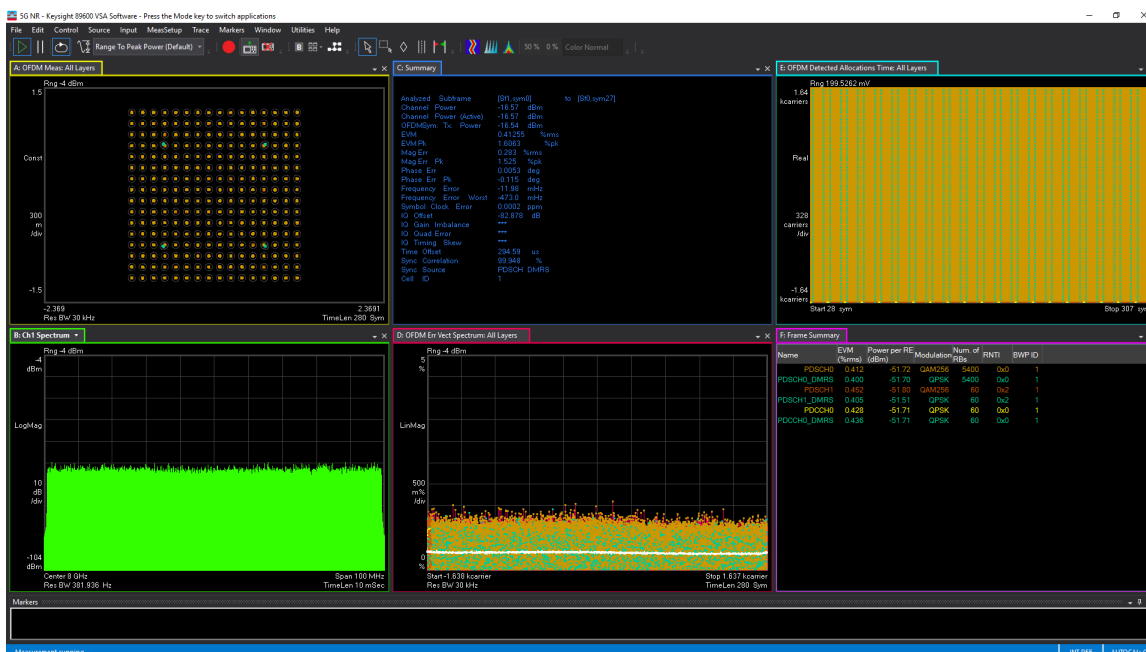


Figure 7-226. TX 100 MHz NR EVM at 8.1 GHz

7.12.6 TX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (24x interpolation), mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 8.1GHz matching

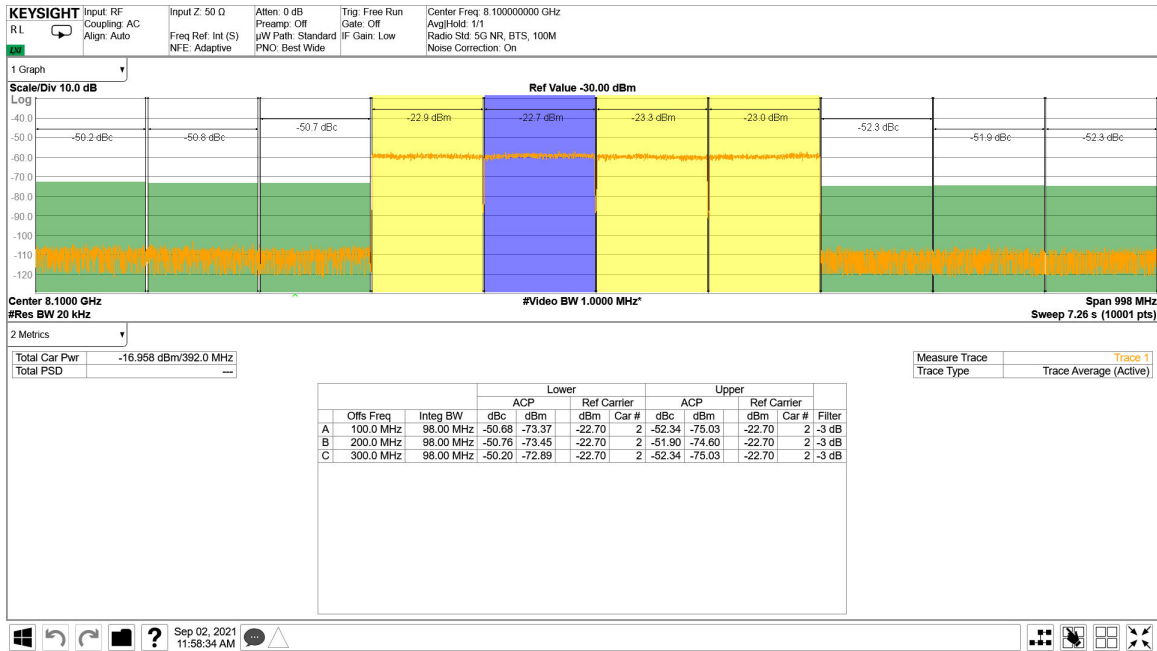


Figure 7-227. TX 4x100 MHz NR Output Spectrum 8.11 GHz

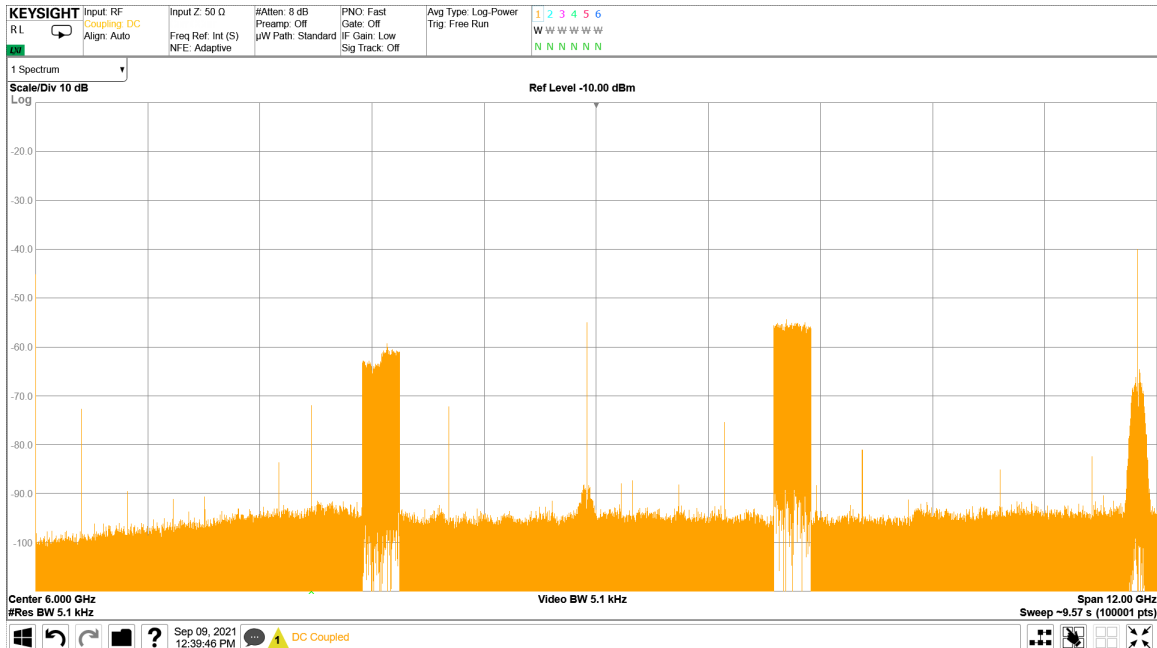
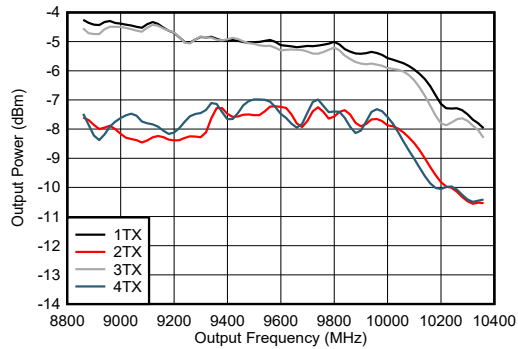


Figure 7-228. TX 4x100 MHz NR Output Spectrum 8.11 GHz

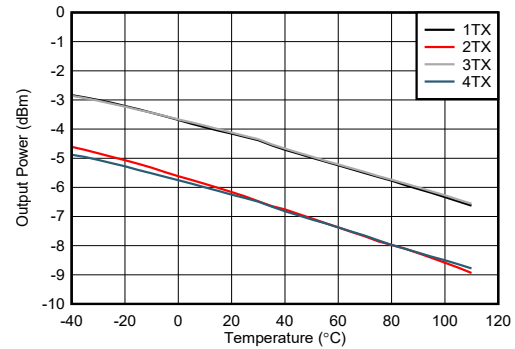
7.12.7 TX Typical Characteristics at 9.6 GHz

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



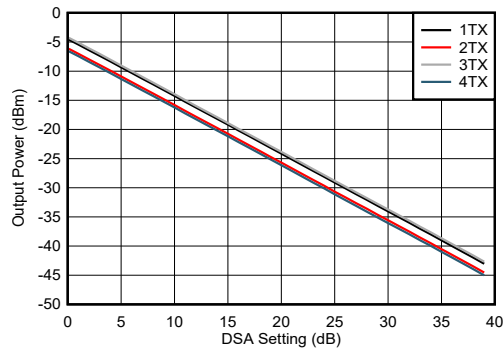
Includes PCB and cable losses.

Figure 7-229. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

Figure 7-230. TX Output Power vs Frequency at 9.61 GHz



Includes PCB and cable losses.

Figure 7-231. TX Output Power vs DSA Setting at 9.6 GHz

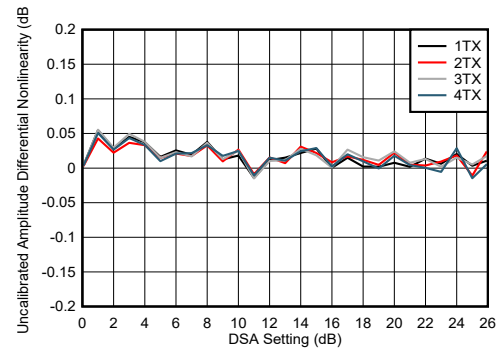


Figure 7-232. TX DSA Uncalibrated Amplitude Differential Nonlinearity

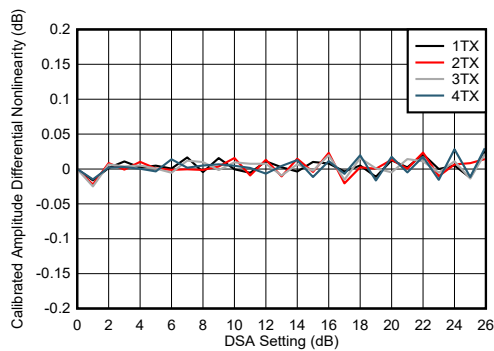


Figure 7-233. TX DSA Calibrated Amplitude Differential Nonlinearity

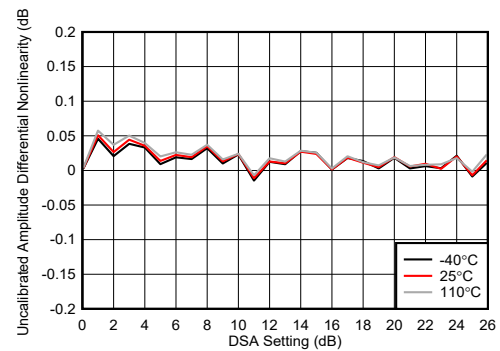


Figure 7-234. TX DSA Uncalibrated Amplitude Differential Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

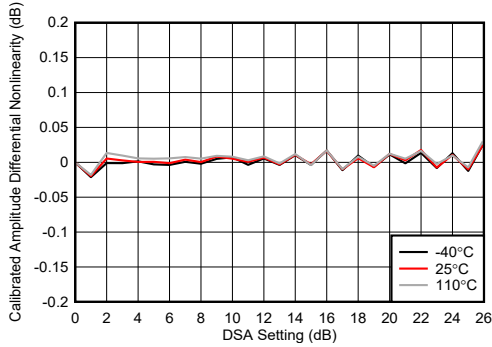


Figure 7-235. TX DSA Calibrated Amplitude Differential Nonlinearity

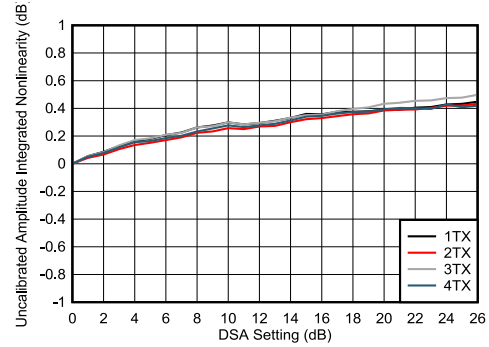


Figure 7-236. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

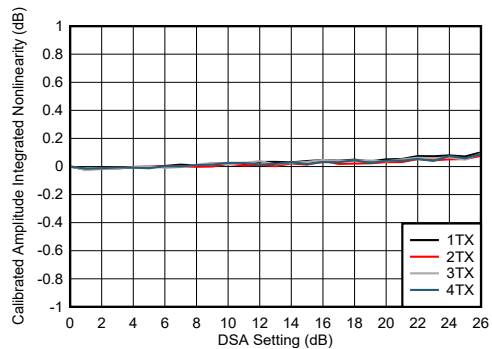


Figure 7-237. TX DSA Calibrated Amplitude Integrated Nonlinearity

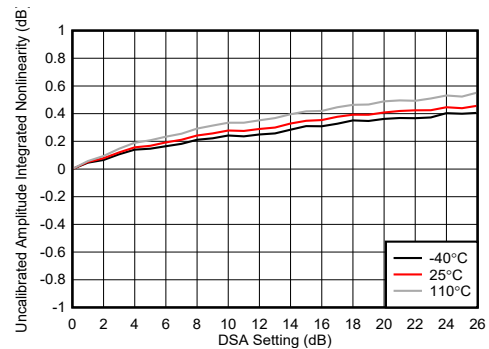


Figure 7-238. TX DSA Uncalibrated Amplitude Integrated Nonlinearity

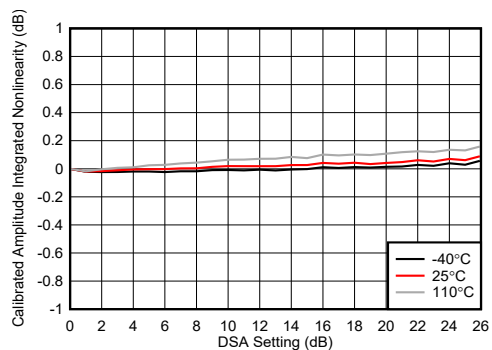


Figure 7-239. TX DSA Calibrated Amplitude Integrated Nonlinearity

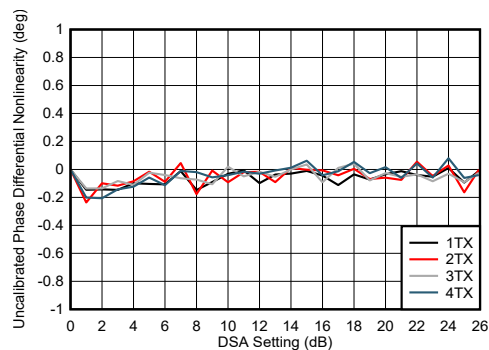


Figure 7-240. TX DSA Uncalibrated Phase Differential Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

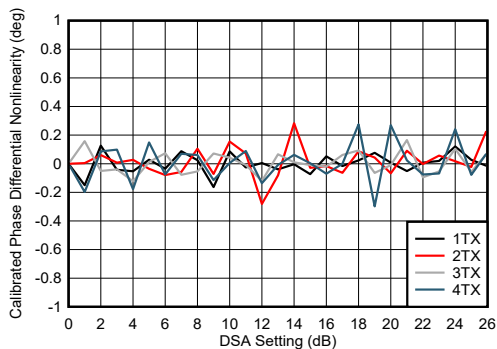


Figure 7-241. TX DSA Calibrated Phase Differential Nonlinearity

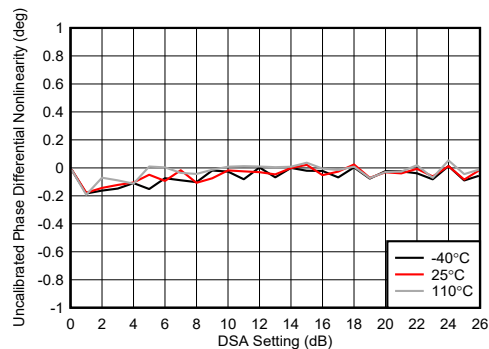


Figure 7-242. TX DSA Uncalibrated Phase Differential Nonlinearity

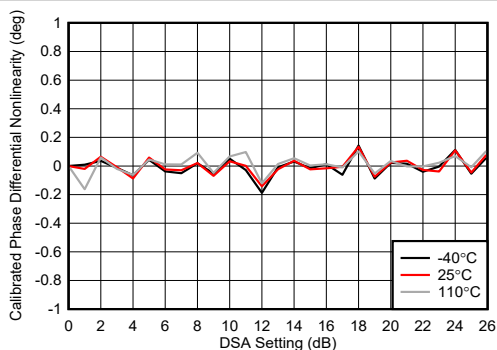


Figure 7-243. TX DSA Calibrated Phase Differential Nonlinearity

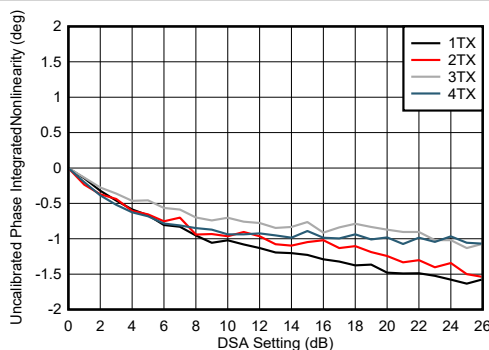


Figure 7-244. TX DSA Uncalibrated Phase Integrated Nonlinearity

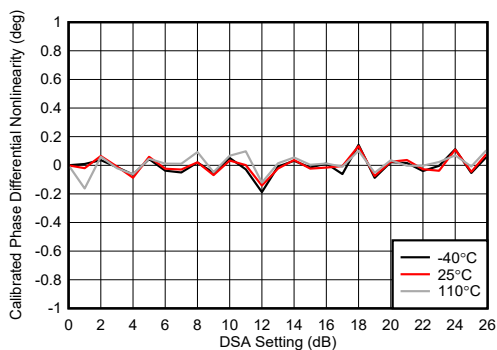


Figure 7-245. TX DSA Calibrated Phase Integrated Nonlinearity

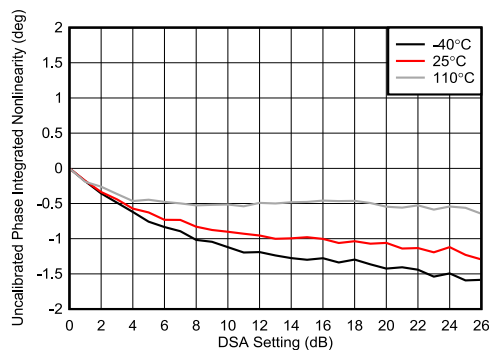


Figure 7-246. TX DSA Uncalibrated Phase Integrated Nonlinearity

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

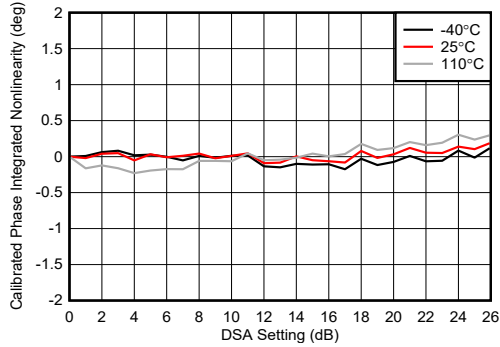
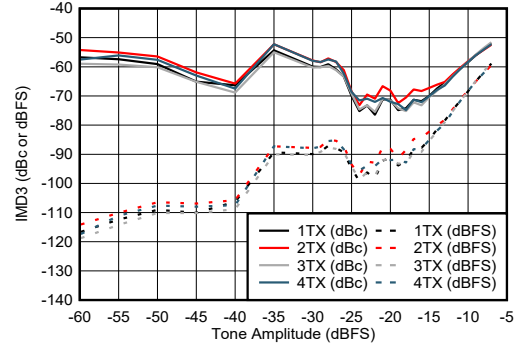
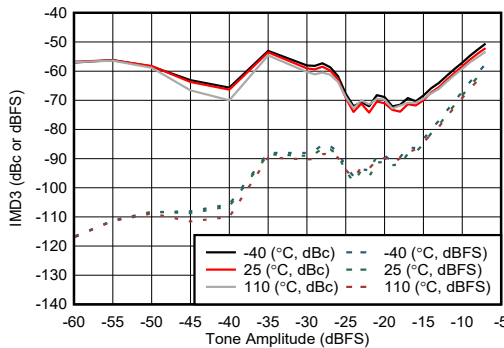


Figure 7-247. TX DSA Calibrated Amplitude Integrated Nonlinearity



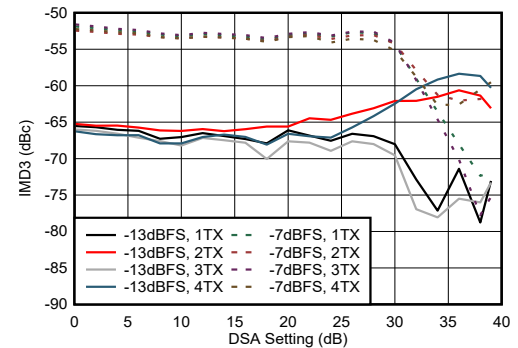
50 MHz tone spacing

Figure 7-248. TX IMD3 vs Digital Amplitude at 9.61 GHz



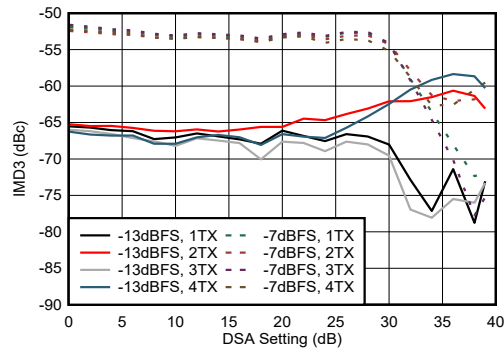
50 MHz tone spacing

Figure 7-249. TX IMD3 vs Digital Amplitude at 9.61 GHz



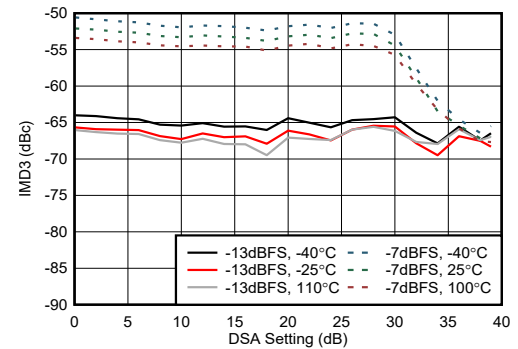
50 MHz tone spacing

Figure 7-250. TX IMD3 vs DSA Setting at 9.61 GHz



50 MHz tone spacing

Figure 7-251. TX IMD3 vs DSA Setting at 9.61 GHz



50 MHz tone spacing

Figure 7-252. TX IMD3 vs DSA Setting at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

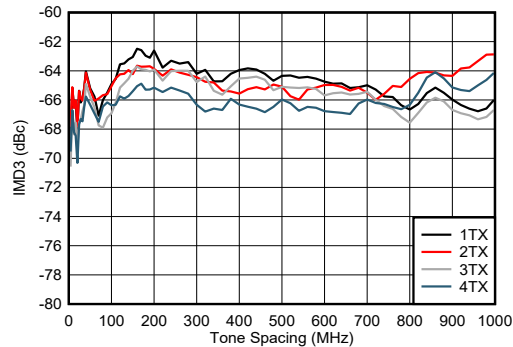


Figure 7-253. TX IMD3 vs Tone Spacing at 9.61 GHz

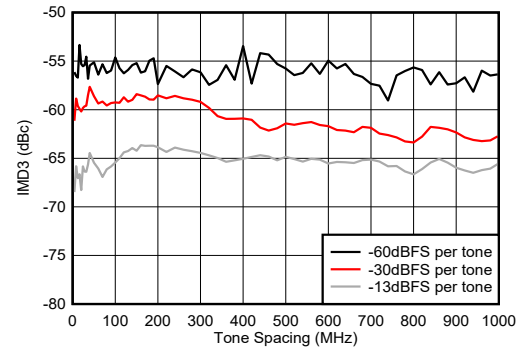


Figure 7-254. TX IMD3 vs Tone Spacing at 9.61 GHz

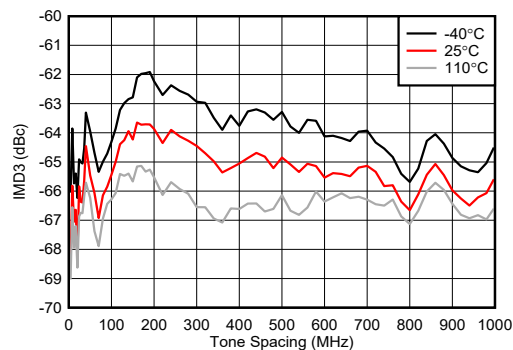


Figure 7-255. TX IMD3 vs Tone Spacing at 9.61 GHz

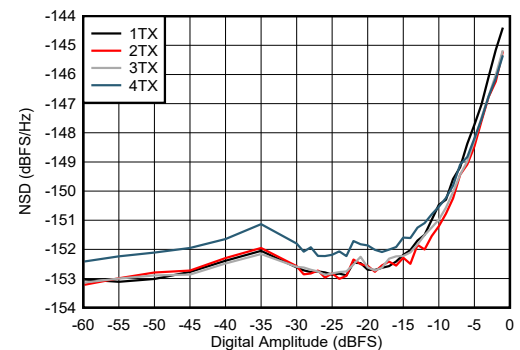


Figure 7-256. TX NSD vs Digital Amplitude at 9.61 GHz

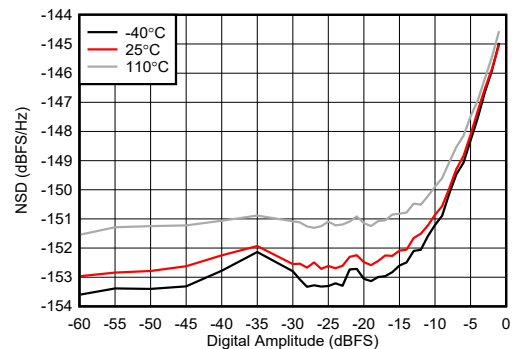


Figure 7-257. TX NSD vs Digital Amplitude at 9.61 GHz

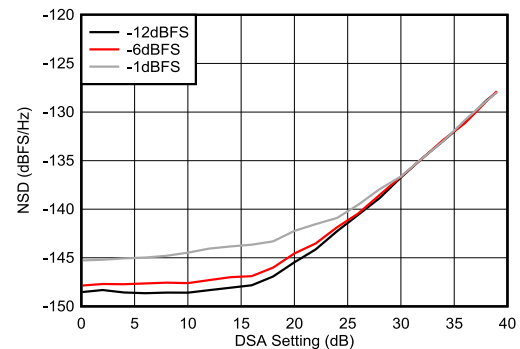


Figure 7-258. TX NSD vs DSA Setting at 9.61 GHz

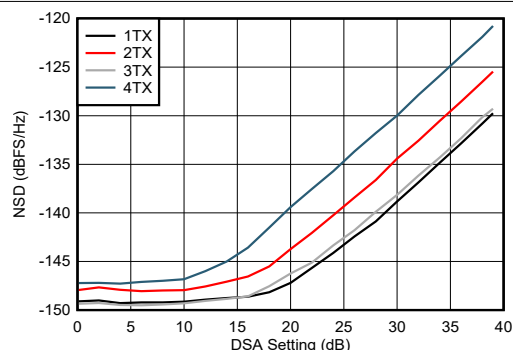


Figure 7-259. TX NSD vs DSA Setting at 9.61 GHz

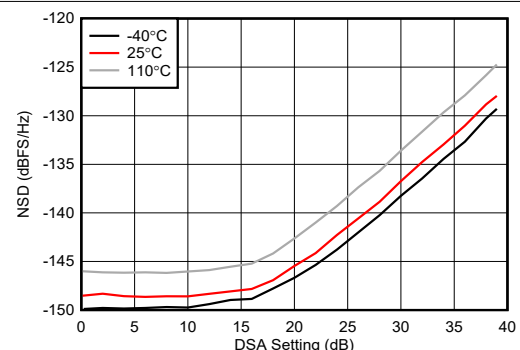
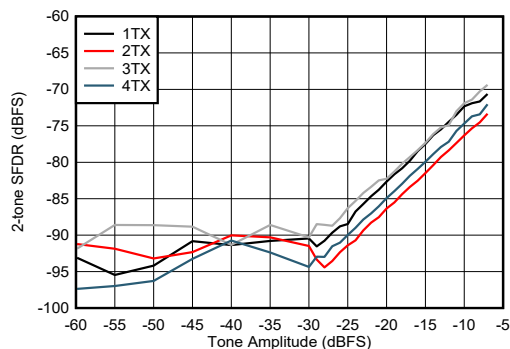


Figure 7-260. TX NSD vs DSA Setting at 9.61 GHz

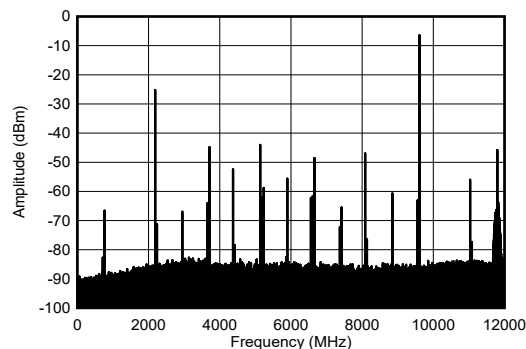
7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



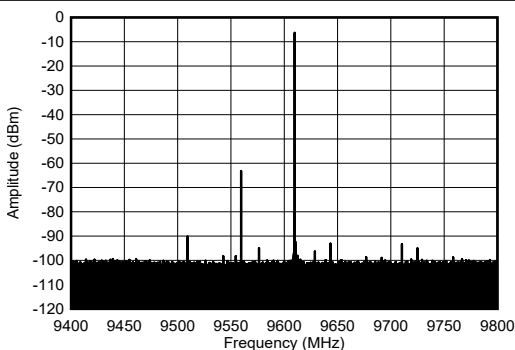
50MHz tone spacing

Figure 7-261. TX 2-tone SFDR vs Digital Amplitude at 9.61 GHz



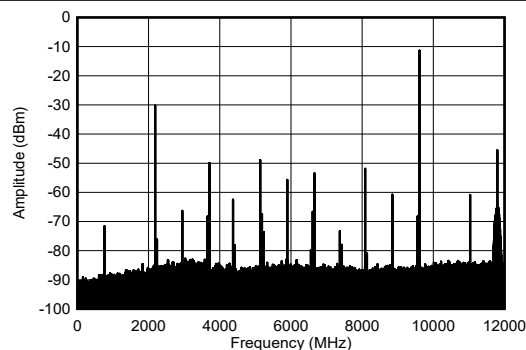
Includes PCB and cable losses.

Figure 7-262. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (wideband)



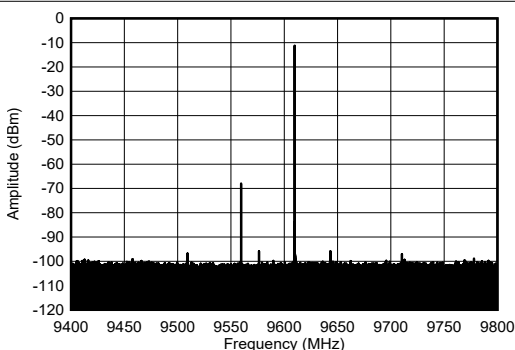
Includes PCB and cable losses.

Figure 7-263. TX Single Tone Spectrum at 9.61 GHz and -1 dBFS (400 MHz BW)



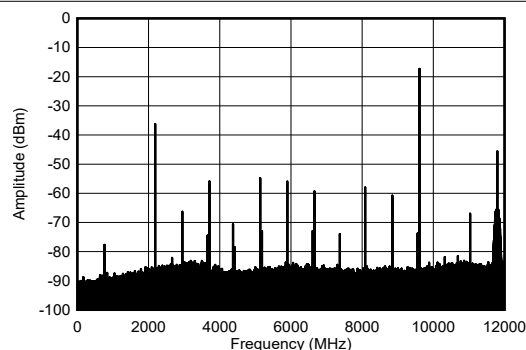
Includes PCB and cable losses.

Figure 7-264. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (wideband)



Includes PCB and cable losses.

Figure 7-265. TX Single Tone Spectrum at 9.61 GHz and -6 dBFS (400 MHz BW)

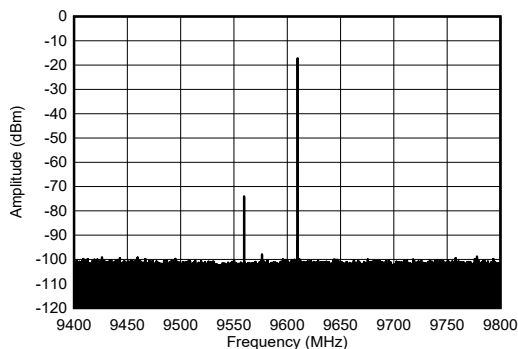


Includes PCB and cable losses.

Figure 7-266. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)

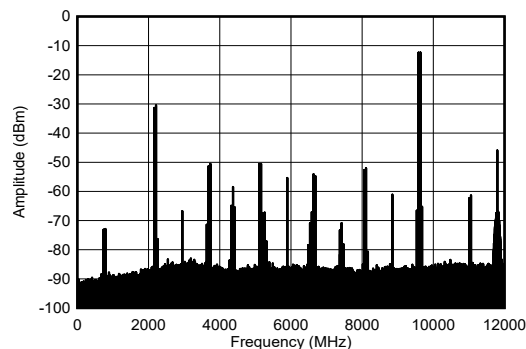
7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching



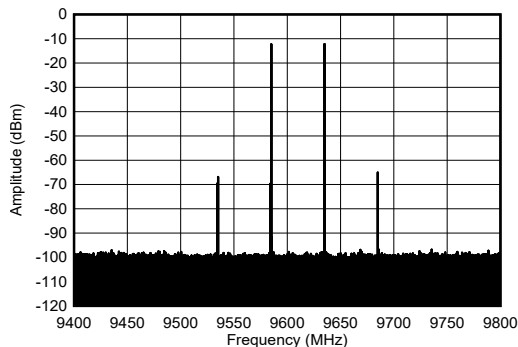
Includes PCB and cable losses.

Figure 7-267. TX Single Tone Spectrum at 9.61 GHz and -12 dBFS (400 MHz BW)



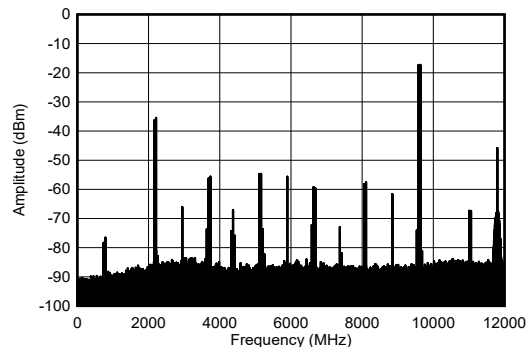
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 7-268. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (wideband)



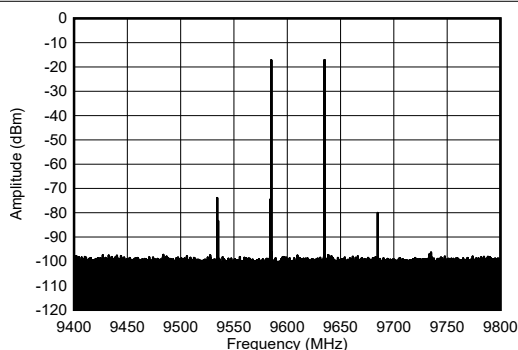
Includes PCB and cable losses, 50 MHz tone spacing.

Figure 7-269. TX 2-Tone Spectrum at 9.61 GHz and -7 dBFS (400 MHz BW)



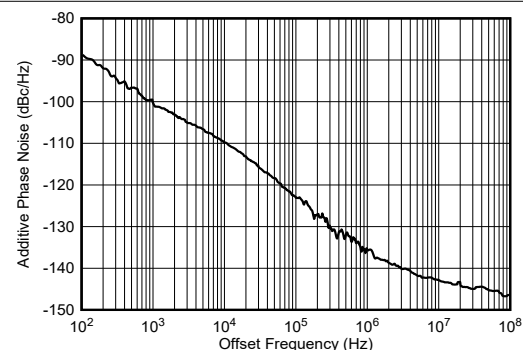
Includes PCB and cable losses, 50MHz tone spacing.

Figure 7-270. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (wideband)



Includes PCB and cable losses, 50 MHz tone spacing.

Figure 7-271. TX 2-Tone Spectrum at 9.61 GHz and -12 dBFS (400 MHz BW)



Single sideband, external clock mode, input clock phase noise removed

Figure 7-272. TX Additive Phase Noise vs Offset Frequency at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

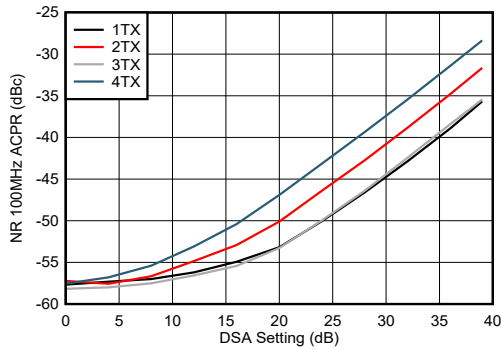


Figure 7-273. TX NR100MHz ACPR vs DSA Setting at 9.61 GHz

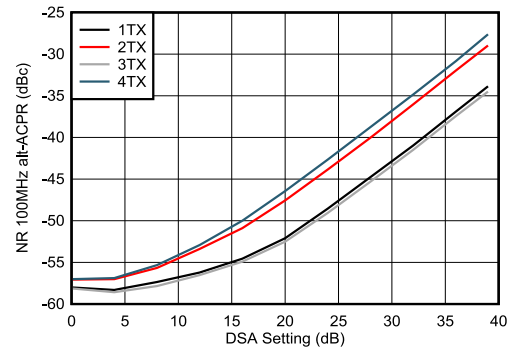


Figure 7-274. TX NR100MHz alt-ACPR vs DSA Setting at 9.61 GHz

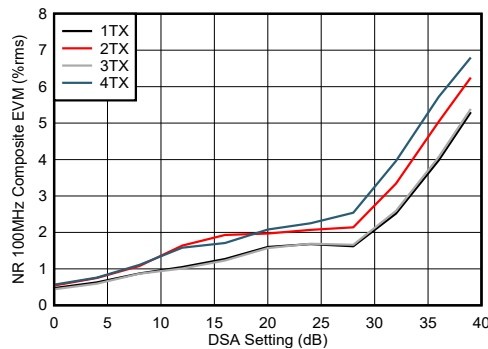
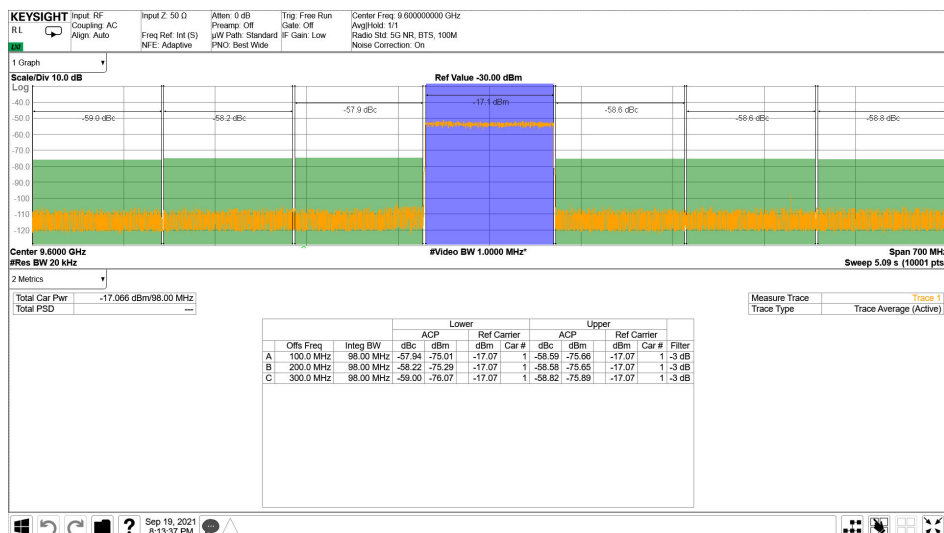


Figure 7-275. TX NR100MHz EVM vs DSA Setting at 9.61 GHz

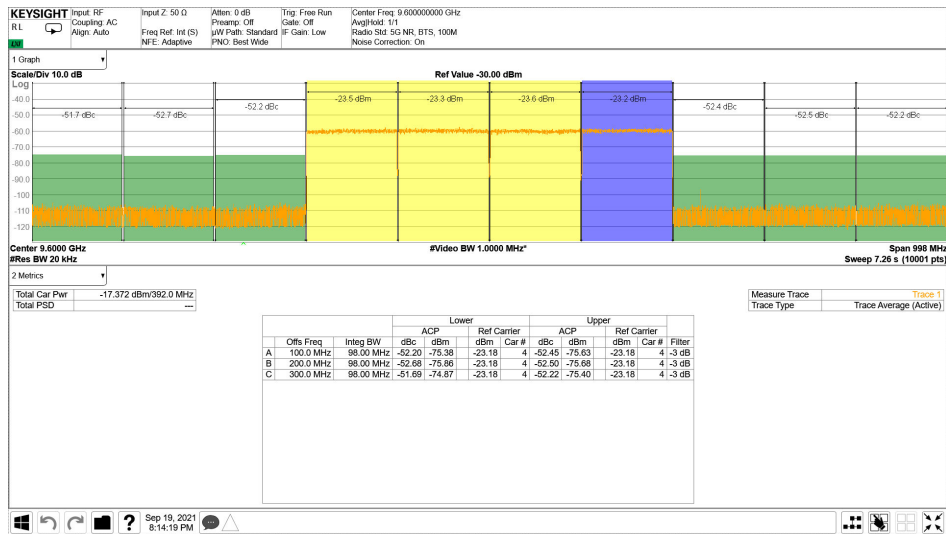


Includes PCB and cable losses.

Figure 7-276. TX NR100 MHz Output Spectrum at 9.61 GHz

7.12.7 TX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$ with nominal supplies. Default conditions: TX input data rate = 491.52 MSPS, $f_{\text{DAC}} = 11796.48$ MSPS (8x interpolation), Mixed mode, 1st Nyquist zone output, PLL clock mode with $f_{\text{REF}} = 1474.56$ MHz, $A_{\text{OUT}} = -1$ dBFS, DSA = 0 dB, Sin(x)/x enabled, DSA calibrated, TX Clock Dither Enabled, 9.6 GHz matching

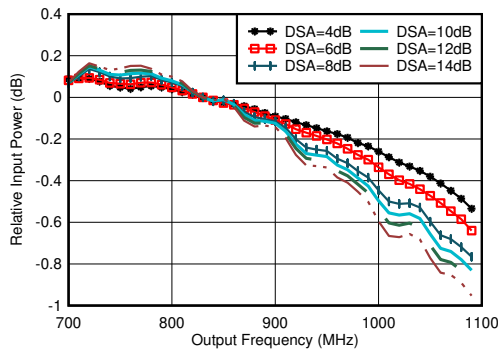


Includes PCB and cable losses.

Figure 7-277. TX 4xNR100 MHz Output Spectrum at 9.61 GHz

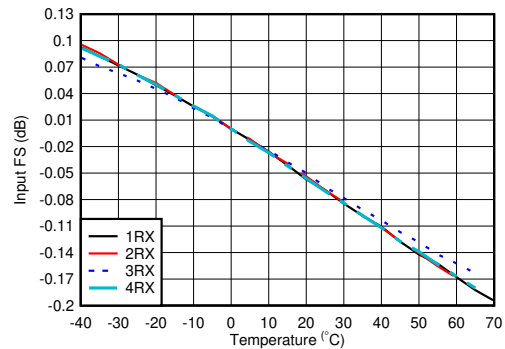
7.12.8 RX Typical Characteristics at 800 MHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52$ MHz, $A_{\text{IN}} = -3$ dBFS, DSA setting = 4 dB.



With 0.8 GHz matching, normalized to 830 MHz

Figure 7-278. RX In-Band Gain Flatness for Channel 1RX, $f_{\text{IN}} = 830$ MHz

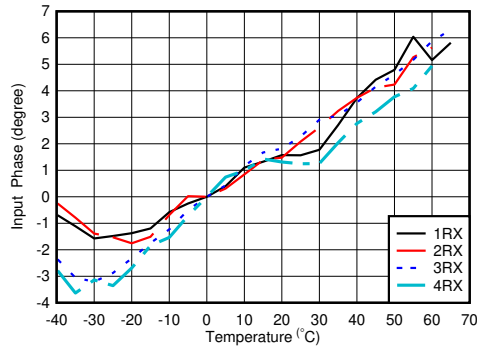


With 0.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 7-279. RX Input Fullscale vs Temperature and Channel at 800 MHz

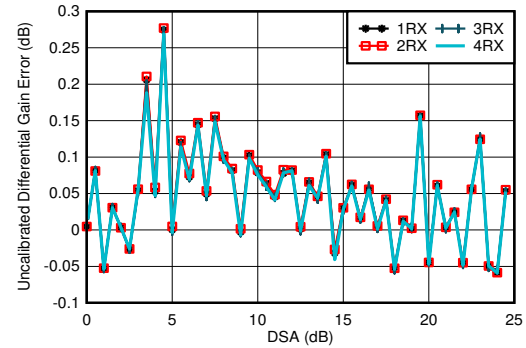
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 0.8 GHz matching, normalized to phase at 25°C

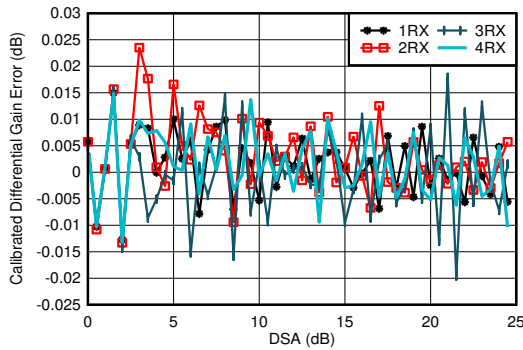
Figure 7-280. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 0.8 \text{ GHz}$



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

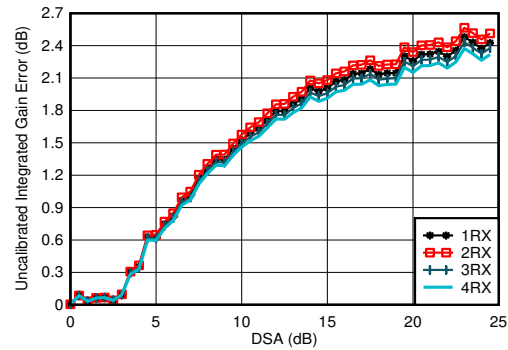
Figure 7-281. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

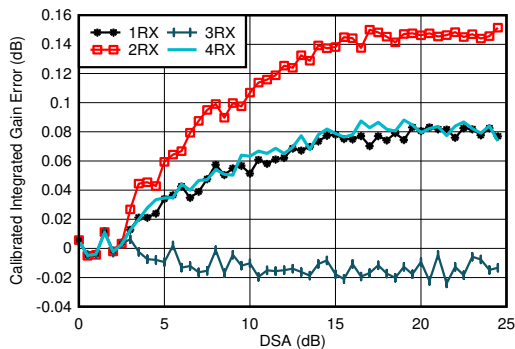
Figure 7-282. RX Calibrated Differential Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

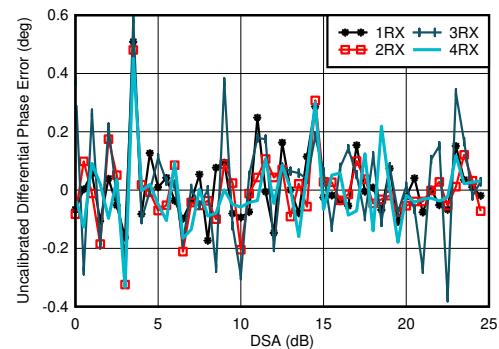
Figure 7-283. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-284. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



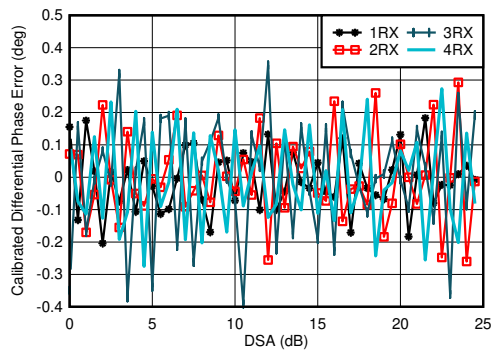
With 0.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

Figure 7-285. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz

7.12.8 RX Typical Characteristics at 800 MHz (continued)

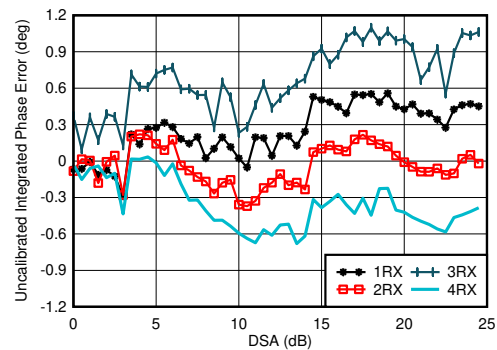
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 0.8 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

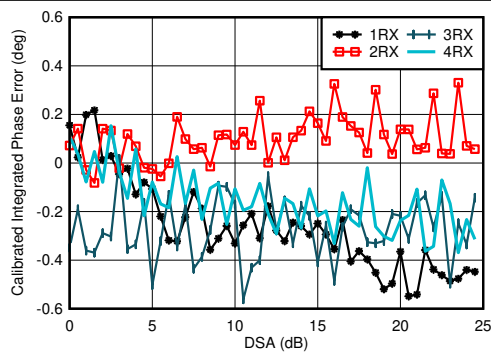
Figure 7-286. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

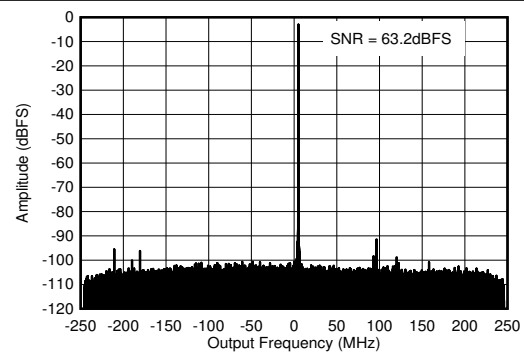
Figure 7-287. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

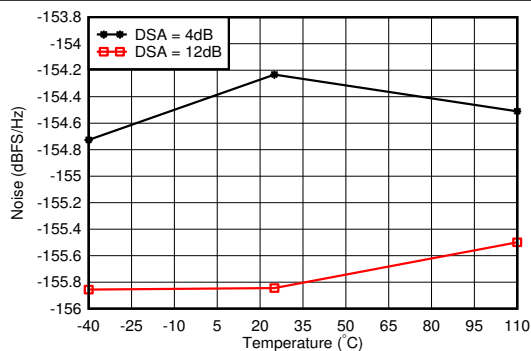
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-288. RX Calibrated Integrated Phase Error vs DSA Setting at 0.8 GHz



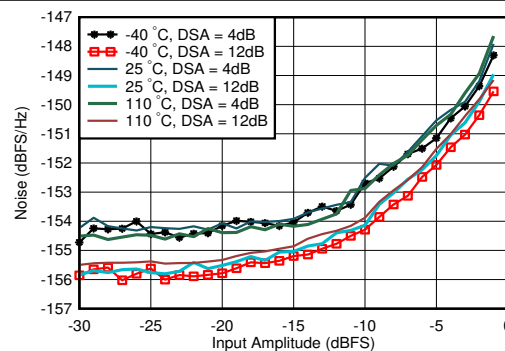
With 0.8 GHz matching, $f_{\text{IN}} = 840\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

Figure 7-289. RX Output FFT at 0.8 GHz



With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 7-290. RX Noise Spectral Density vs Temperature at 0.8 GHz

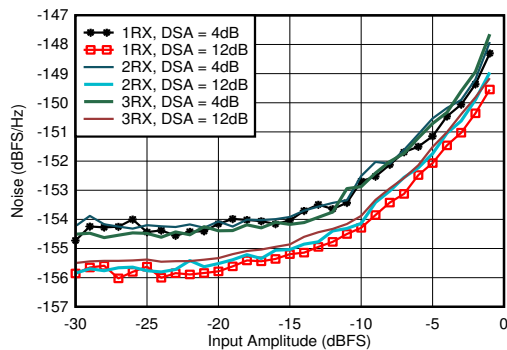


With 0.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-291. RX Noise Spectral Density vs Input Amplitude and Temperature at 0.8 GHz

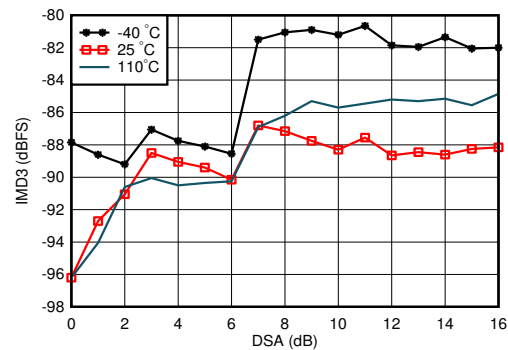
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



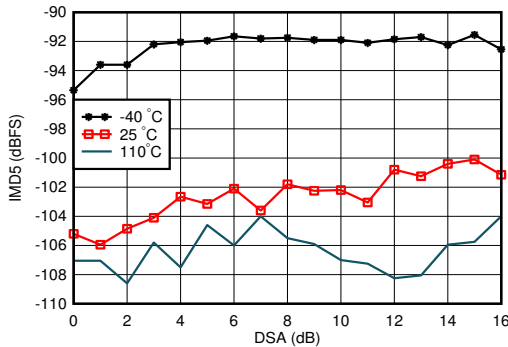
With 0.8 GHz matching, 12.5-MHz offset from tone

Figure 7-292. RX Noise Spectral Density vs Input Amplitude and Channel at 0.8 GHz



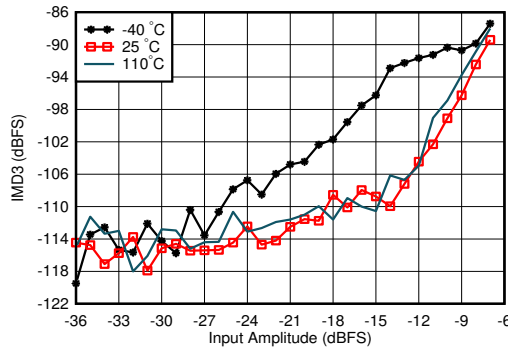
A. With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-293. RX IMD3 vs DSA Setting and Temperature at 0.8 GHz



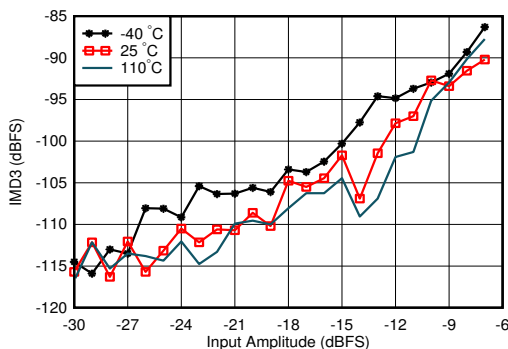
With 0.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-294. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



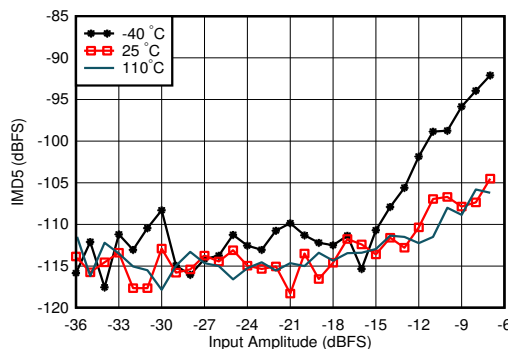
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-295. RX IMD3 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-296. RX IMD3 vs Input Level and Temperature at 0.8 GHz

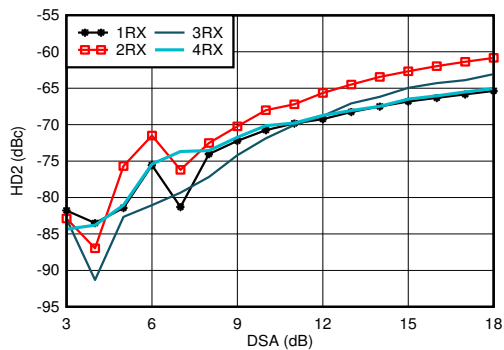


With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-297. RX IMD5 vs Input Level and Temperature at 0.8 GHz

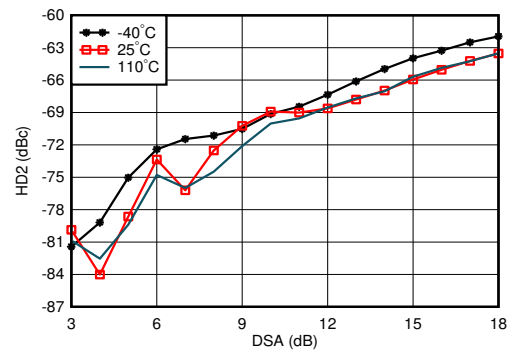
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



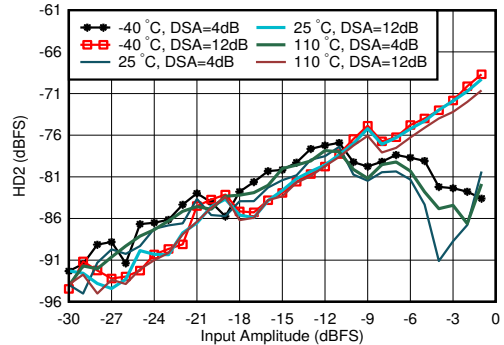
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-298. RX HD2 vs DSA Setting and Channel at 0.8 GHz



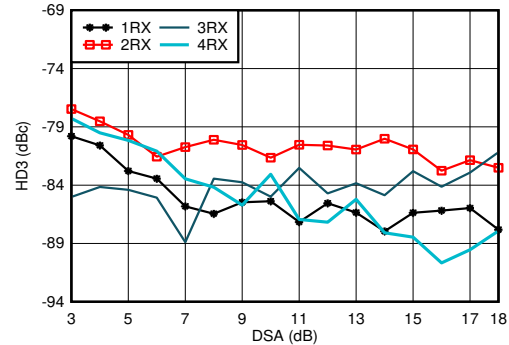
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-299. RX HD2 vs DSA Setting and Temperature at 0.8 GHz



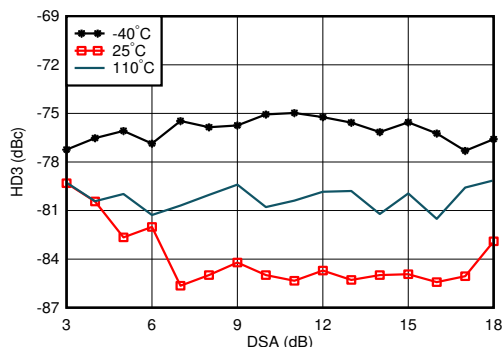
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-300. RX HD2 vs Input Level and Temperature at 0.8 GHz



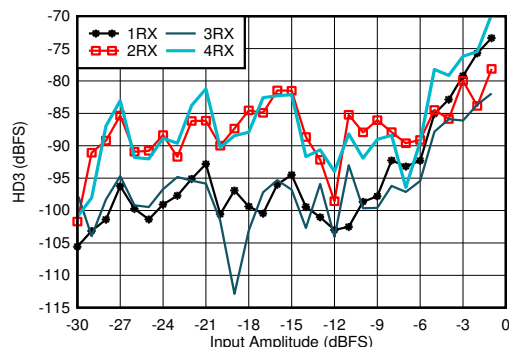
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-301. RX HD3 vs DSA Setting and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-302. RX HD3 vs DSA Setting and Temperature at 0.8 GHz

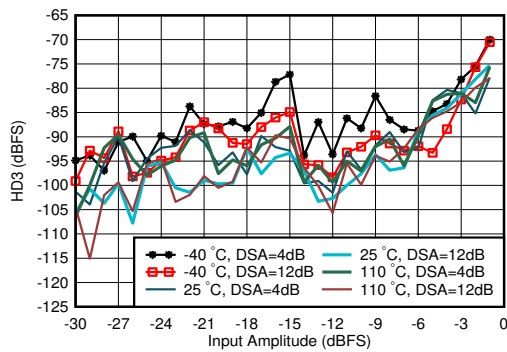


With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-303. RX HD3 vs Input Level and Channel at 0.8 GHz

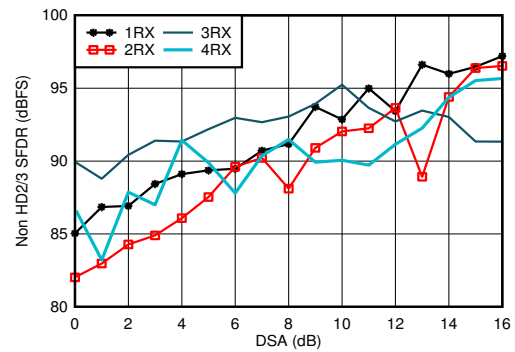
7.12.8 RX Typical Characteristics at 800 MHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



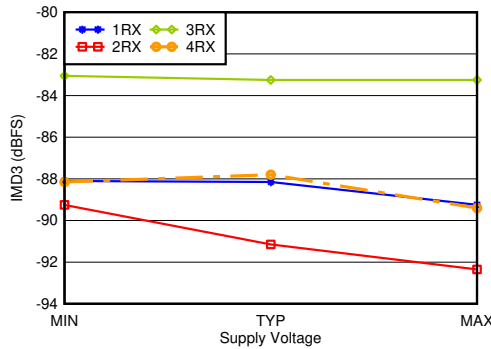
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-304. RX HD3 vs Input Level and Temperature at 0.8 GHz



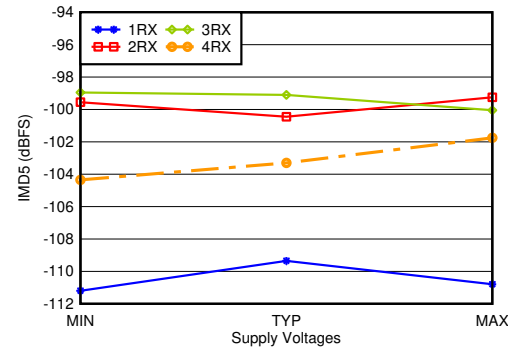
With 0.8 GHz matching

Figure 7-305. RX Non-HD2/3 vs DSA Setting at 0.8 GHz



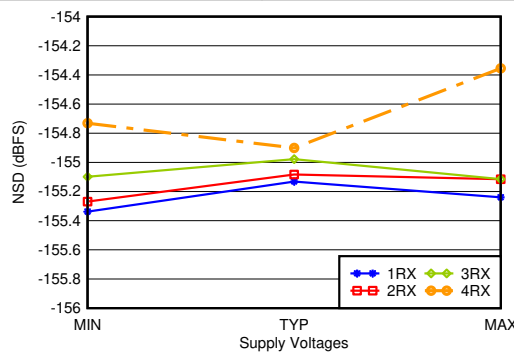
With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-306. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-307. RX IMD5 vs Supply and Channel at 0.8 GHz

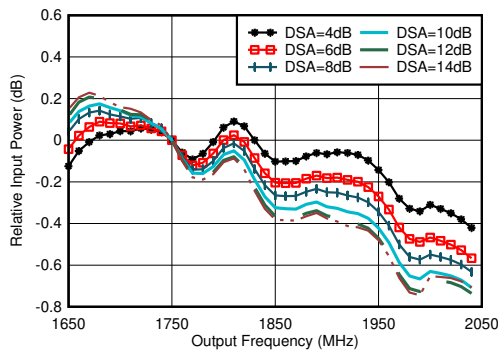


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-308. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

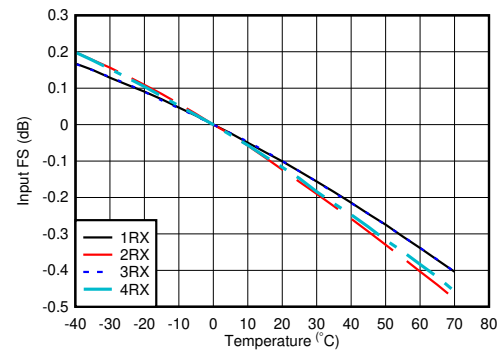
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



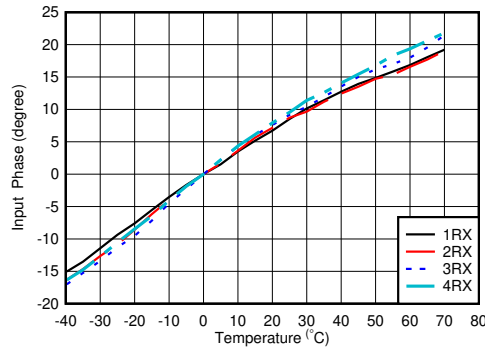
With 1.8 GHz matching, normalized to 1.75 GHz

Figure 7-309. RX In-Band Gain Flatness, $f_{\text{IN}} = 1750 \text{ MHz}$



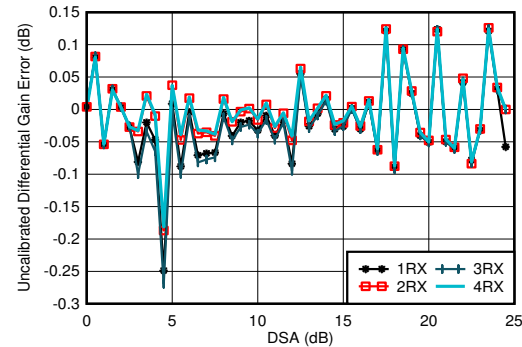
With 1.8 GHz matching, normalized to fullscale at 25°C for each channel

Figure 7-310. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at 25°C

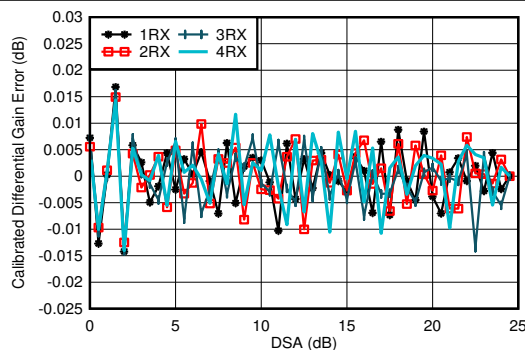
Figure 7-311. RX Input Phase vs Temperature and DSA at $f_{\text{IN}} = 1.75 \text{ GHz}$



With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

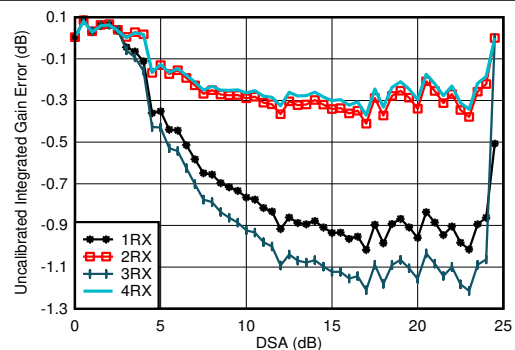
Figure 7-312. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-313. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



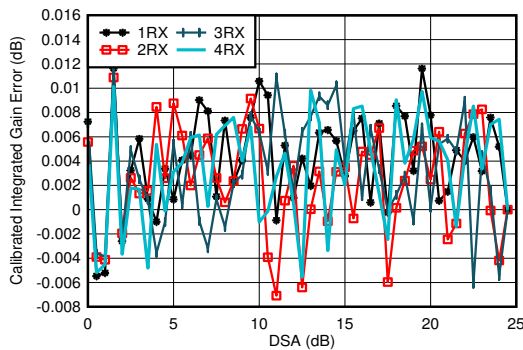
With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-314. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

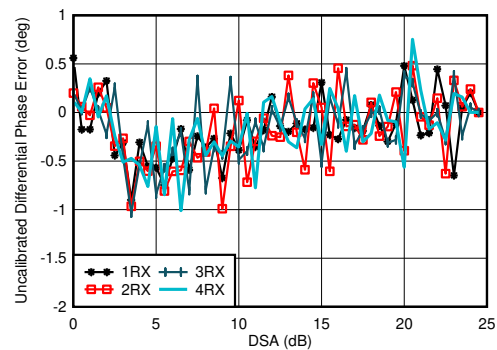
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

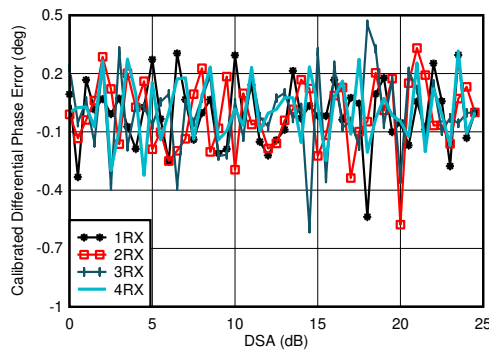
Figure 7-315. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

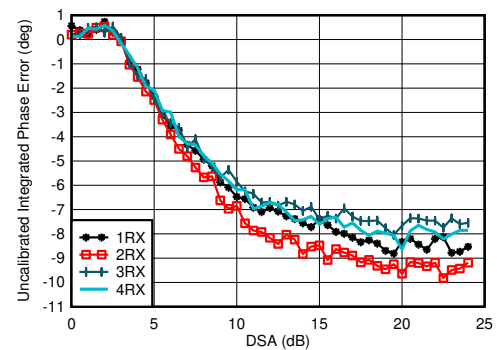
Figure 7-316. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

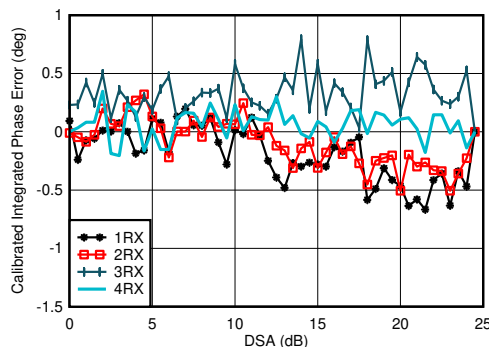
Figure 7-317. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

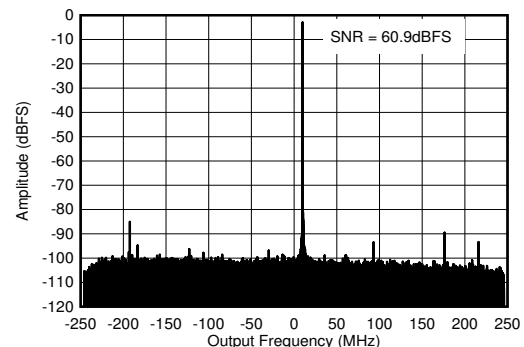
Figure 7-318. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-319. RX Calibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

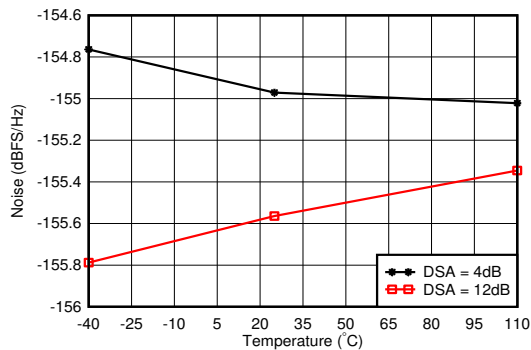


With 1.8 GHz matching, $f_{\text{IN}} = 2610 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

Figure 7-320. RX Output FFT at 1.75 GHz

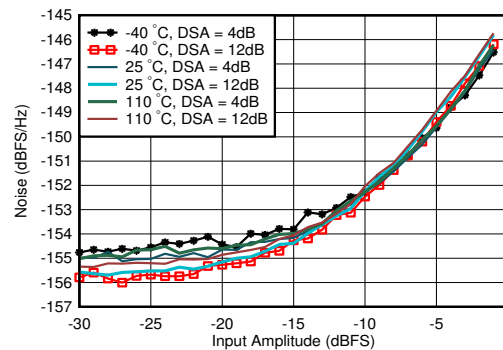
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



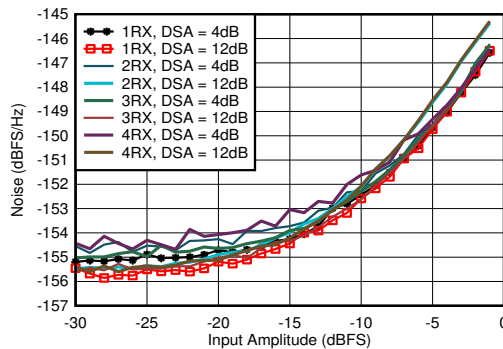
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 7-321. RX Noise Spectral Density vs Temperature at 1.75 GHz



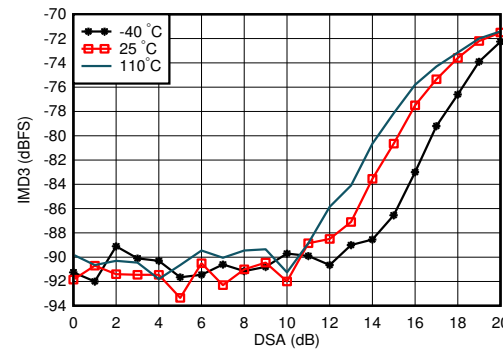
With 1.8 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-322. RX Noise Spectral Density vs Input Amplitude and Temperature at 1.75 GHz



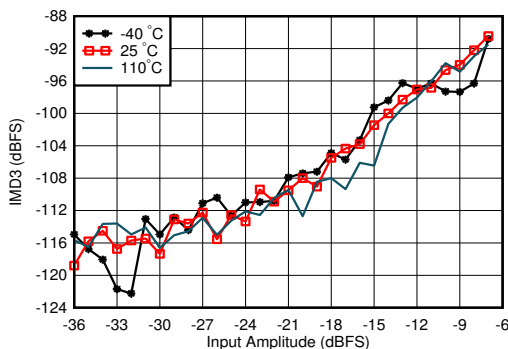
With 1.8 GHz matching, 12.5-MHz offset from tone

Figure 7-323. RX Noise Spectral Density vs Input Amplitude and Channel at 1.75 GHz



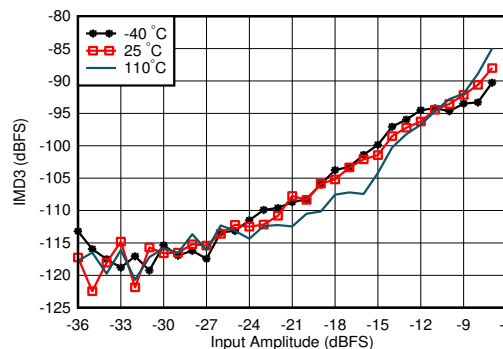
With 1.8 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-324. RX IMD3 vs DSA Setting and Temperature at 1.75 GHz



With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-325. RX IMD3 vs Input Level and Temperature at 1.75 GHz

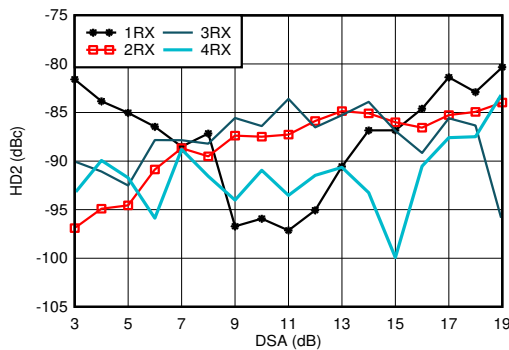


With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-326. RX IMD3 vs Input Level and Temperature at 1.75 GHz

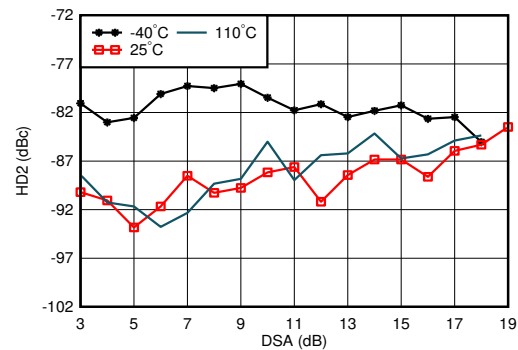
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



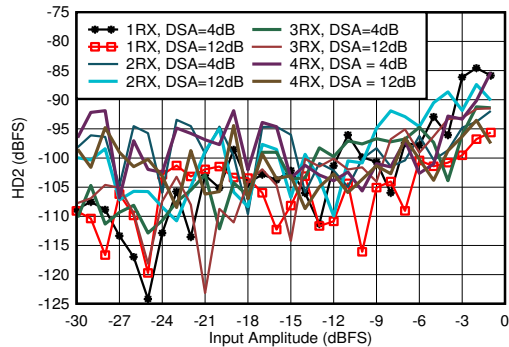
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-327. RX HD2 vs DSA Setting and Channel at 1.9 GHz



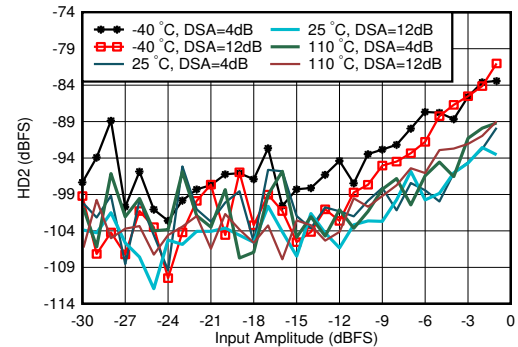
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-328. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



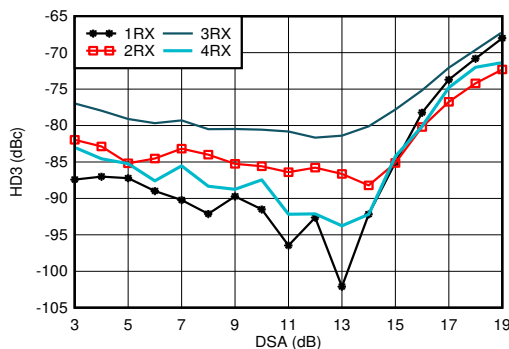
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-329. RX HD2 vs Input Amplitude and Channel at 1.9 GHz



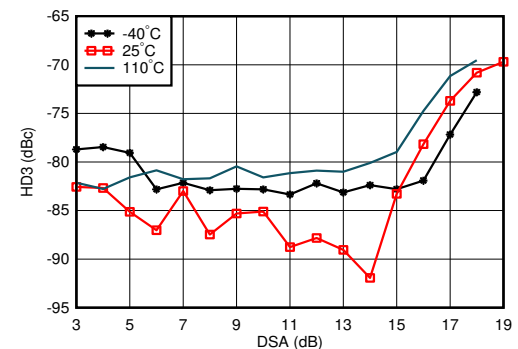
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-330. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz



With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-331. RX HD3 vs DSA Setting and Channel at 1.9 GHz

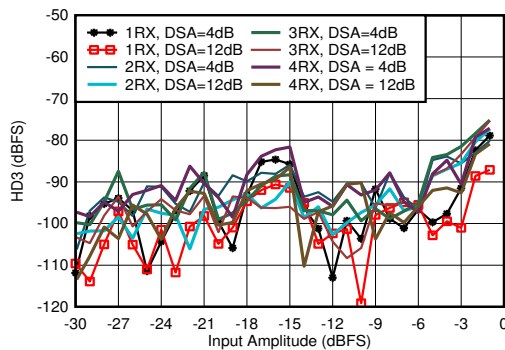


With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-332. RX HD3 vs DSA Setting and Temperature at 1.9 GHz

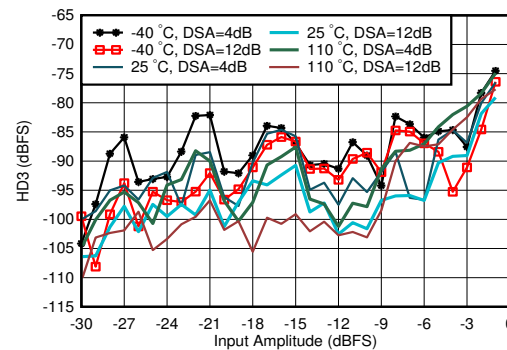
7.12.9 RX Typical Characteristics at 1.75-1.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



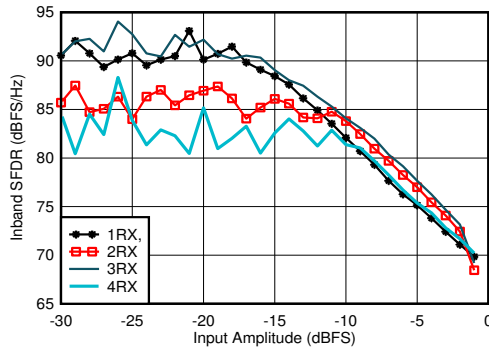
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-333. RX HD3 vs Input Level and Channel at 1.9 GHz



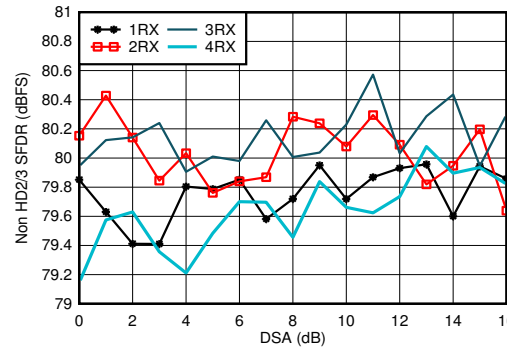
With 1.8 GHz matching, $f_{\text{in}} = 1900\text{ MHz}$, DDC bypass mode (TI only mode for characterization)

Figure 7-334. RX HD3 vs Input Level and Temperature at 1.9 GHz



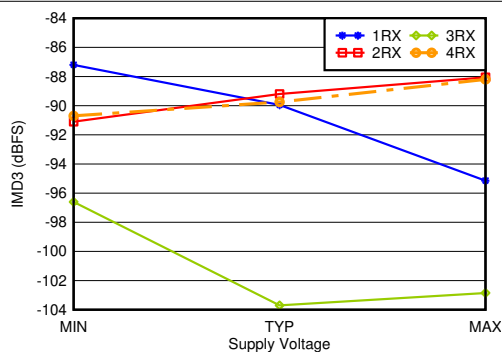
With 1.8 GHz matching, decimated by 3

Figure 7-335. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude at 1.75 GHz



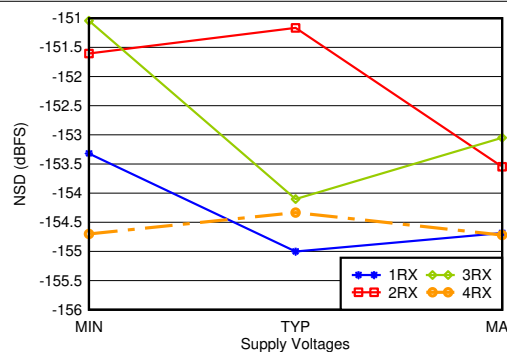
With 1.8 GHz matching

Figure 7-336. RX Non-HD2/3 vs DSA Setting at 1.75 GHz



With 1.8 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-337. RX IMD3 vs Supply and Channel at 1.75 GHz

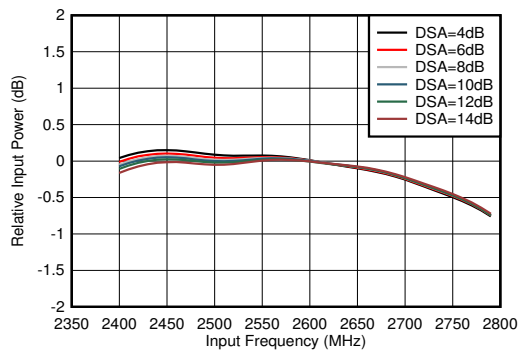


With 1.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-338. RX Noise Spectral Density vs Supply and Channel at 1.75 GHz

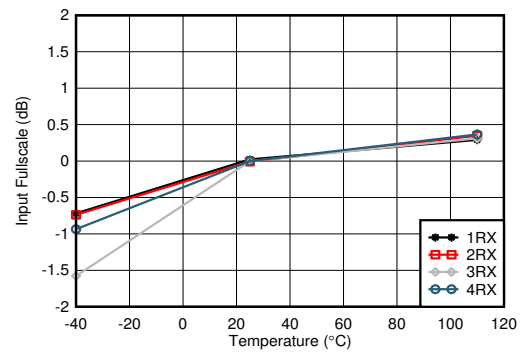
7.12.10 RX Typical Characteristics at 2.6 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



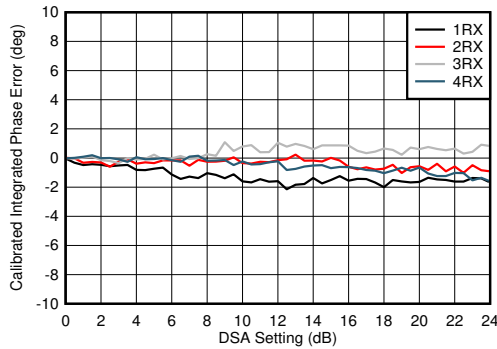
With matching, normalized to power at 2.6 GHz for each DSA setting

Figure 7-339. RX Inband Gain Flatness, $f_{\text{IN}} = 2600 \text{ MHz}$



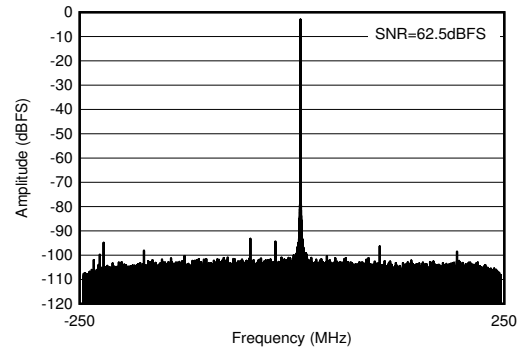
With 2.6 GHz matching, normalized to fullscale at 25°C for each channel

Figure 7-340. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



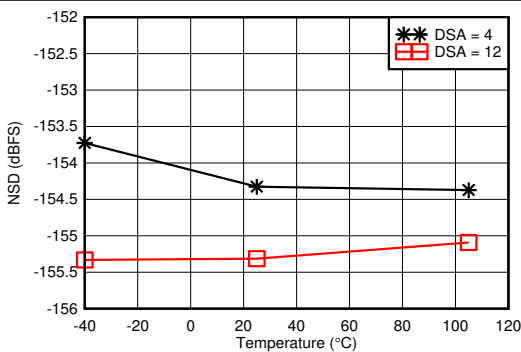
With 2.6 GHz matching
Integrated Phase Error = Phase(DSA Setting) – Phase(DSA Setting = 0)

Figure 7-341. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



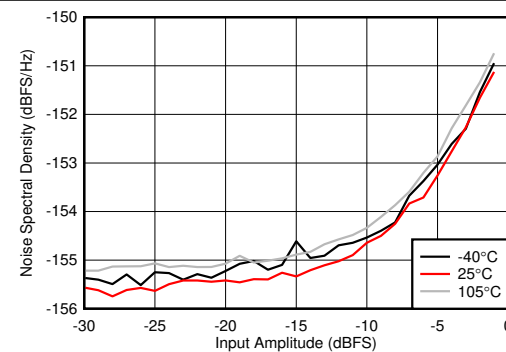
With 2.6 GHz matching, $f_{\text{IN}} = 2610 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

Figure 7-342. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 7-343. RX Noise Spectral Density vs Temperature at 2.6 GHz

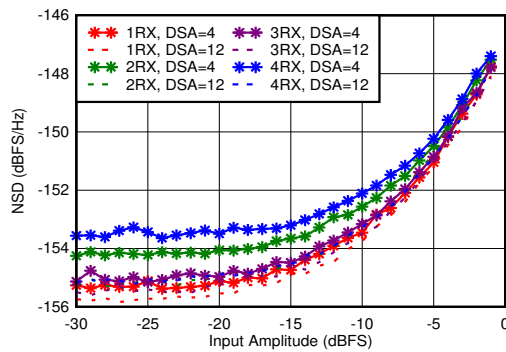


With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-344. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

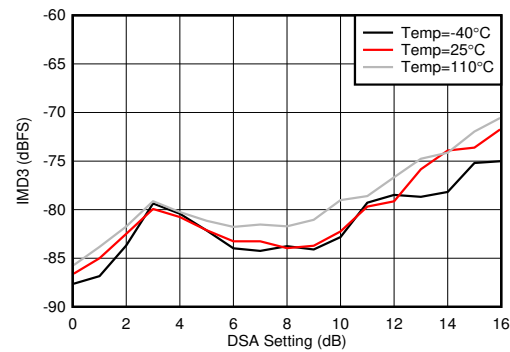
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



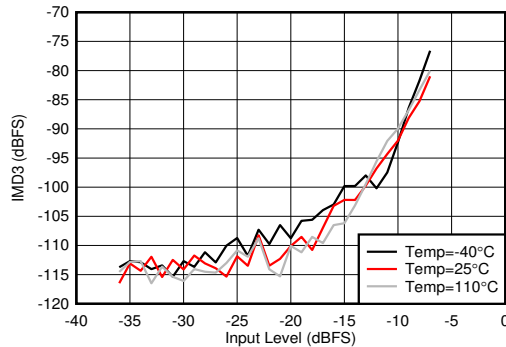
With 2.6 GHz matching, 12.5-MHz offset from tone

Figure 7-345. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz



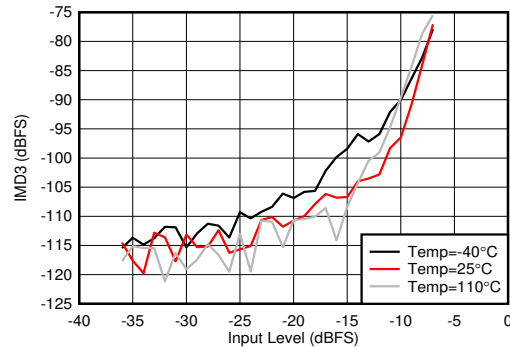
With 2.6 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-346. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz



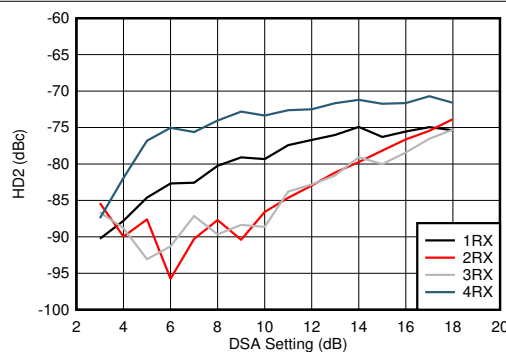
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-347. RX IMD3 vs Input Level and Temperature at 2.6 GHz



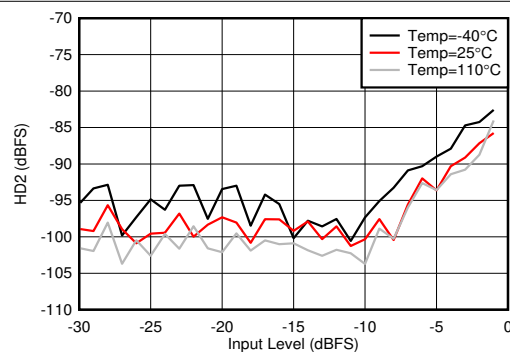
With 2.6 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-348. RX IMD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-349. RX HD2 vs DSA Setting and Channel at 2.6 GHz

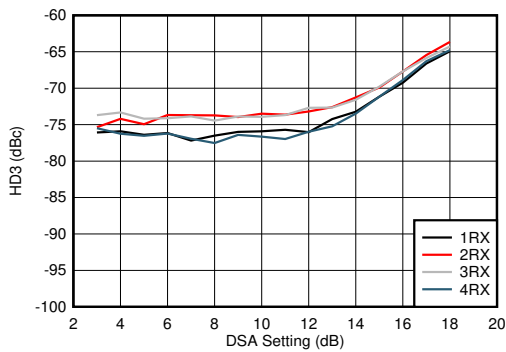


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-350. RX HD2 vs Input Level and Temperature at 2.6 GHz

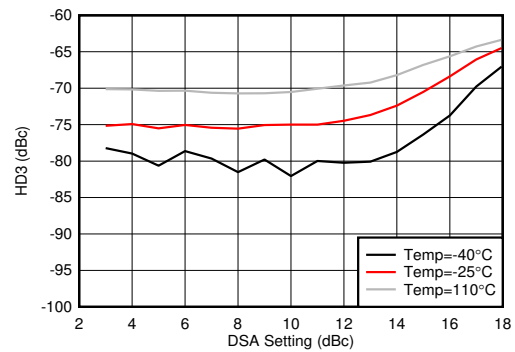
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



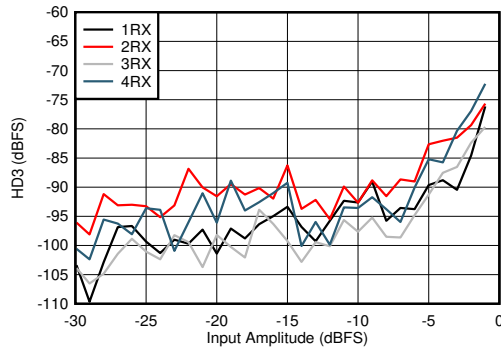
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-351. RX HD3 vs DSA Setting and Channel at 2.6 GHz



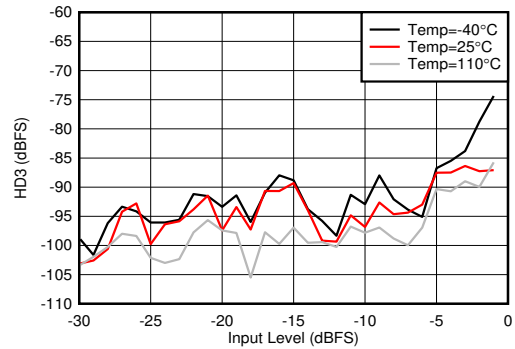
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-352. RX HD3 vs DSA Setting and Temperature at 2.6 GHz



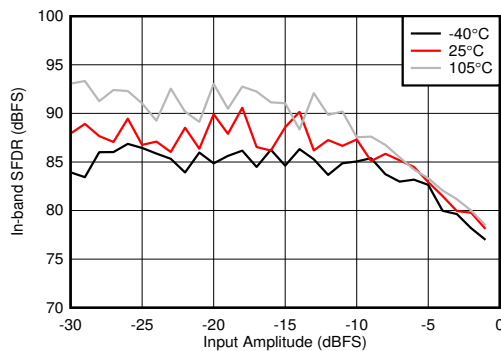
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-353. RX HD3 vs Input Level and Channel at 2.6 GHz



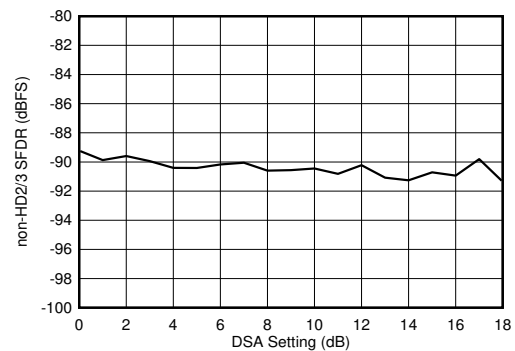
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-354. RX HD3 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, decimate by 4

Figure 7-355. RX In-Band SFDR ($\pm 300 \text{ MHz}$) vs Input Amplitude and Temperature at 2.6 GHz

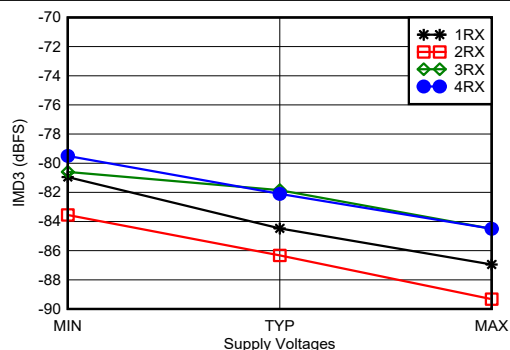


With 2.6 GHz matching

Figure 7-356. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

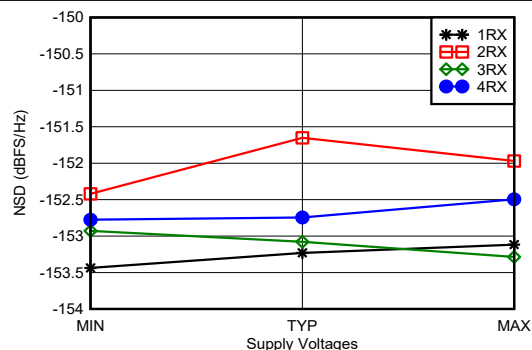
7.12.10 RX Typical Characteristics at 2.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 2.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-357. RX IMD3 vs Supply and Channel at 2.6 GHz

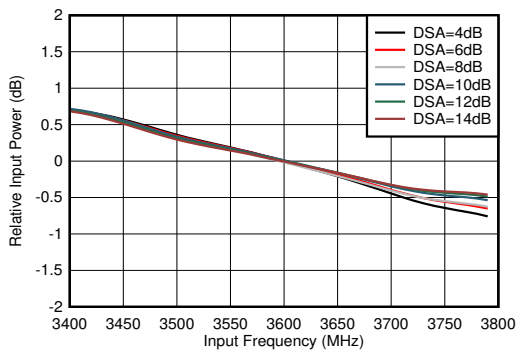


With 2.6 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-358. RX Noise Spectral Density vs Supply and Channel at 2.6 GHz

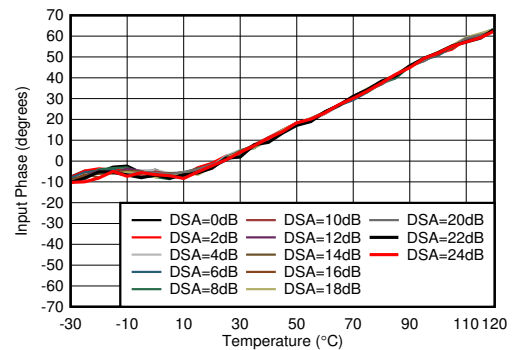
7.12.11 RX Typical Characteristics at 3.5 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



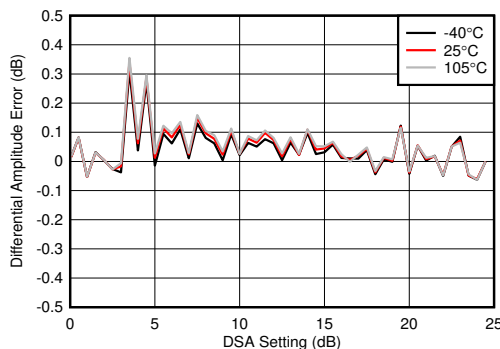
With 3.6 GHz matching, normalized to 3.6 GHz

Figure 7-359. RX In-Band Gain Flatness, $f_{\text{IN}} = 3600 \text{ MHz}$



With 3.6 GHz matching, normalized to phase at 25°C

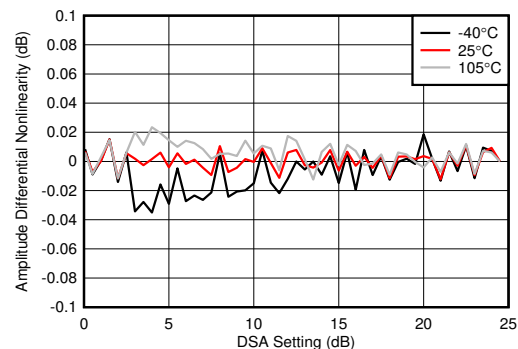
Figure 7-360. RX Input Phase vs Temperature at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

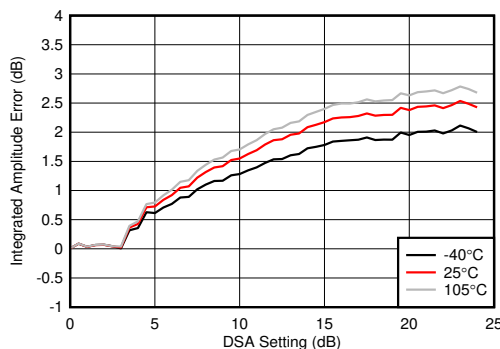
Figure 7-361. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

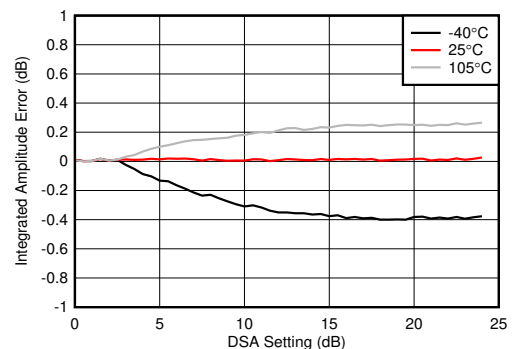
Figure 7-362. RX Calibrated Differential Amplitude Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-363. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz



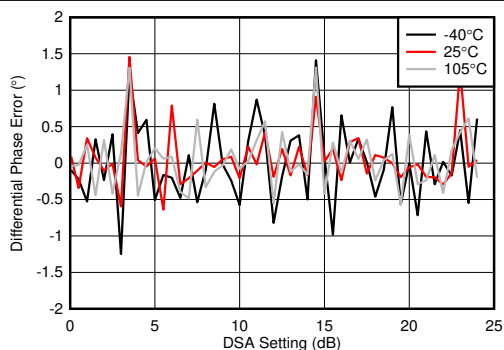
With 3.6 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-364. RX Calibrated Integrated Amplitude Error vs DSA Setting at 3.6 GHz

7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

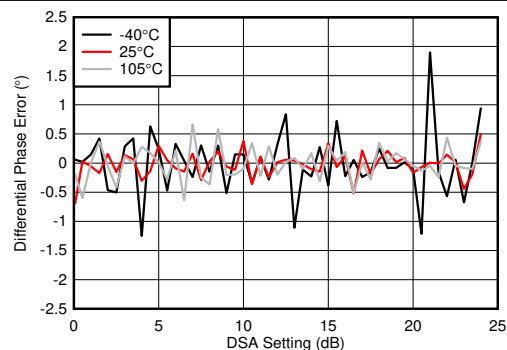
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

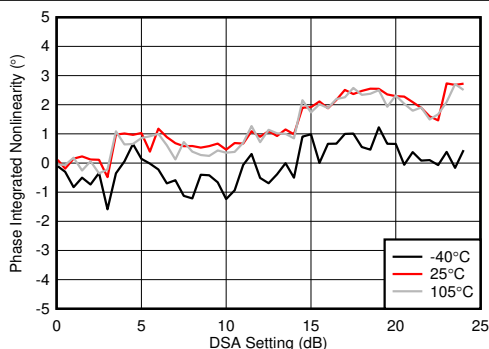
Figure 7-365. RX Uncalibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

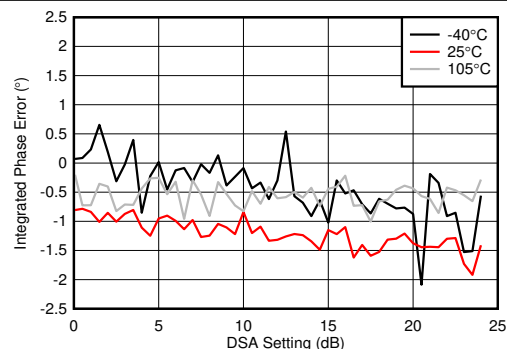
Figure 7-366. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

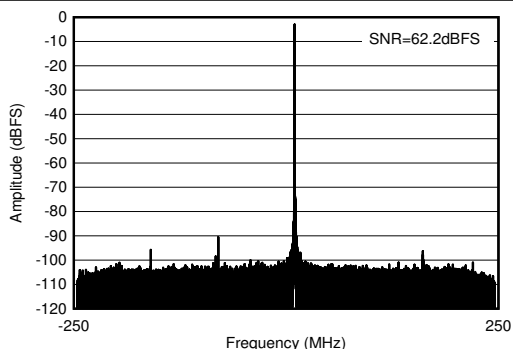
Figure 7-367. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

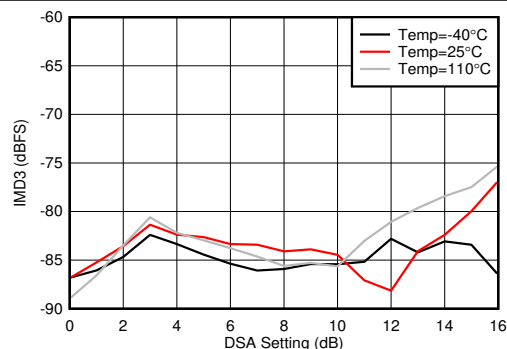
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

Figure 7-368. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching, $f_{\text{IN}} = 3610\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$

Figure 7-369. RX Output FFT at 3.6 GHz

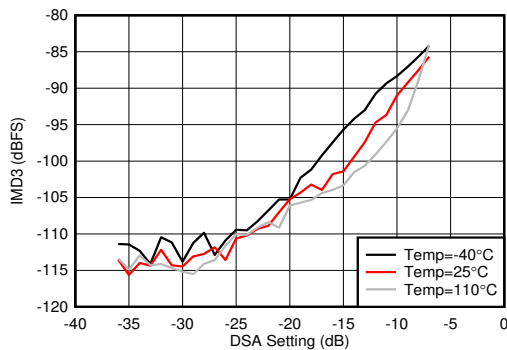


With 3.5 GHz matching, each tone at -7 dBFS , 20-MHz tone spacing

Figure 7-370. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

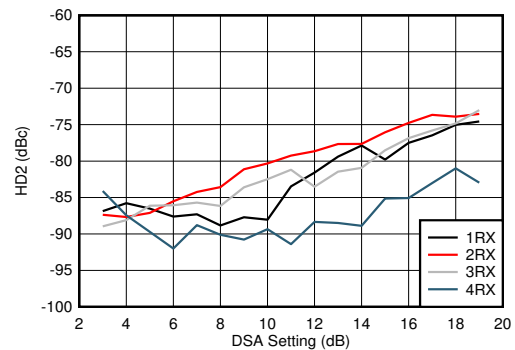
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



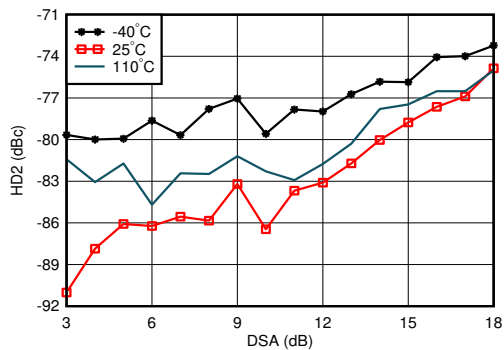
With 3.5 GHz matching, 20-MHz tone spacing

Figure 7-371. RX IMD3 vs Input Level and Temperature at 3.6 GHz



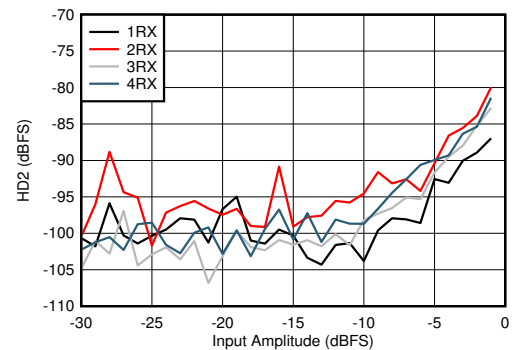
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-372. RX HD2 vs DSA Setting and Channel at 3.6 GHz



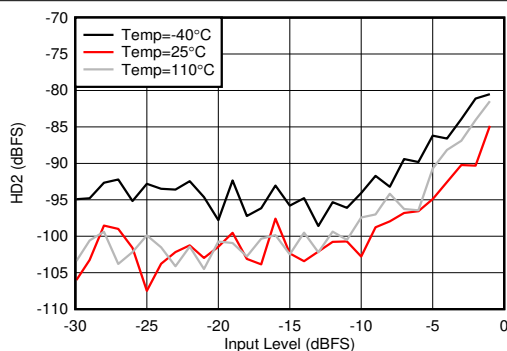
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-373. RX HD2 vs DSA Setting and Temperature at 3.6 GHz



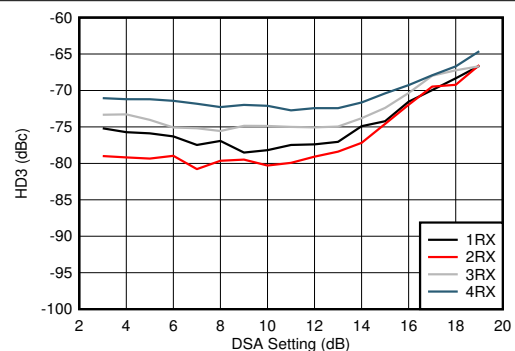
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-374. RX HD2 vs Input Level and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-375. RX HD2 vs Input Level and Temperature at 3.6 GHz

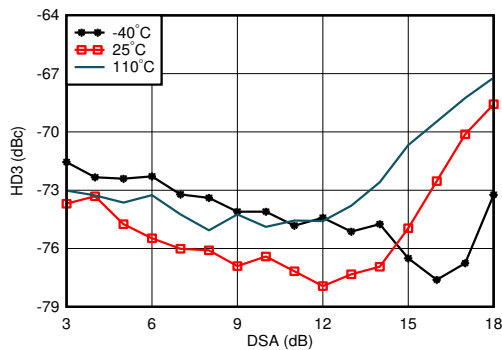


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-376. RX HD3 vs DSA Setting and Channel at 3.6 GHz

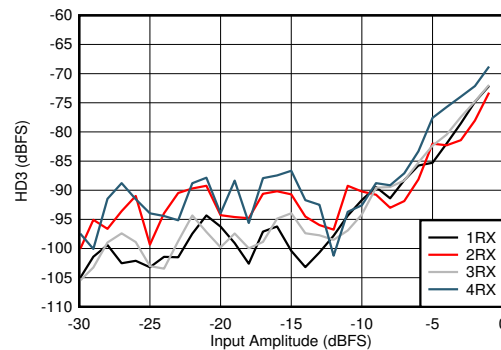
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



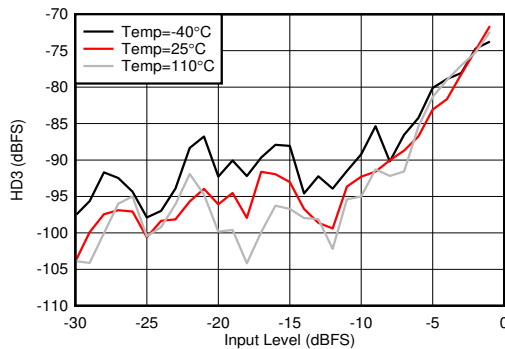
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-377. RX HD3 vs DSA Setting and Temperature at 3.6 GHz



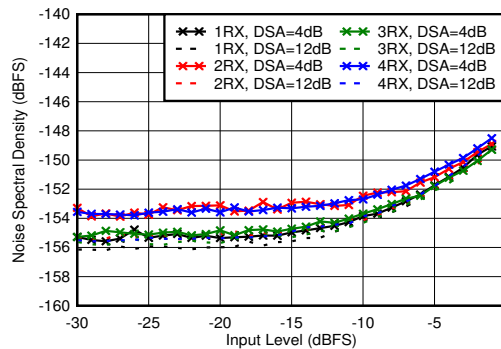
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-378. RX HD3 vs Input Level and Channel at 3.6 GHz



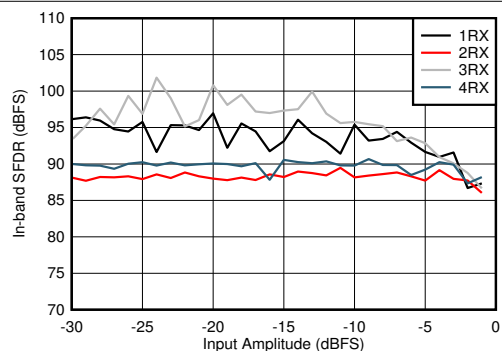
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-379. RX HD3 vs Input Level and Temperature at 3.6 GHz



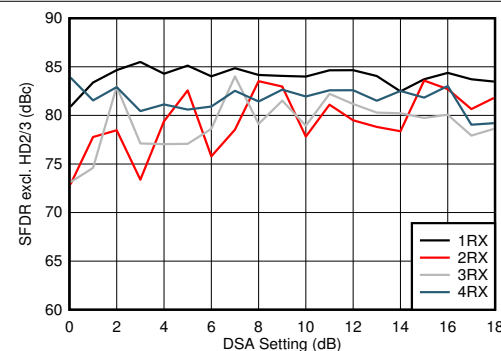
With 3.5 GHz matching, 12.5-MHz offset from tone

Figure 7-380. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



With 3.5 GHz matching

Figure 7-381. RX In-Band SFDR ($\pm 200\text{ MHz}$) vs Input Level and Channel at 3.6 GHz

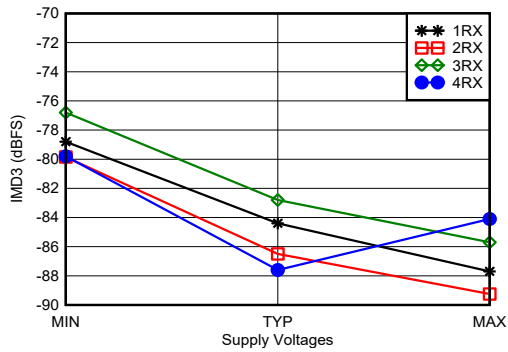


With 3.5 GHz matching

Figure 7-382. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz

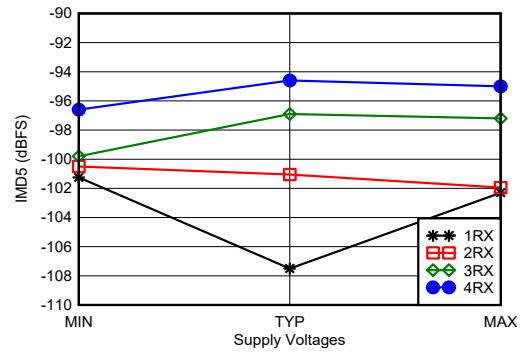
7.12.11 RX Typical Characteristics at 3.5 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



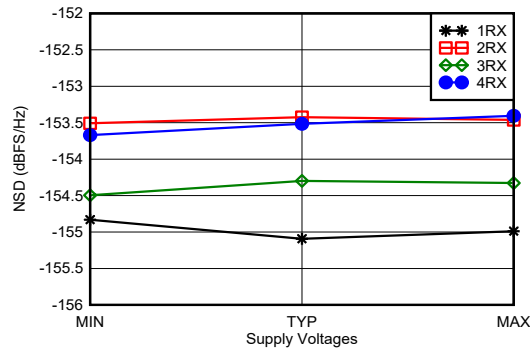
With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-383. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-384. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

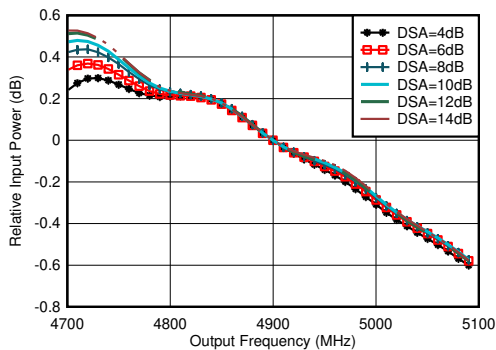


With 3.6 GHz matching, tone at -20 dBFS , 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-385. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

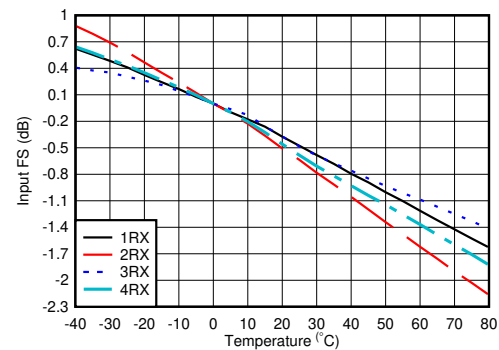
7.12.12 RX Typical Characteristics at 4.9 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



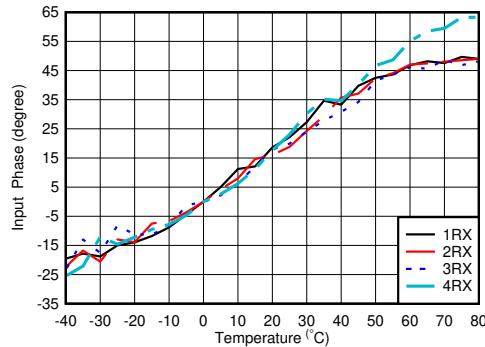
With matching, normalized to power at 4.9 GHz for each DSA setting

Figure 7-386. RX Inband Gain Flatness, $f_{\text{IN}} = 4900\text{ MHz}$



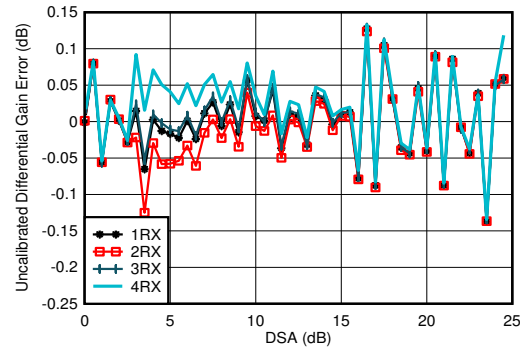
With 4.9 GHz matching, normalized to fullscale at 25°C for each channel

Figure 7-387. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at 25°C

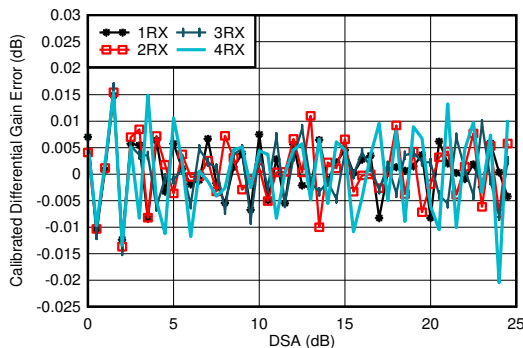
Figure 7-388. RX Input Phase vs Temperature and DSA at $f_{\text{OUT}} = 4.9\text{ GHz}$



With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

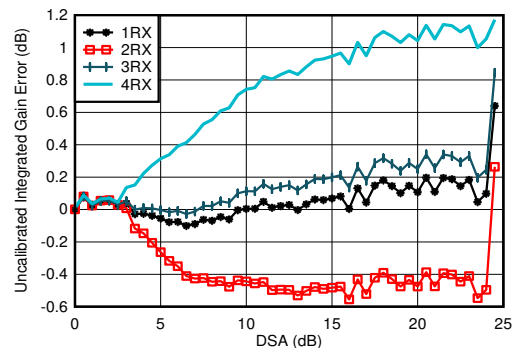
Figure 7-389. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Amplitude Error = $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

Figure 7-390. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



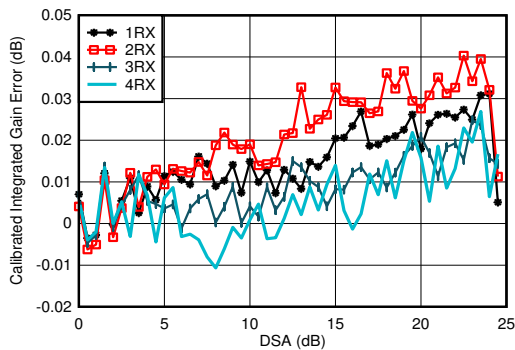
With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

Figure 7-391. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

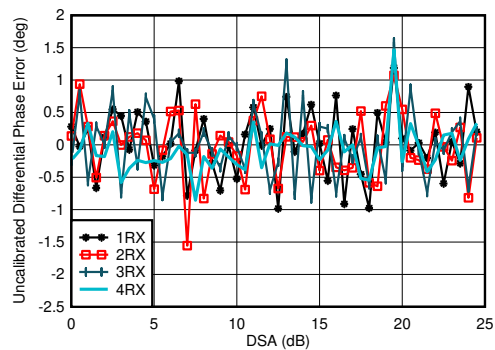
Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 4 dB.



With 4.9 GHz matching

Integrated Amplitude Error = $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

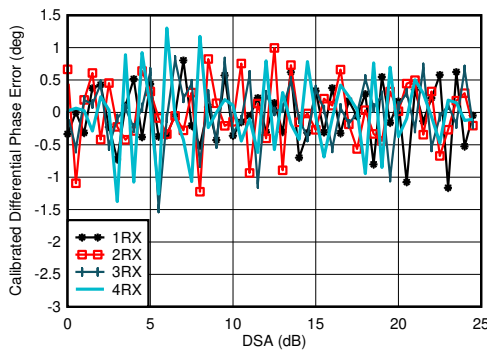
Figure 7-392. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

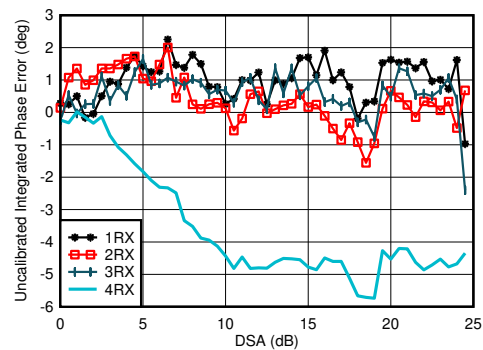
Figure 7-393. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Differential Phase Error = $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

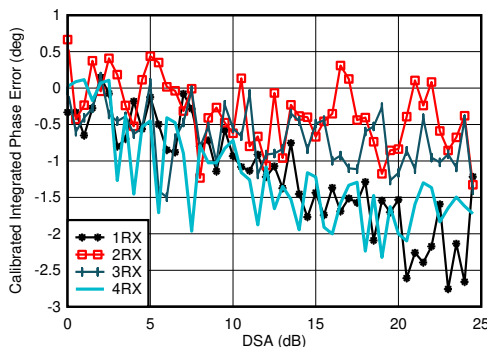
Figure 7-394. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

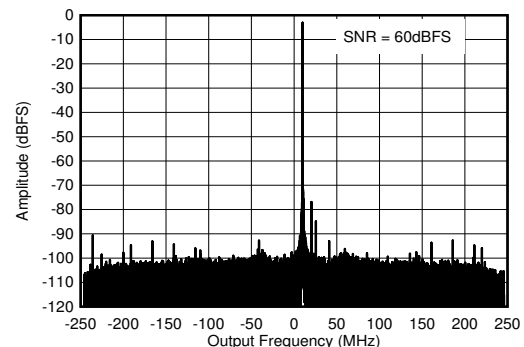
Figure 7-395. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

Integrated Phase Error = $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

Figure 7-396. RX Calibrated Integrated Phase Error vs DSA Setting at 4.9 GHz

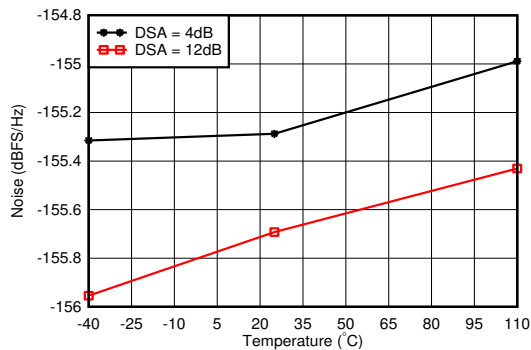


With 4.9 GHz matching, $f_{\text{IN}} = 4910 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$

Figure 7-397. RX Output FFT at 4.9 GHz

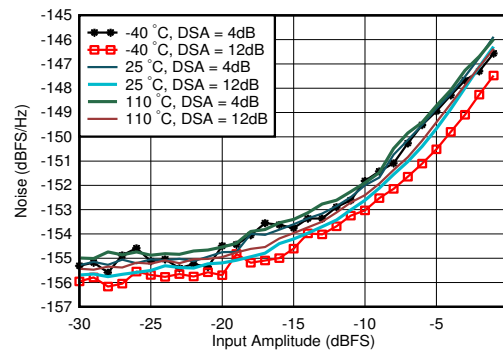
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



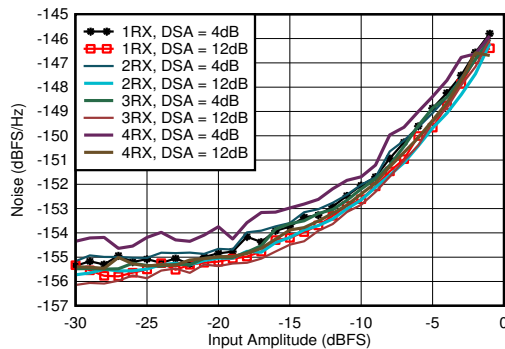
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 7-398. RX Noise Spectral Density vs Temperature at 4.9 GHz



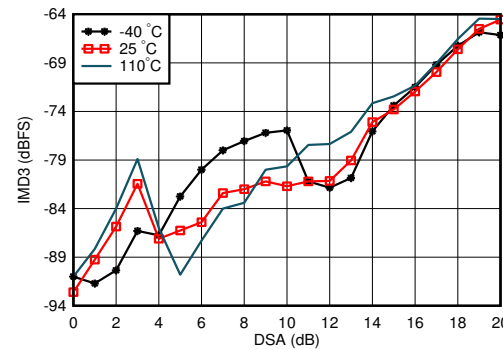
With 4.9 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

Figure 7-399. RX Noise Spectral Density vs Input Amplitude and Temperature at 4.9 GHz



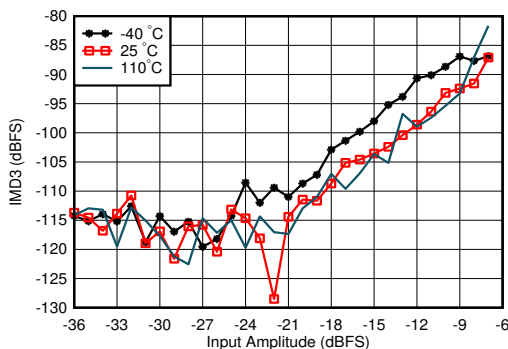
With 4.9 GHz matching, 12.5-MHz offset from tone

Figure 7-400. RX Noise Spectral Density vs Input Amplitude and Channel at 4.9 GHz



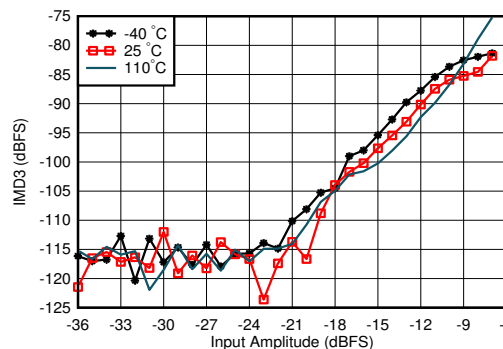
With 4.9 GHz matching, each tone -7 dBFS , tone spacing = 20 MHz

Figure 7-401. RX IMD3 vs DSA Setting and Temperature at 4.9 GHz



With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

Figure 7-402. RX IMD3 vs Input Level and Temperature at 4.9 GHz

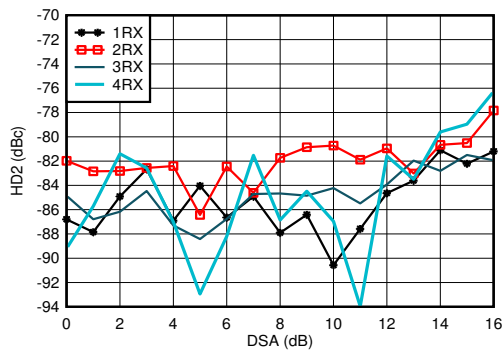


With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

Figure 7-403. RX IMD3 vs Input Level and Temperature at 4.9 GHz

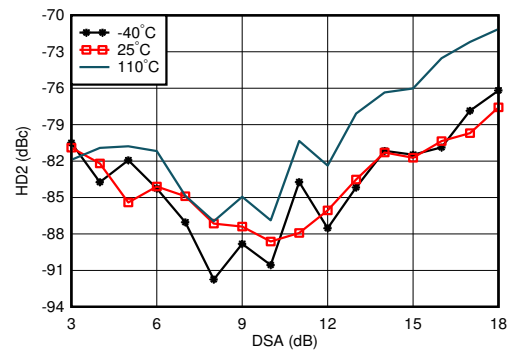
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



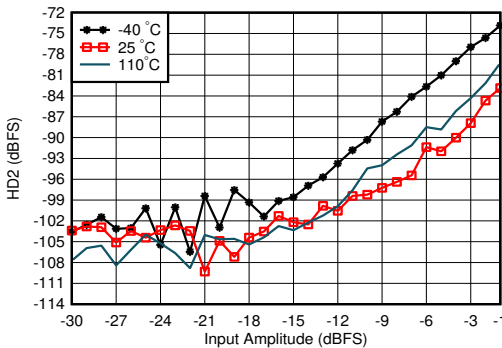
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-404. RX HD2 vs DSA Setting and Channel at 4.9 GHz



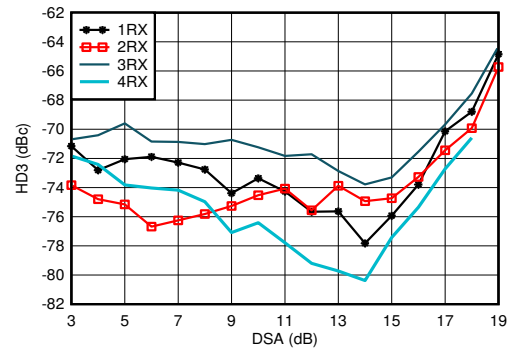
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-405. RX HD2 vs DSA and Temperature at 4.9 GHz



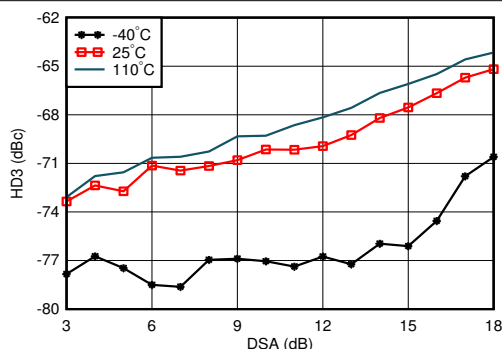
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

Figure 7-406. RX HD2 vs Input Level and Temperature at 4.9 GHz



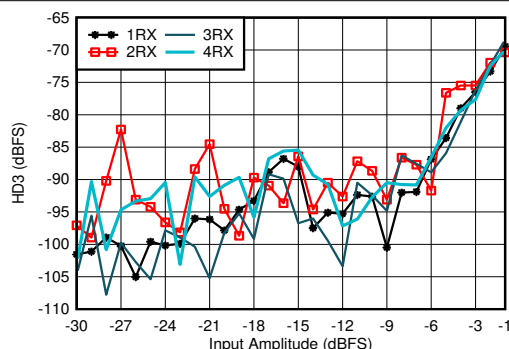
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-407. RX HD3 vs DSA Setting and Channel at 4.9 GHz



With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-408. RX HD3 vs DSA Setting and Temperature at 4.9 GHz

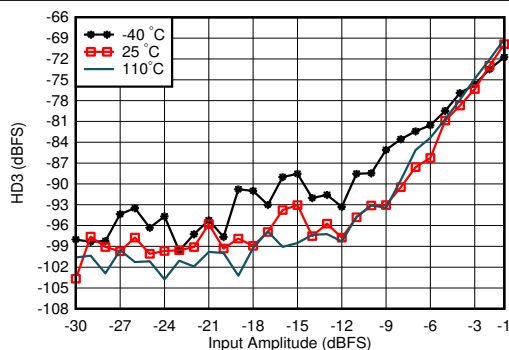


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-409. RX HD3 vs Input Level and Channel at 4.9 GHz

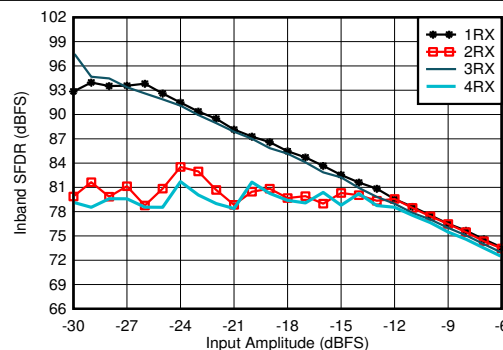
7.12.12 RX Typical Characteristics at 4.9 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 491.52 MSPS (decimate by 6), PLL clock mode with $f_{\text{REF}} = 491.52\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 4 dB.



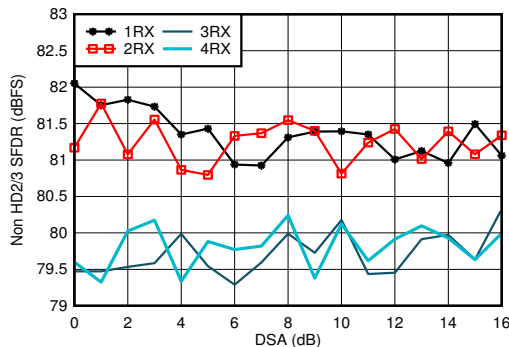
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

Figure 7-410. RX HD3 vs Input Level and Temperature at 4.9 GHz



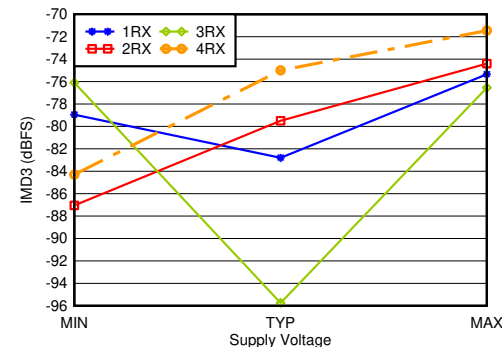
With 4.9 GHz matching, decimate by 3

Figure 7-411. RX In-Band SFDR ($\pm 400\text{ MHz}$) vs Input Amplitude and Channel at 4.9 GHz



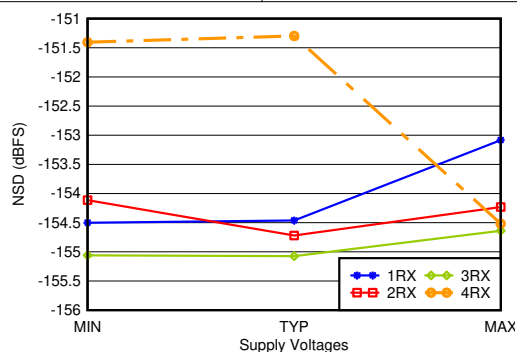
With 4.9 GHz matching

Figure 7-412. RX Non-HD2/3 vs DSA Setting at 4.9 GHz



With 4.9 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-413. RX IMD3 vs Supply and Channel at 4.9 GHz



With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

Figure 7-414. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 8.1 GHz matching.

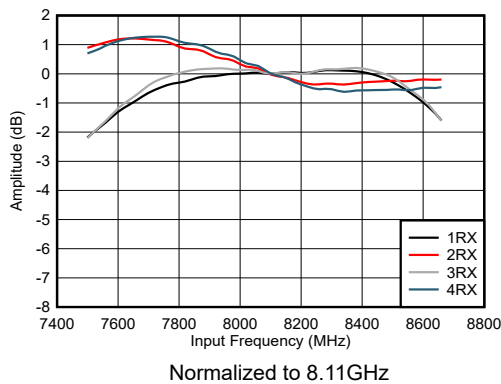


Figure 7-415. RX Amplitude vs Frequency and Channel

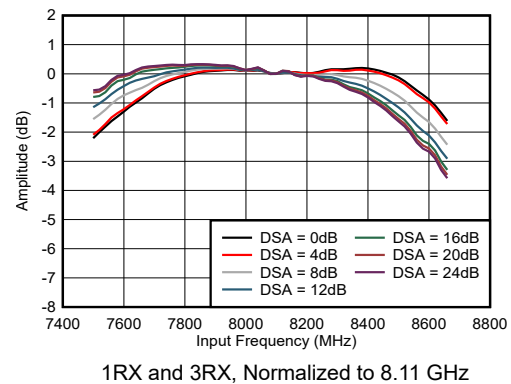


Figure 7-416. RX Amplitude vs Frequency and DSA Setting

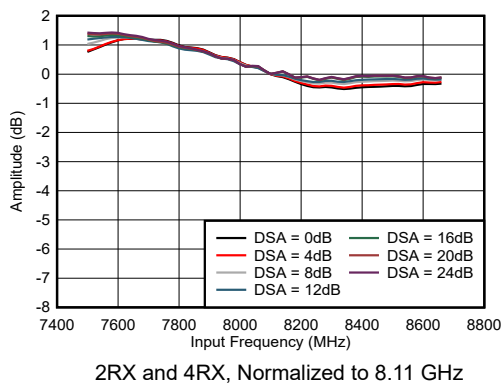


Figure 7-417. RX Amplitude vs Frequency and DSA Setting

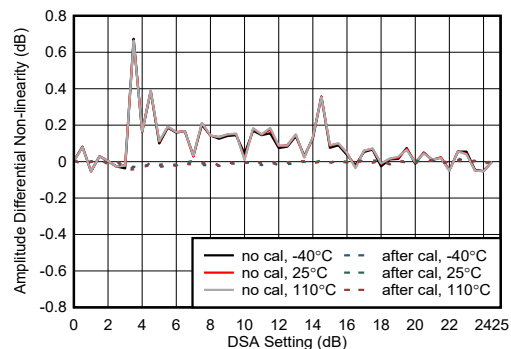


Figure 7-418. RX Amplitude Differential Nonlinearity at 8.11 GHz

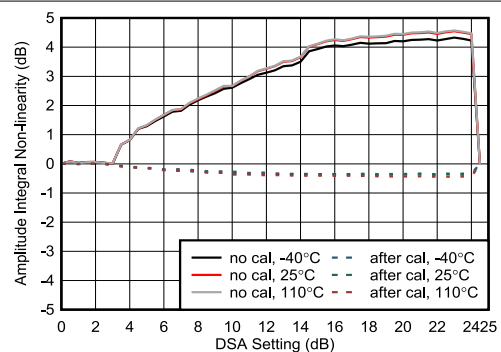


Figure 7-419. RX Amplitude Integrated Nonlinearity at 8.11 GHz

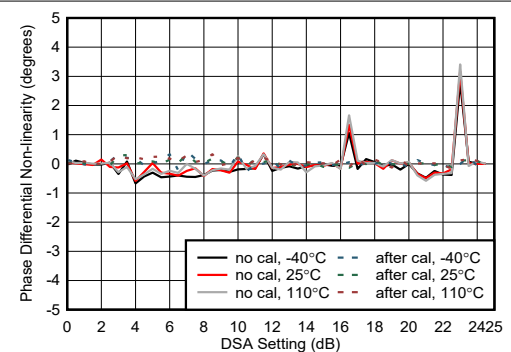


Figure 7-420. RX Phase Differential Nonlinearity at 8.11 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1 GHz matching.

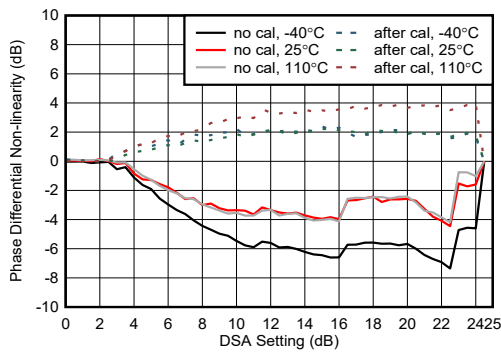


Figure 7-421. RX Phase Differential Nonlinearity at 8.1 GHz

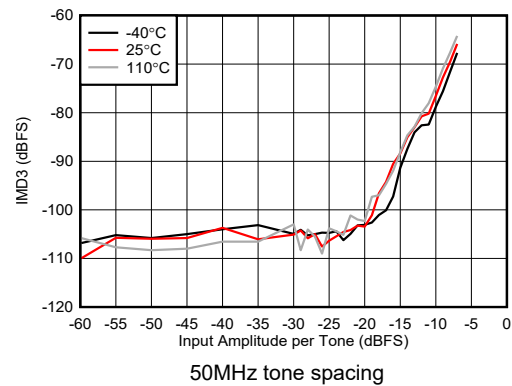


Figure 7-422. RX IMD3 vs Input Amplitude at 8.1 GHz

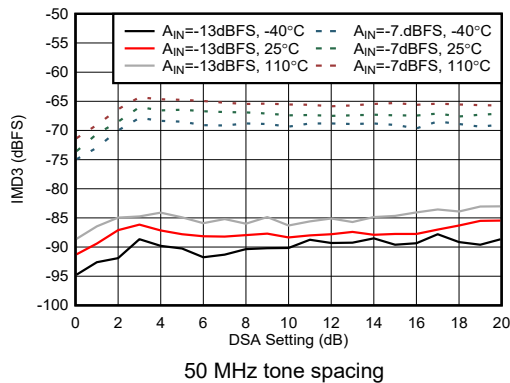


Figure 7-423. RX IMD3 vs DSA Setting at 8.1 GHz

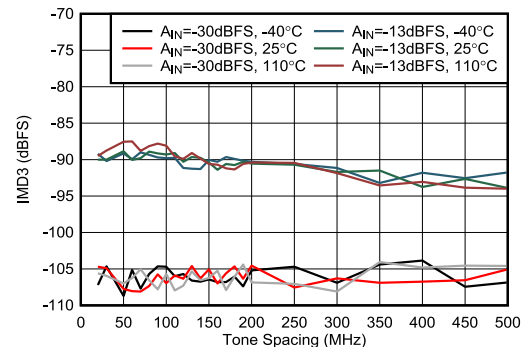


Figure 7-424. RX IMD3 vs Tone Spacing at 8.1 GHz

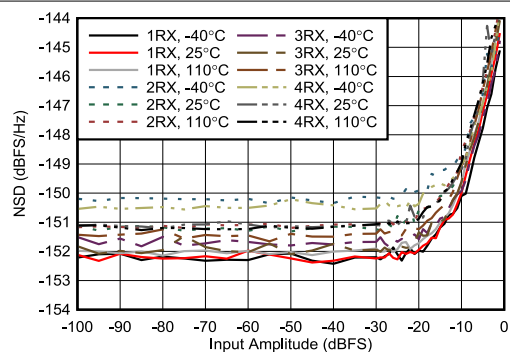


Figure 7-425. RX NSD vs Digital Amplitude at 8.1 GHz

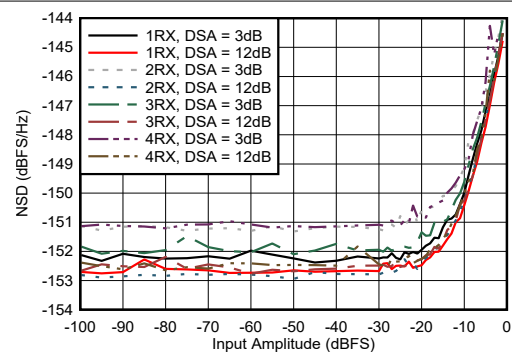


Figure 7-426. RX NSD vs Digital Amplitude at 8.1 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 8.1 GHz matching.

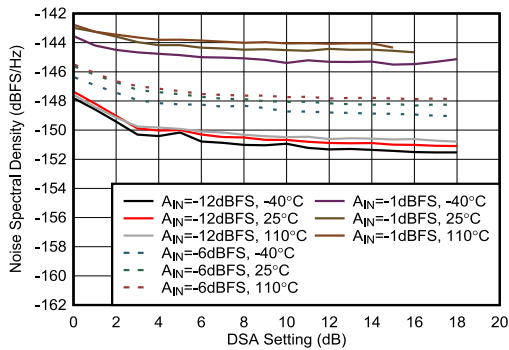
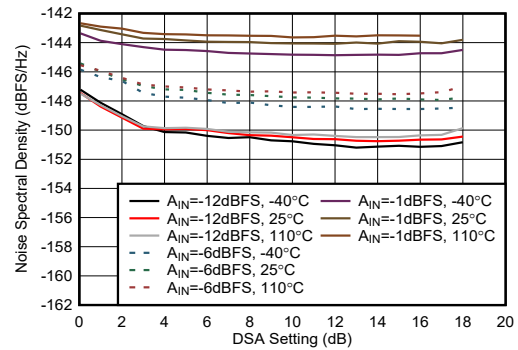


Figure 7-427. RX NSD vs DSA Setting at 8.1 GHz



External clock mode

Figure 7-428. RX NSD vs DSA Setting at 8.1 GHz

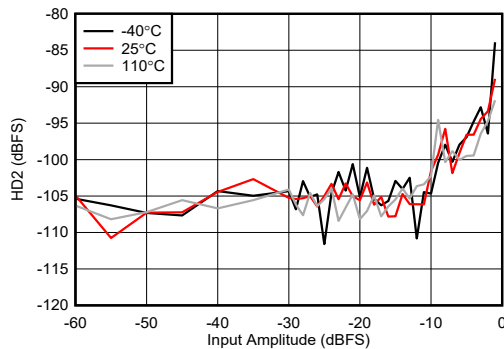


Figure 7-429. RX HD2 vs Digital Amplitude at 8.1 GHz

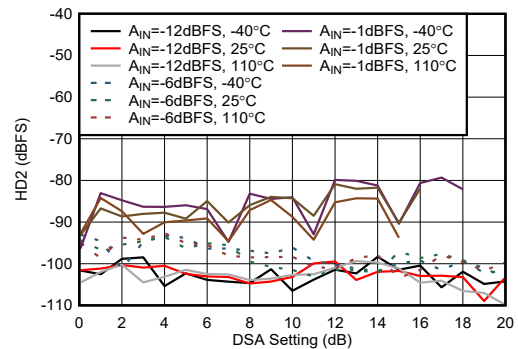


Figure 7-430. RX HD2 vs DSA Setting at 8.1 GHz

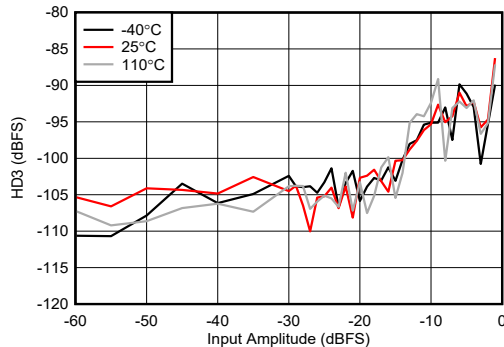


Figure 7-431. RX HD3 vs Digital Amplitude at 8.1 GHz

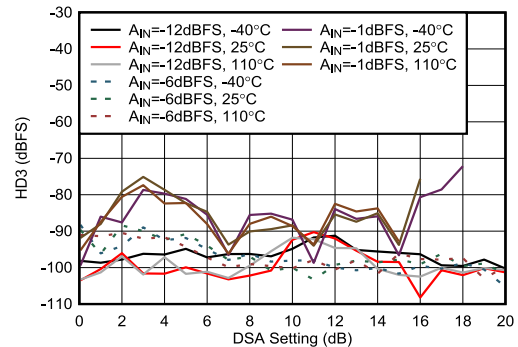


Figure 7-432. RX HD3 vs DSA Setting at 8.1 GHz

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 8.1 GHz matching.

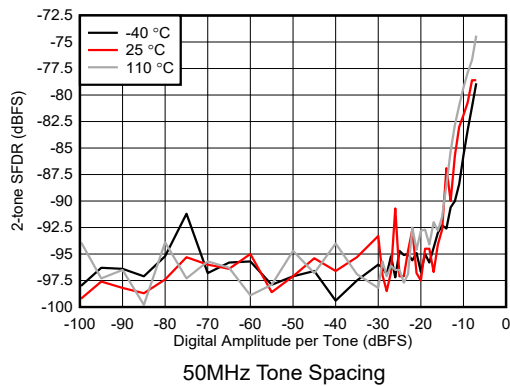


Figure 7-433. RX 2-tone SFDR vs Digital Amplitude at 8.1 GHz

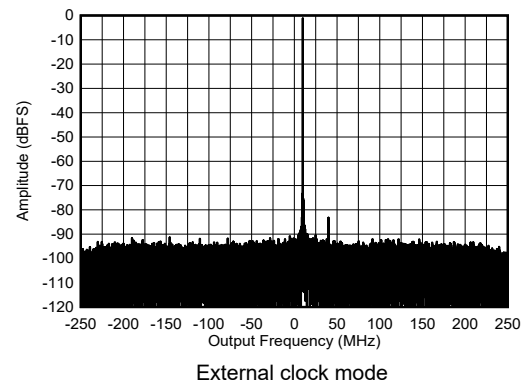


Figure 7-434. RX Single Tone Output FFT at 8.1 GHz, -1 dBFS

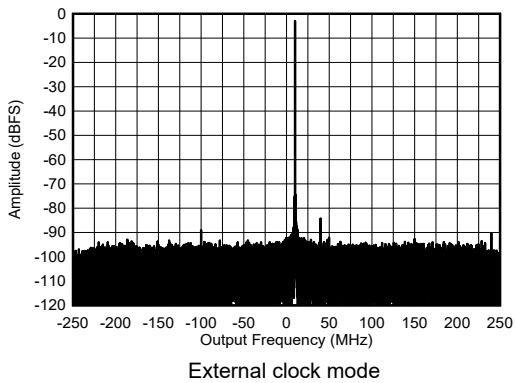


Figure 7-435. RX Single Tone Output FFT at 8.1 GHz, -3 dBFS

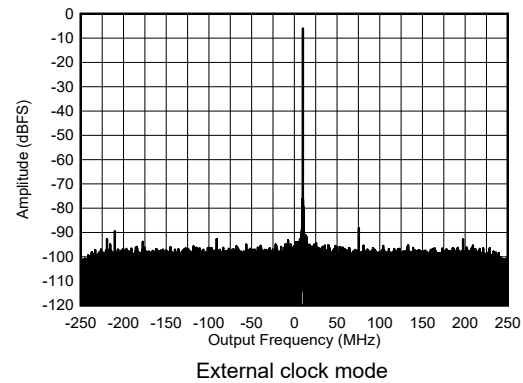


Figure 7-436. RX Single Tone Output FFT at 8.1 GHz, -6 dBFS

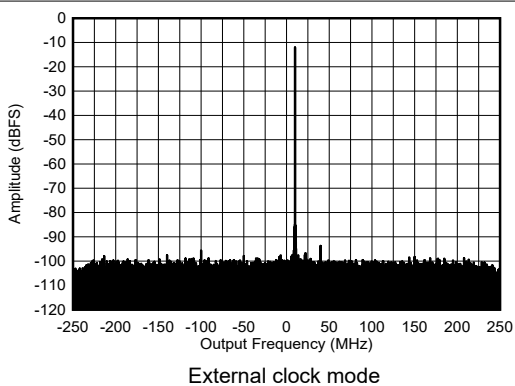


Figure 7-437. RX Single Tone Output FFT at 8.1 GHz, -12 dBFS

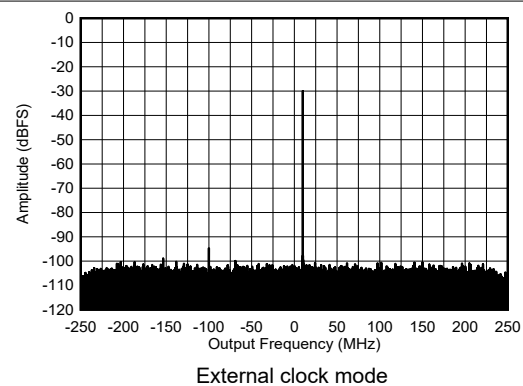


Figure 7-438. RX Single Tone Output FFT at 8.1 GHz, -30 dBFS

7.12.13 RX Typical Characteristics at 8.1 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 8.1 GHz matching.

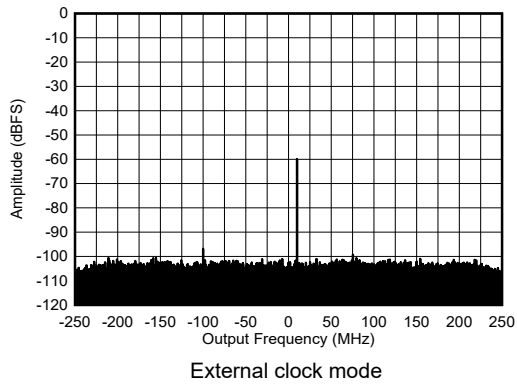


Figure 7-439. RX Single Tone Output FFT at 8.1 GHz, -60 dBFS

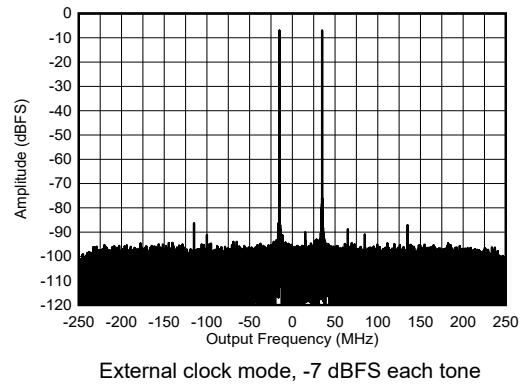


Figure 7-440. RX Dual Tone Output FFT at 8.1 GHz

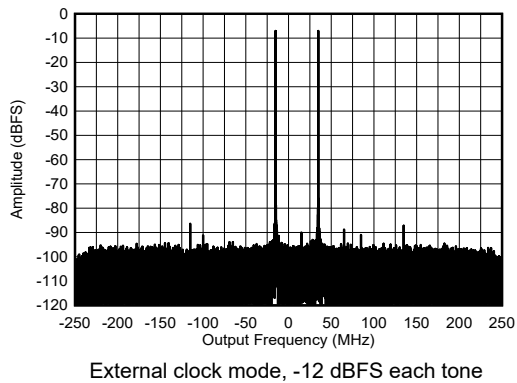


Figure 7-441. RX Dual Tone Output FFT at 8.1 GHz

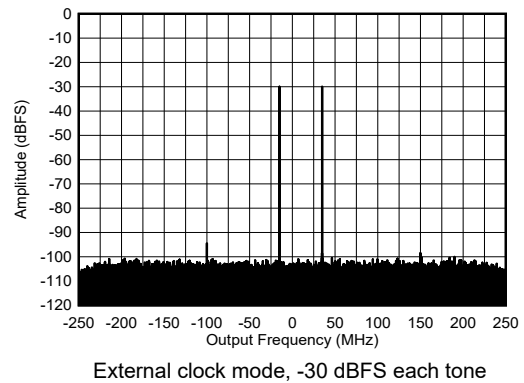


Figure 7-442. RX Dual Tone Output FFT at 8.1 GHz

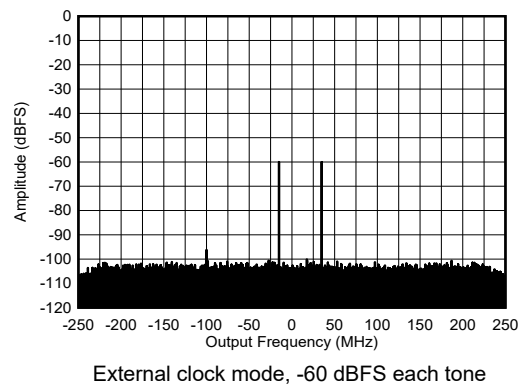
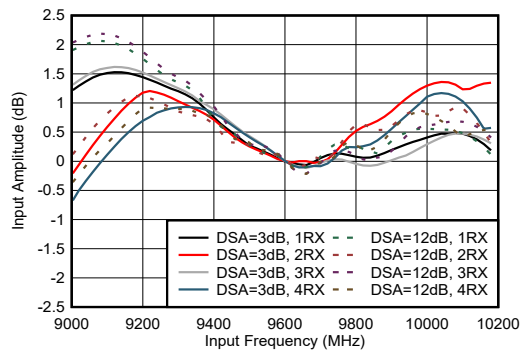


Figure 7-443. RX Dual Tone Output FFT at 8.1 GHz

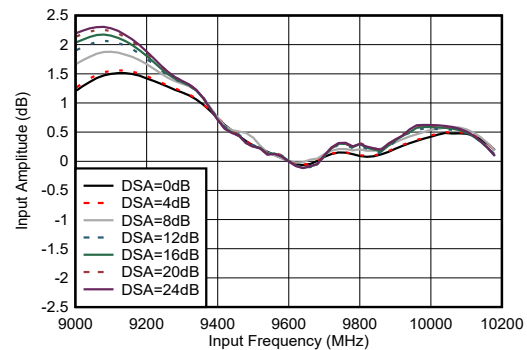
7.12.14 RX Typical Characteristics at 9.6 GHz

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.



Normalized to 9.6 GHz RX Input Amplitude vs Frequency at 9.6

Figure 7-444. RX Input Amplitude vs Frequency



Normalized to 9.6 GHz

Figure 7-445. GHZ

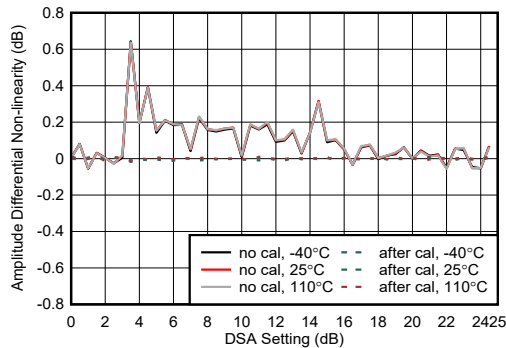


Figure 7-446. RX Amplitude Differential Non-linearity at 9.6 GHz

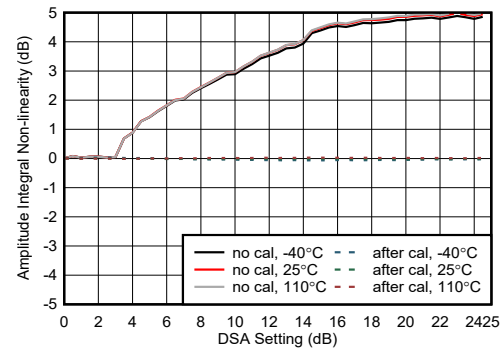


Figure 7-447. RX Amplitude Integrated Non-linearity at 9.6 GHz

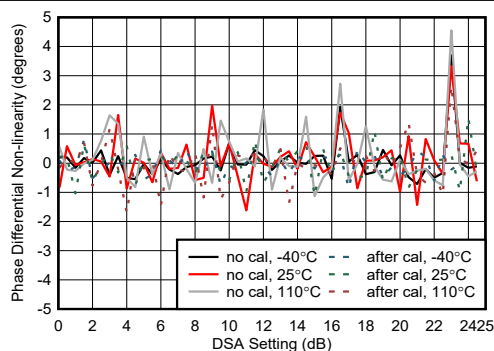


Figure 7-448. RX Phase Differential Non-linearity at 9.6 GHz

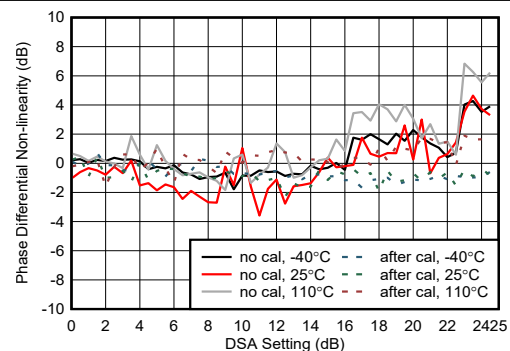


Figure 7-449. RX Phase Integrated Non-linearity at 9.6 GHz

7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.

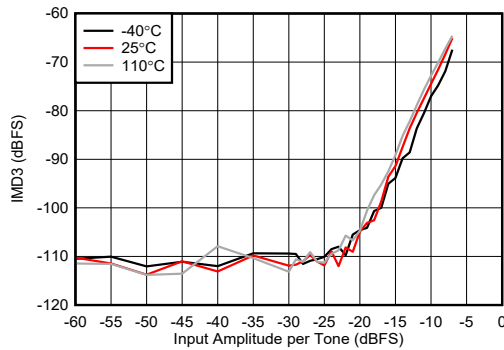


Figure 7-450. RX IMD3 vs Digital Amplitude at 9.6 GHz

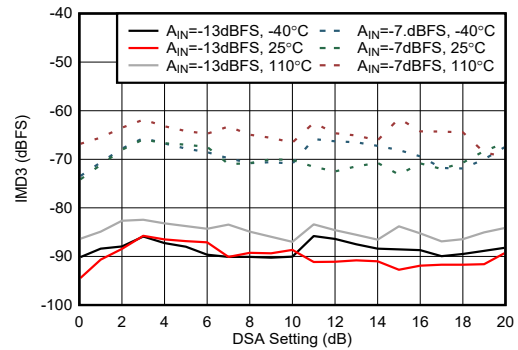


Figure 7-451. RX IMD3 vs DSA Setting at 9.6 GHz

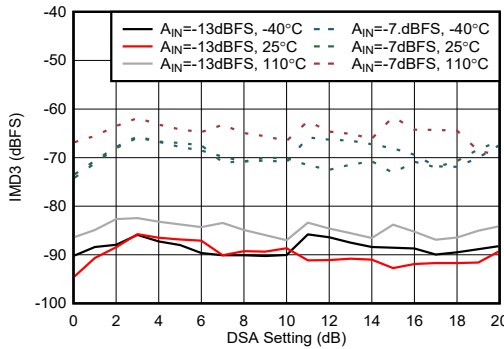


Figure 7-452. RX IMD3 vs DSA Setting at 9.6 GHz

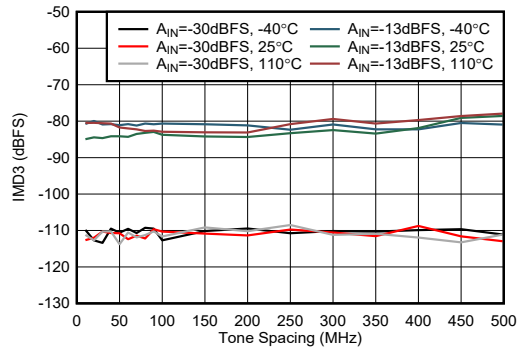


Figure 7-453. RX IMD3 vs Tone Spacing at 9.6 GHz

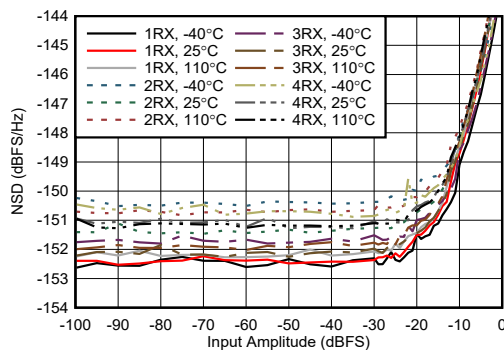


Figure 7-454. RX NSD vs Digital Amplitude at 9.6 GHz

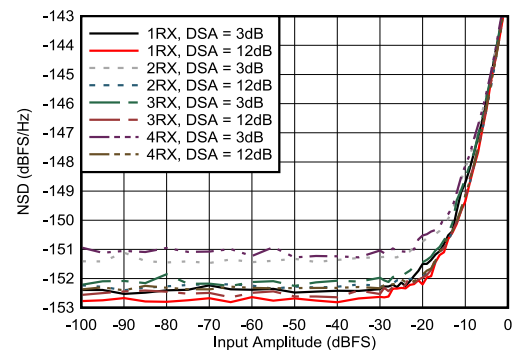


Figure 7-455. RX NSD vs Digital Amplitude at 9.6 GHz

7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48 \text{ MHz}$, $A_{\text{IN}} = -3 \text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.

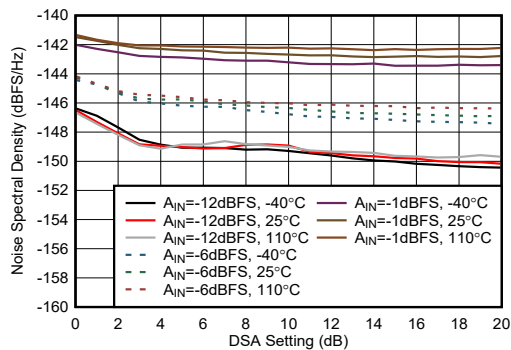


Figure 7-456. RX NSD vs DSA Setting at 9.6 GHz

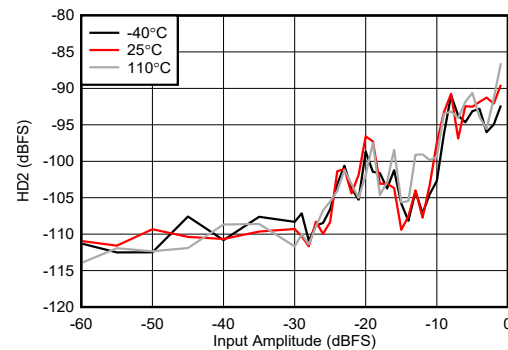


Figure 7-457. RX HD2 vs Digital Level at 9.6 GHz

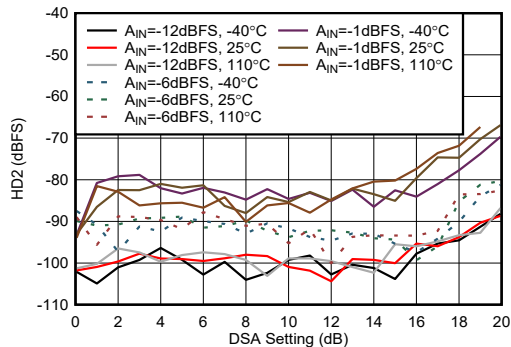


Figure 7-458. RX HD2 vs DSA Setting at 9.6 GHz

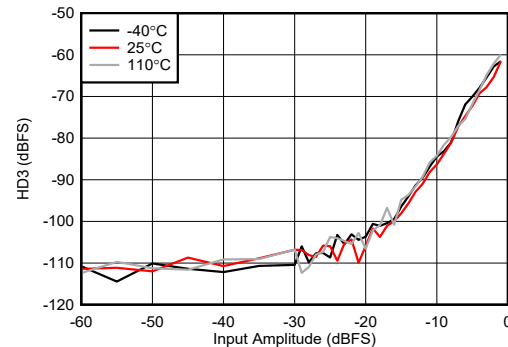


Figure 7-459. RX HD3 vs Digital Level at 9.6 GHz

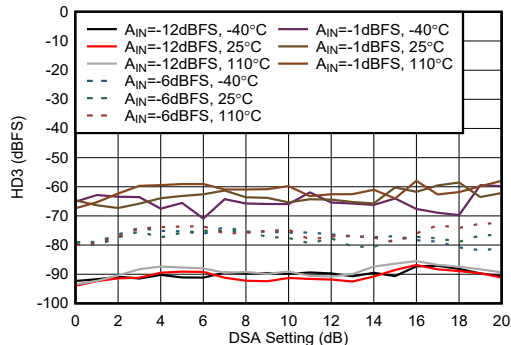
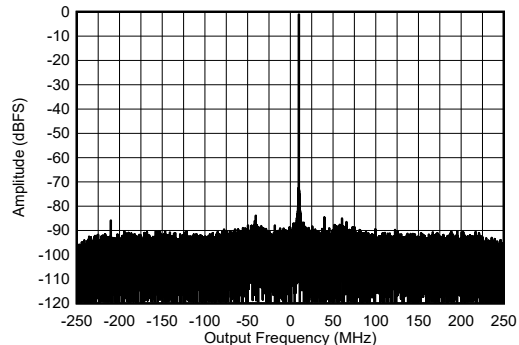


Figure 7-460. RX HD3 vs DSA Setting at 9.6 GHz

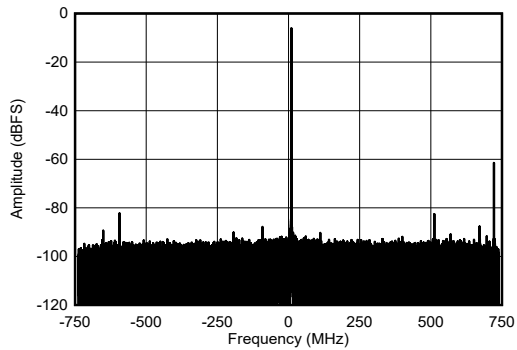


-1 dBFS

Figure 7-461. RX Single Tone Output FFT at 9.61 GHz

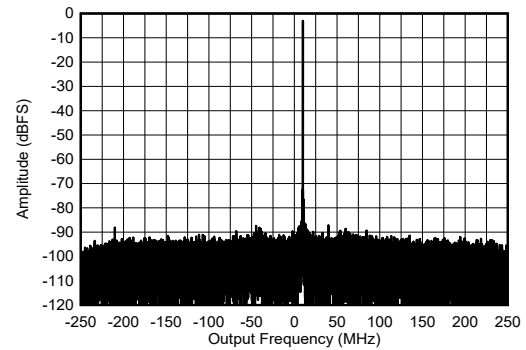
7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.



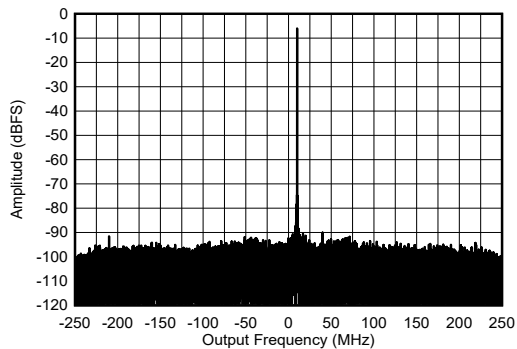
-6 dBFS

Figure 7-462. RX Single Tone Output FFT at 9.61 GHz



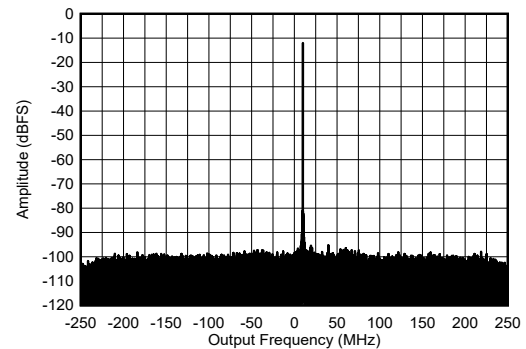
-3 dBFS

Figure 7-463. RX Single Tone Output FFT at 9.61 GHz



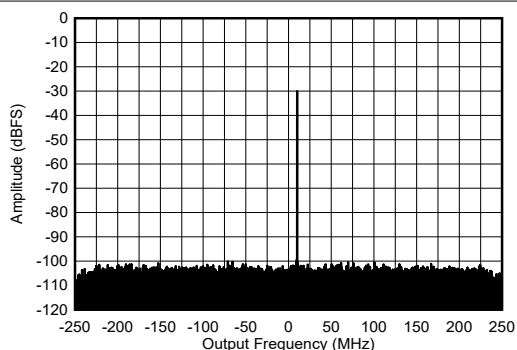
-6 dBFS

Figure 7-464. RX Single Tone Output FFT at 9.61 GHz



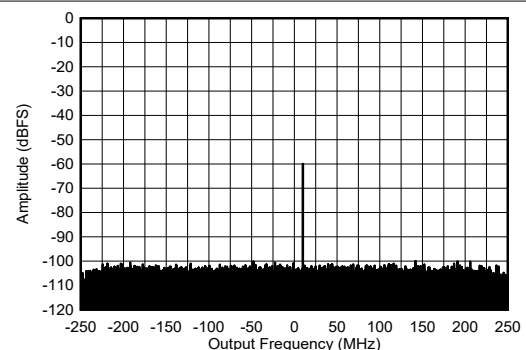
-12 dBFS

Figure 7-465. RX Single Tone Output FFT at 9.61 GHz



-30 dBFS

Figure 7-466. RX Single Tone Output FFT at 9.61 GHz

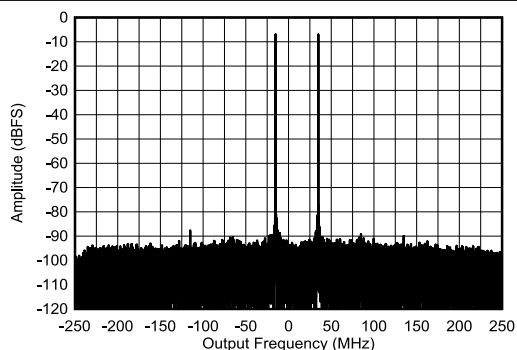


-60 dBFS

Figure 7-467. RX Single Tone Output FFT at 9.61 GHz

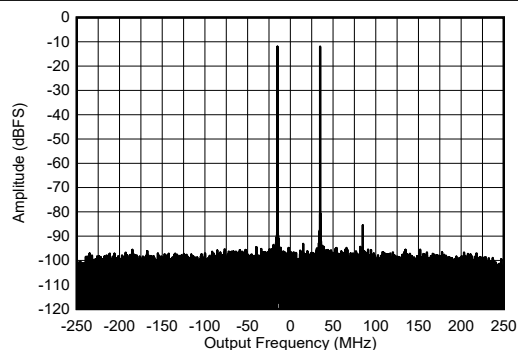
7.12.14 RX Typical Characteristics at 9.6 GHz (continued)

Typical values at $T_A = +25^\circ\text{C}$, ADC Sampling Rate = 2949.12 MHz. Default conditions: output sample rate = 1474.56 MSPS (decimate by 2), External clock mode with $f_{\text{CLK}} = 11796.48\text{ MHz}$, $A_{\text{IN}} = -3\text{ dBFS}$, DSA setting = 3 dB, 9.6 GHz matching.



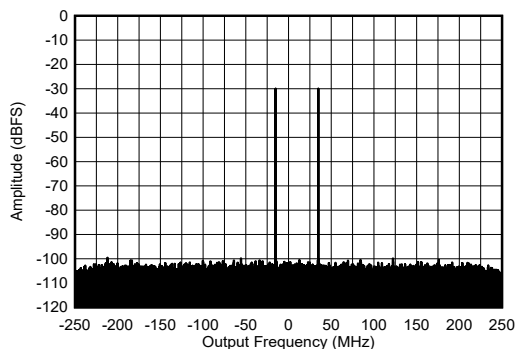
9.585 and 9.635 GHz, -7 dBFS each tone

Figure 7-468. RX Two Tone Output FFT at 9.61 GHz



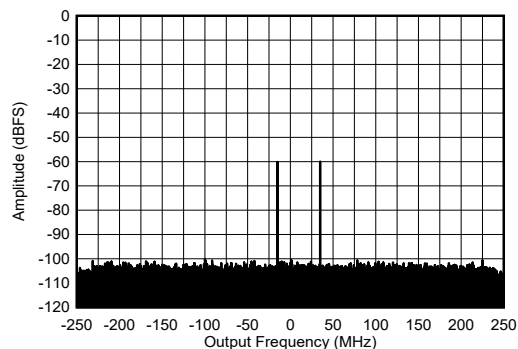
9.585 and 9.635 GHz, -12 dBFS each tone

Figure 7-469. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -30 dBFS each tone

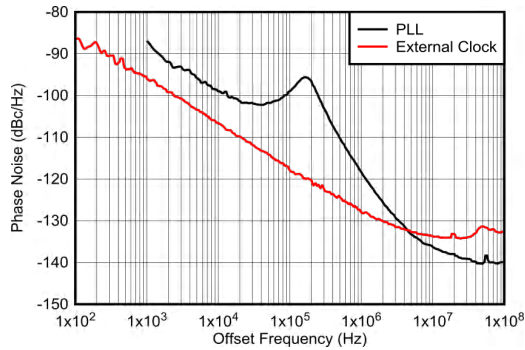
Figure 7-470. RX Two Tone Output FFT at 9.61 GHz



9.585 and 9.635 GHz, -60 dBFS each tone

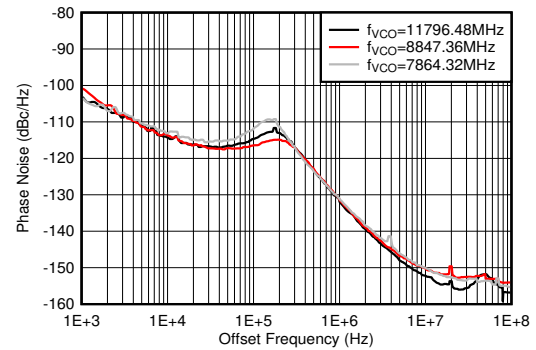
Figure 7-471. RX Two Tone Output FFT at 9.61 GHz

7.12.15 PLL and Clock Typical Characteristics



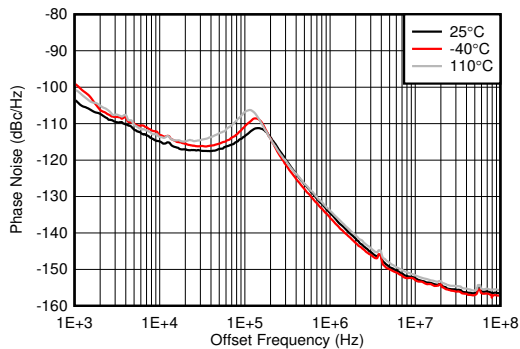
measured at TX output, normalized to 12 GHz by $20 \times \log_{10}(12\text{GHz}/f_{\text{OUT}})$

Figure 7-472. Phase Noise vs Offset Frequency for PLL and External Clock at 12 GHz



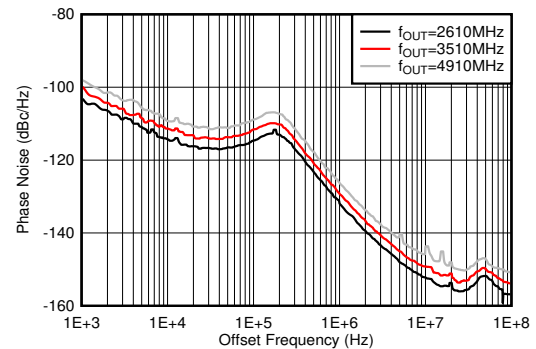
PLL enabled, $f_{\text{REF}} = 491.52$ MSPS, measured at TX output

Figure 7-473. Phase Noise vs Offset Frequency and f_{VCO} at $f_{\text{OUT}} = 2610$ MHz



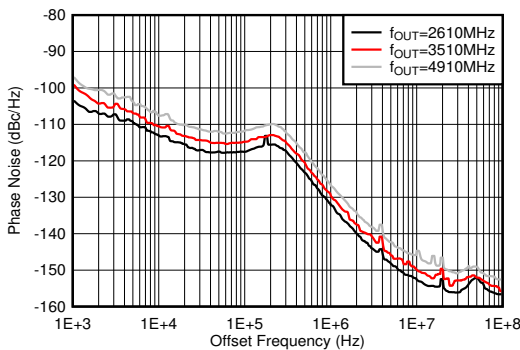
PLL enabled, $f_{\text{VCO}} = 11796.48$ MHz, $f_{\text{REF}} = 491.52$ MSPS, measured at TX output

Figure 7-474. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at $f_{\text{OUT}} = 1910$ MHz



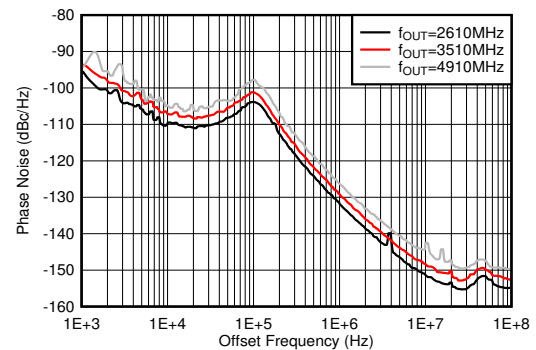
PLL enabled, $f_{\text{VCO}} = 11796.48$ MHz, $f_{\text{REF}} = 491.52$ MSPS, measured at TX output

Figure 7-475. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



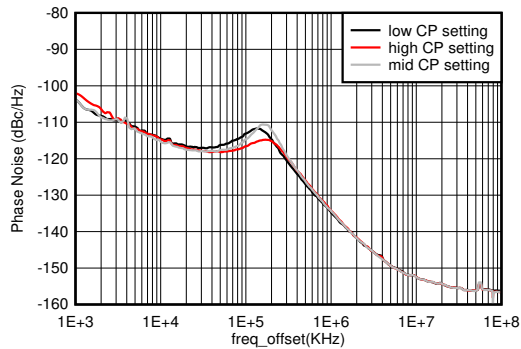
PLL enabled, $f_{\text{VCO}} = 11796.48$ MHz, $f_{\text{REF}} = 491.52$ MSPS, measured at TX output

Figure 7-476. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



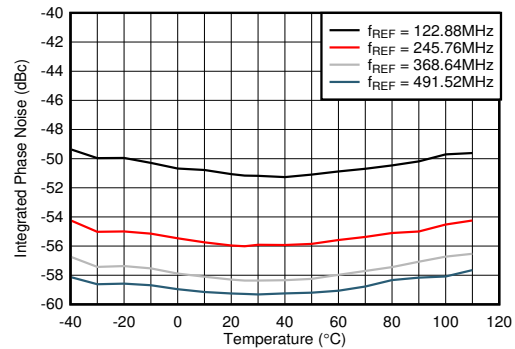
PLL enabled, $f_{\text{VCO}} = 11796.48$ MHz, $f_{\text{REF}} = 491.52$ MSPS, measured at TX output

Figure 7-477. Phase Noise for 12-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



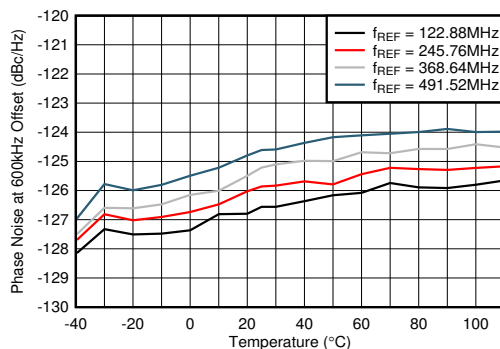
PLL enabled, $f_{VCO} = 11796.48$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-478. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at $f_{OUT} = 2.6$ GHz



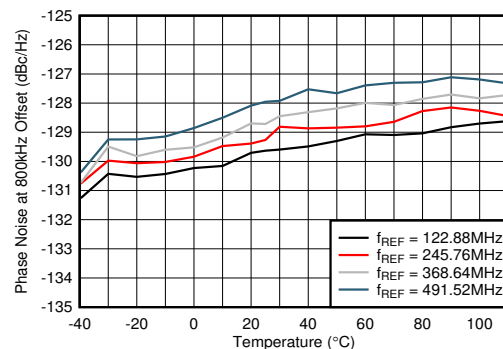
PLL enabled, $f_{VCO} = 11796.48$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

Figure 7-479. Integrated Phase Noise for 12-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



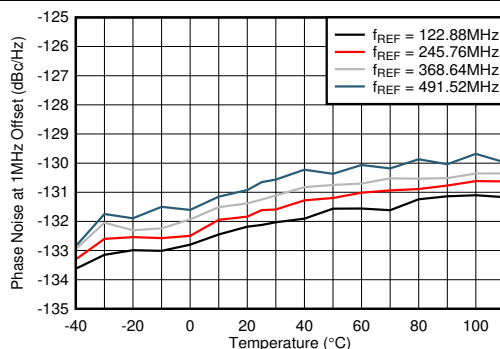
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-480. Phase Noise for 12-GHz VCO at 600 kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



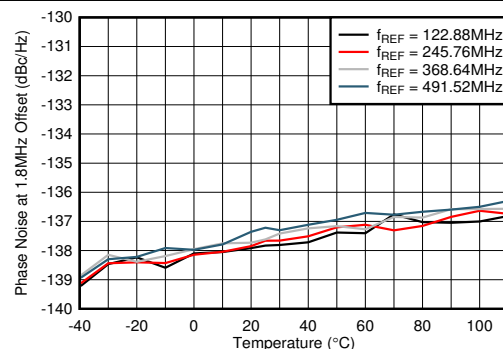
A. PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-481. Phase Noise for 12-GHz VCO at 800 kHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



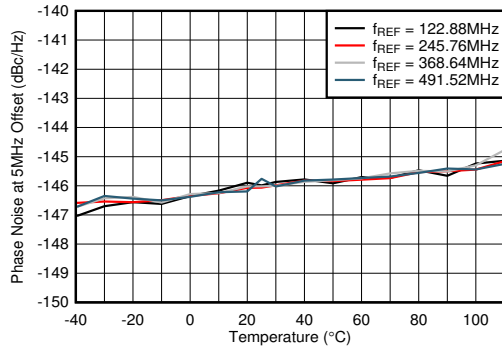
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-482. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



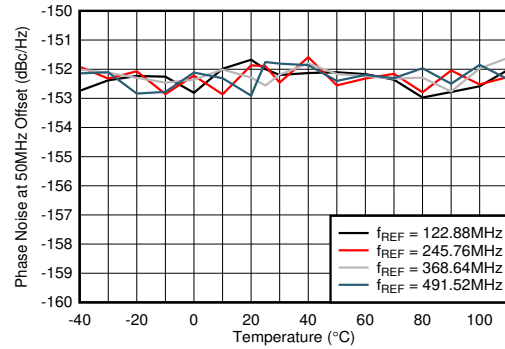
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-483. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



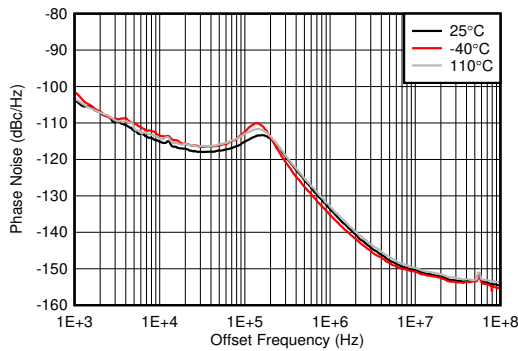
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-484. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



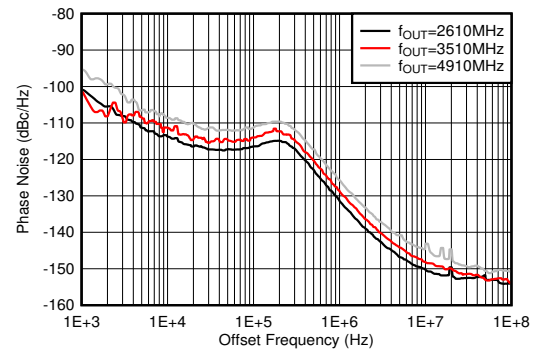
PLL enabled, $f_{VCO} = 11796.48$ MHz, measured at TX output

Figure 7-485. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



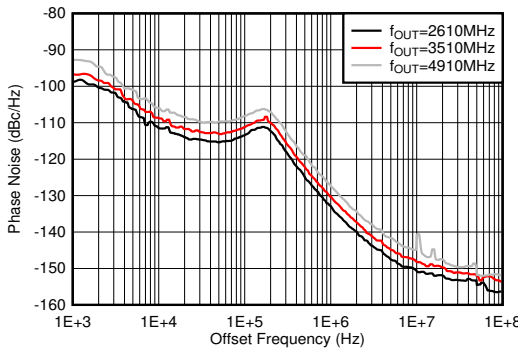
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-486. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



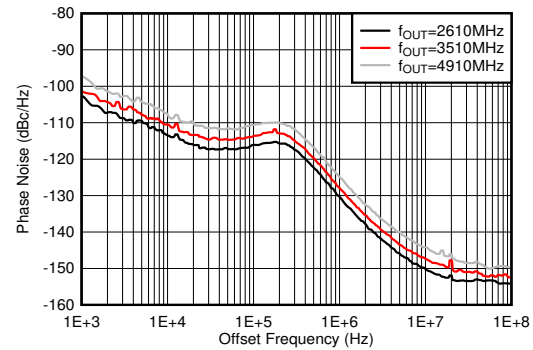
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-487. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



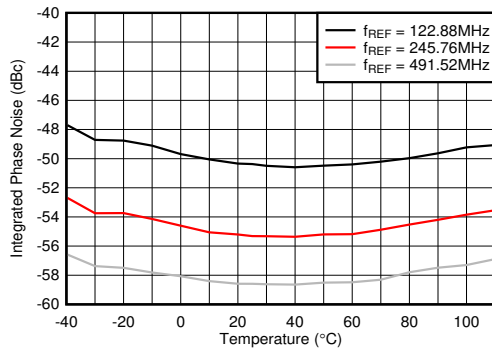
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-488. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



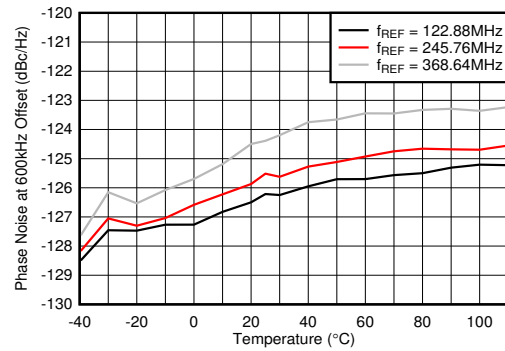
PLL enabled, $f_{VCO} = 9830.4$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-489. Phase Noise for 10-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



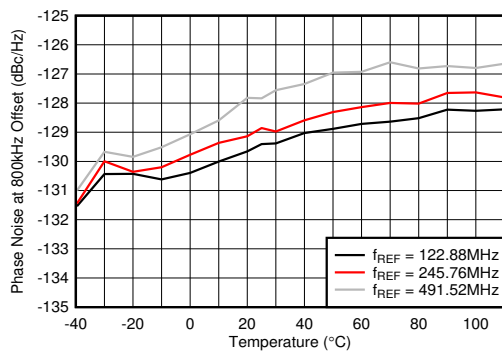
PLL enabled, $f_{VCO} = 9830.4$ MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at TX output

Figure 7-490. Integrated Phase Noise for 10-GHz VCO vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



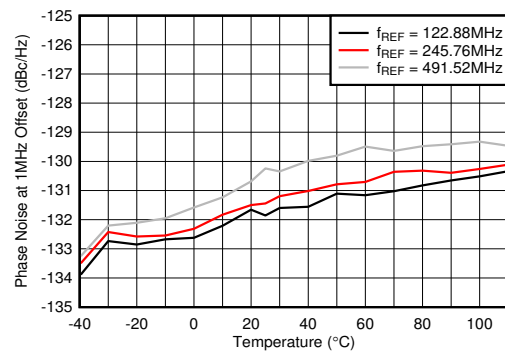
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-491. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



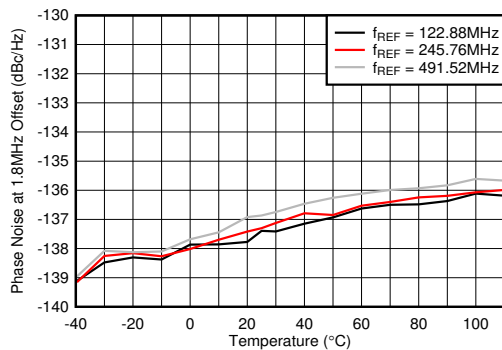
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-492. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



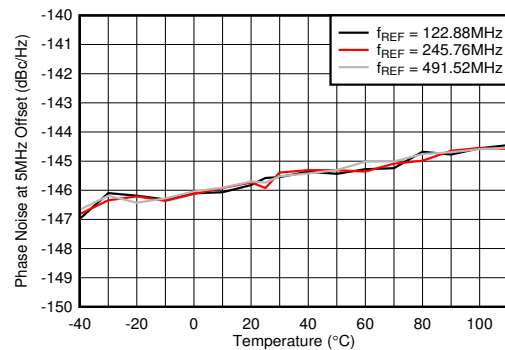
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-493. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



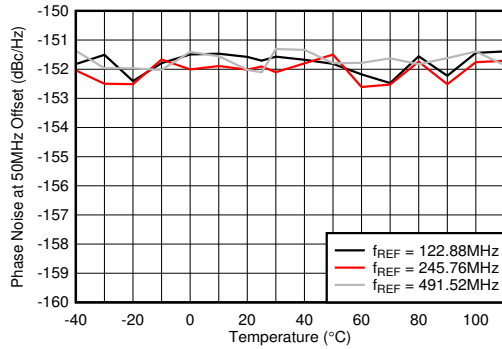
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-494. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



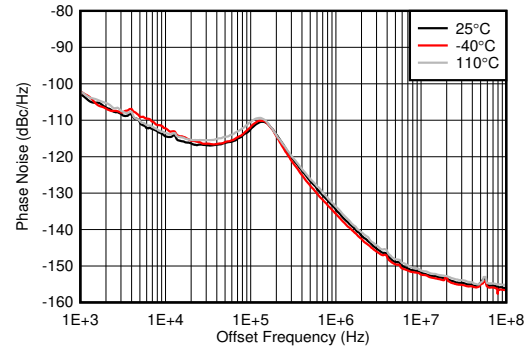
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-495. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



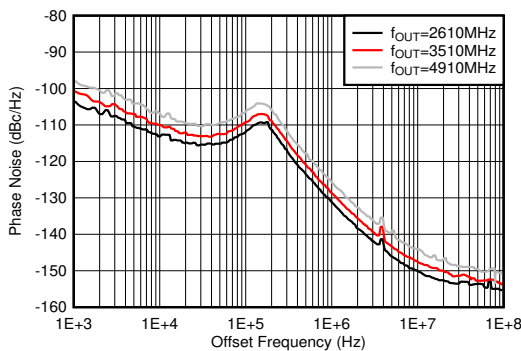
PLL enabled, $f_{VCO} = 9830.4$ MHz, measured at TX output

Figure 7-496. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f_{REF} at $f_{OUT} = 2.6$ GHz



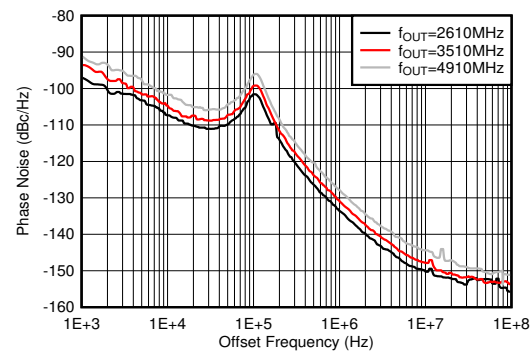
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-497. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz



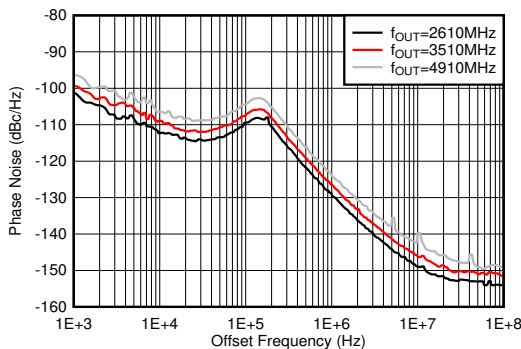
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-498. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 25°C



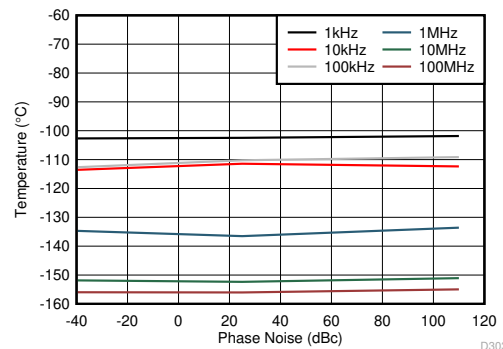
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-499. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at -40°C



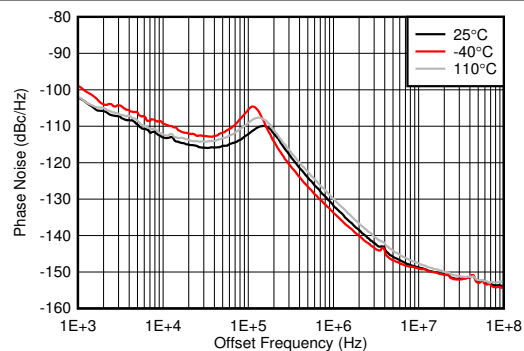
PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-500. Phase Noise for 9-GHz VCO vs Offset Frequency and f_{OUT} at 110°C



PLL enabled, $f_{VCO} = 8847.36$ MHz, $f_{REF} = 491.52$ MSPS, minimum LPF BW, measured at TX output

Figure 7-501. Phase Noise for 9-GHz VCO vs Temperature Over Offset Frequency at $f_{OUT} = 2.6$ GHz



PLL enabled, $f_{VCO} = 7864.32$ MHz, $f_{REF} = 491.52$ MSPS, measured at TX output

Figure 7-502. Phase Noise for 8-GHz VCO vs Offset Frequency and Temperature at $f_{OUT} = 1910$ MHz

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE7951IABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7951I	Samples
AFE7951IALK	ACTIVE	FCBGA	ALK	400	90	Non-RoHS & Green	Call TI	Level-3-220C-168 HR	-40 to 85	AFE7951 SNPB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

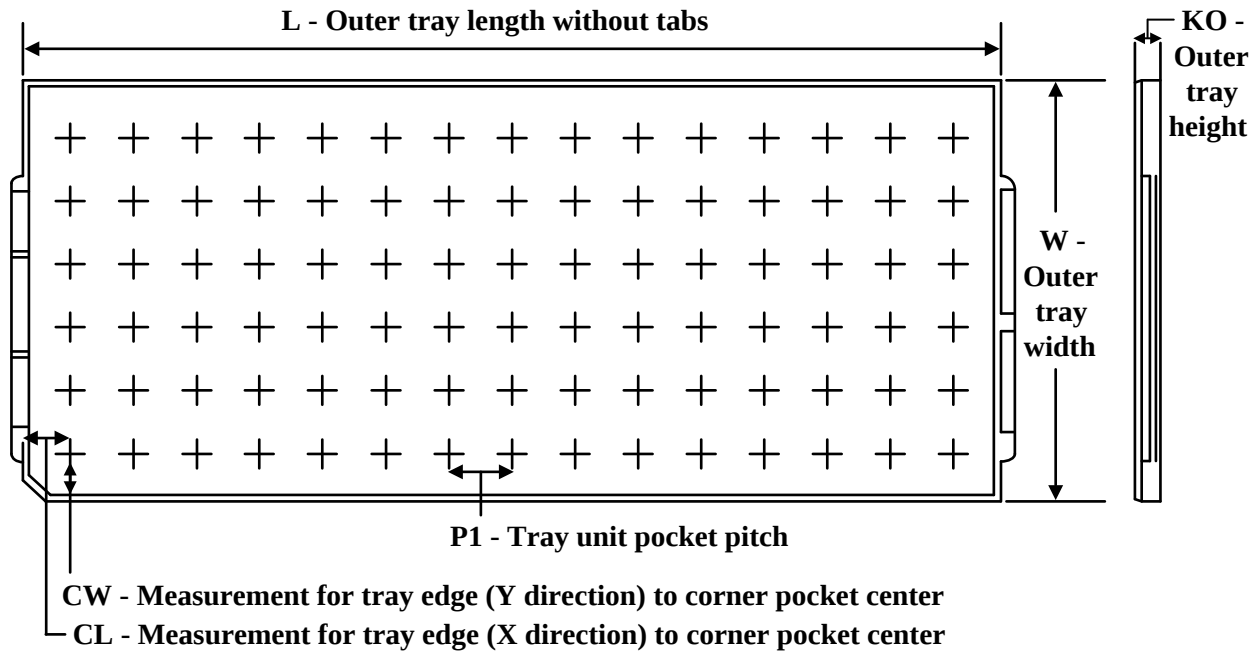
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

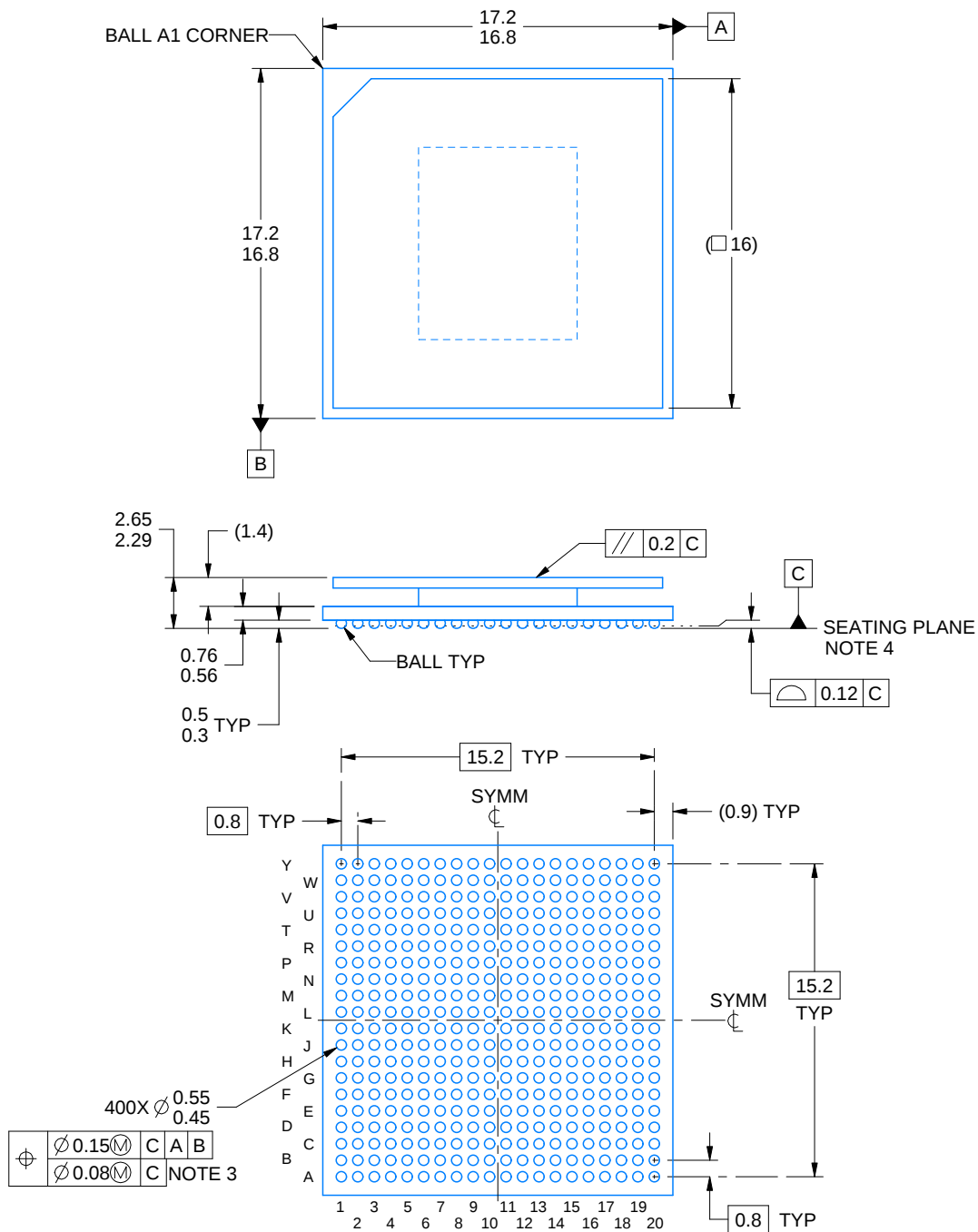
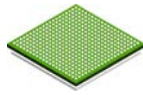
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AFE7951IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7951IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7951IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7951IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



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NOTES:

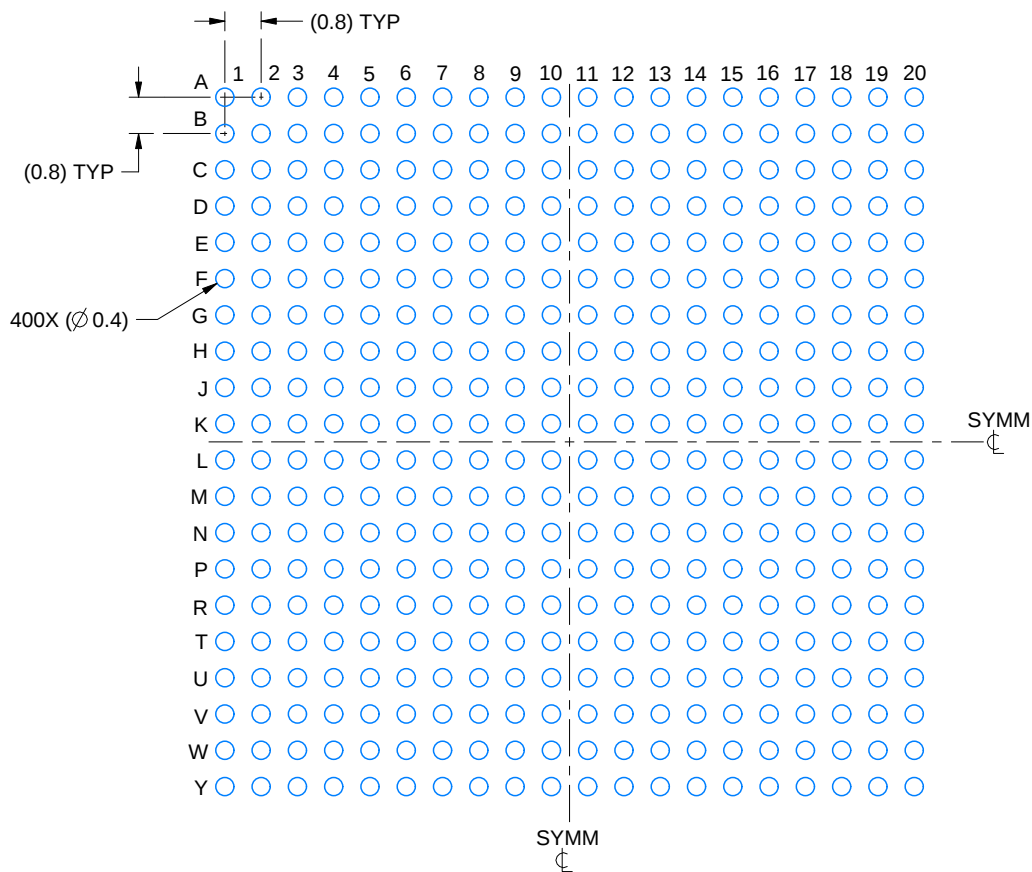
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

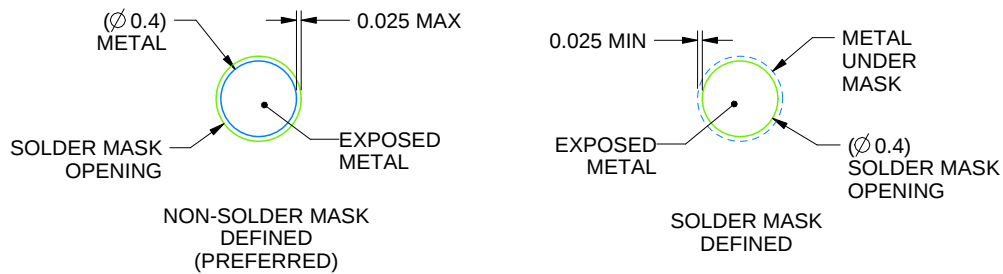
ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

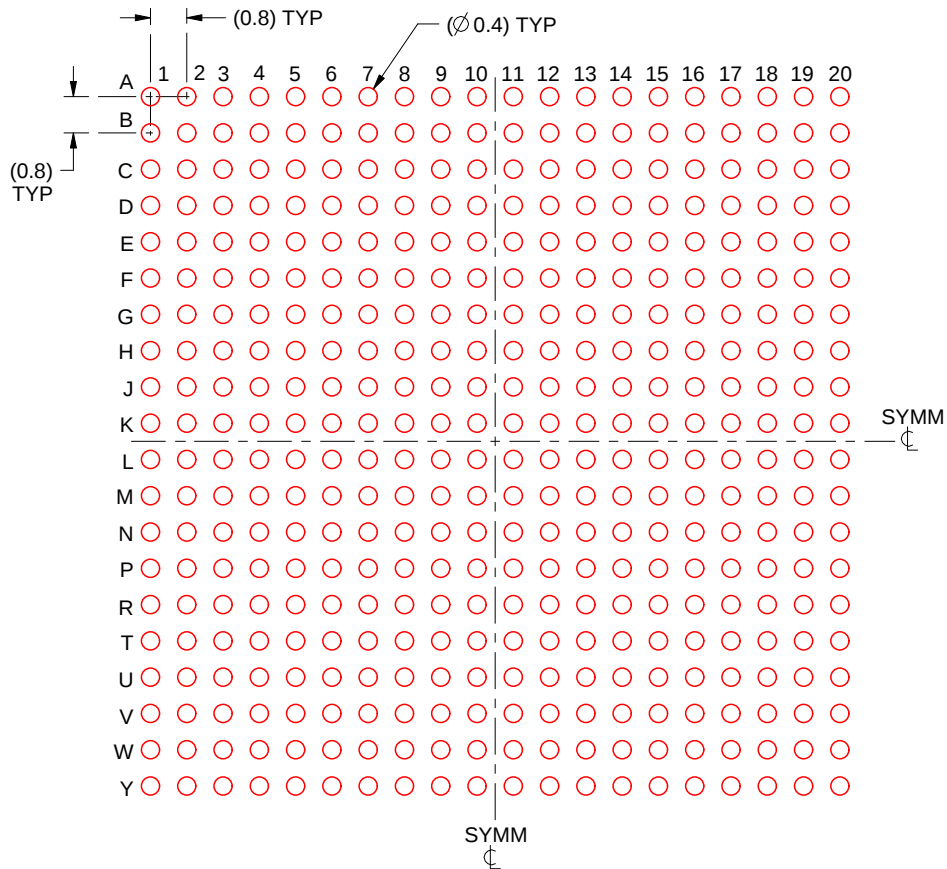
6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY

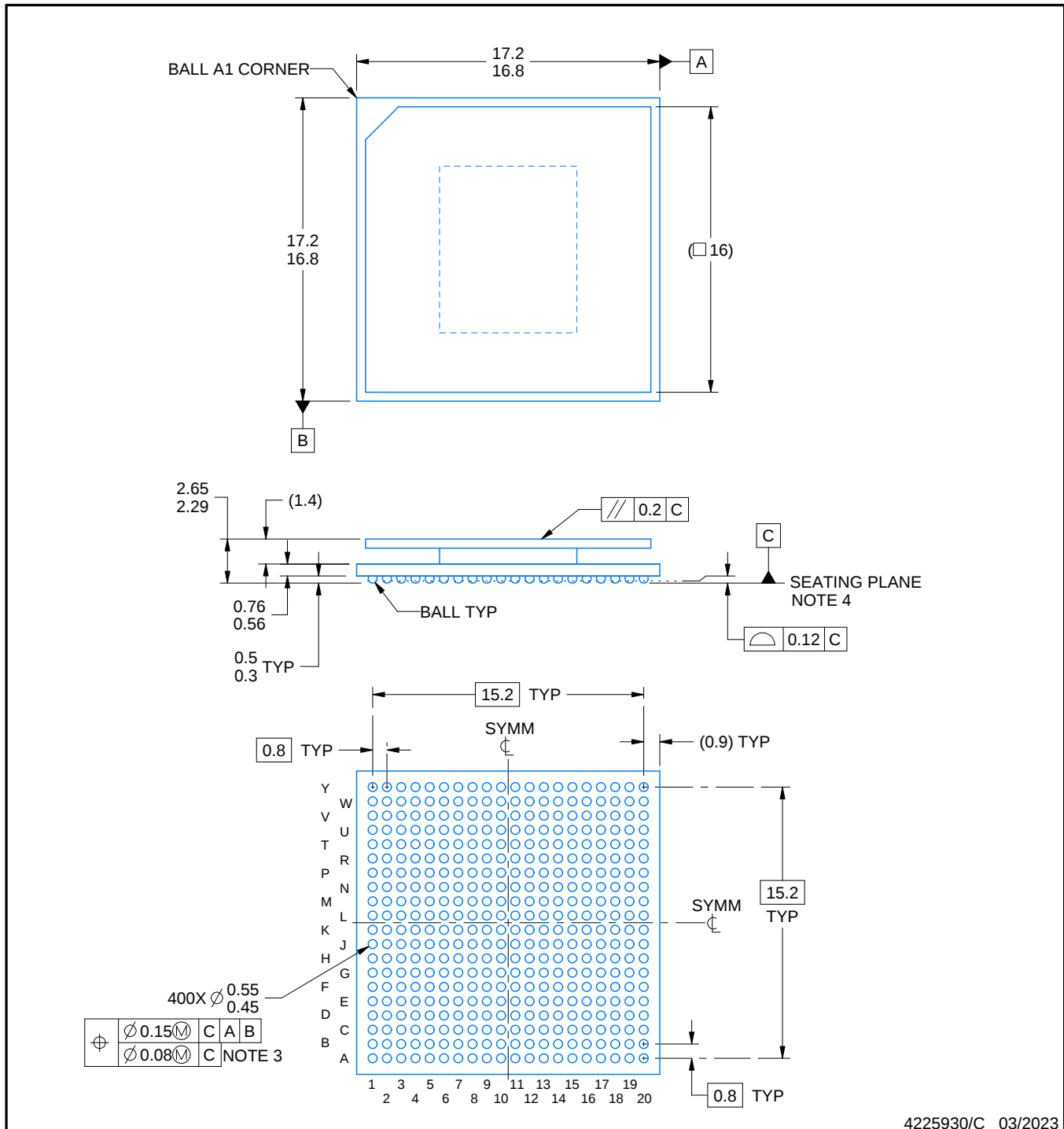
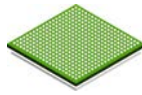


SOLDER PASTE EXAMPLE
 BASED ON 0.15 mm THICK STENCIL
 SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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NOTES:

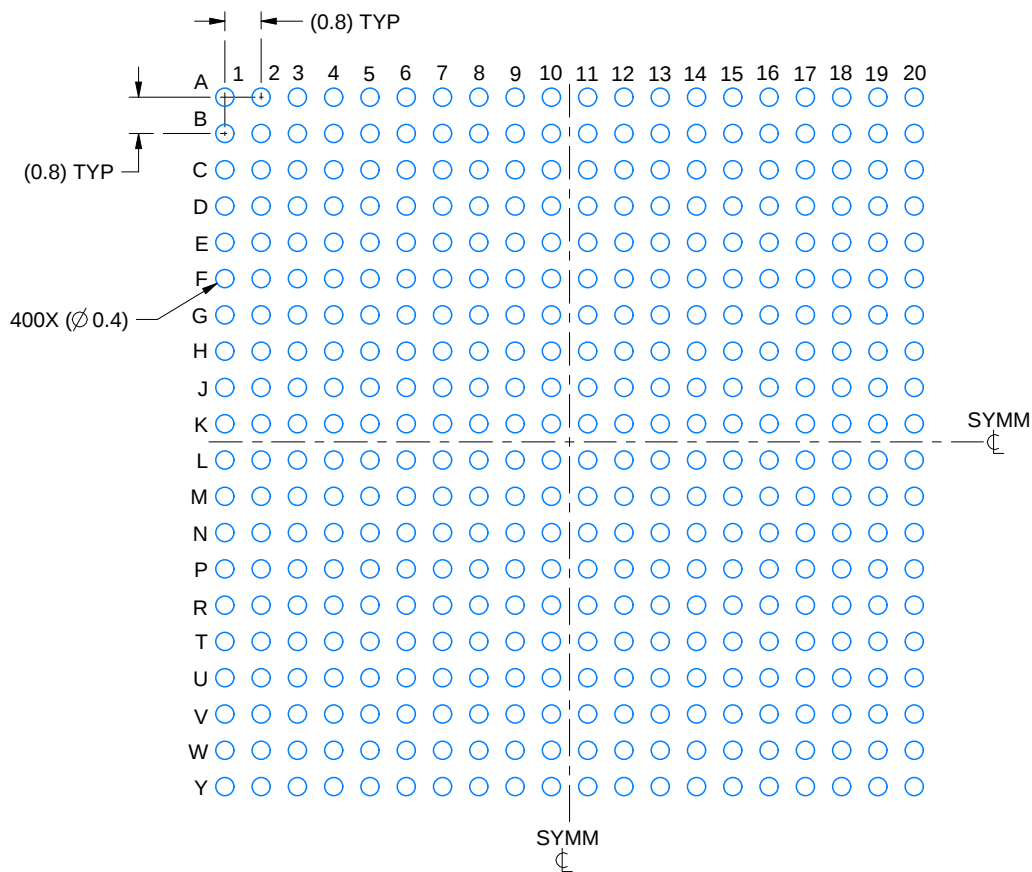
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

EXAMPLE BOARD LAYOUT

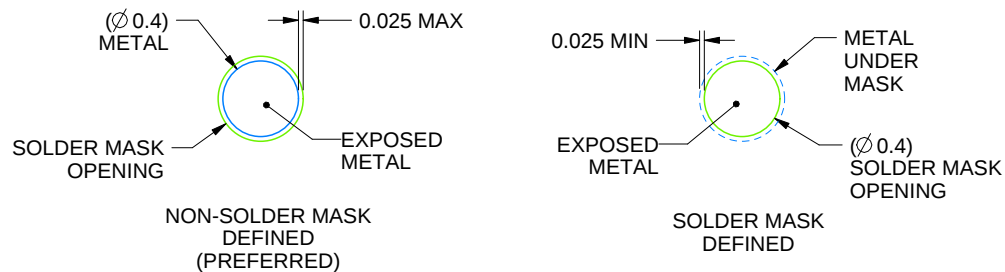
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

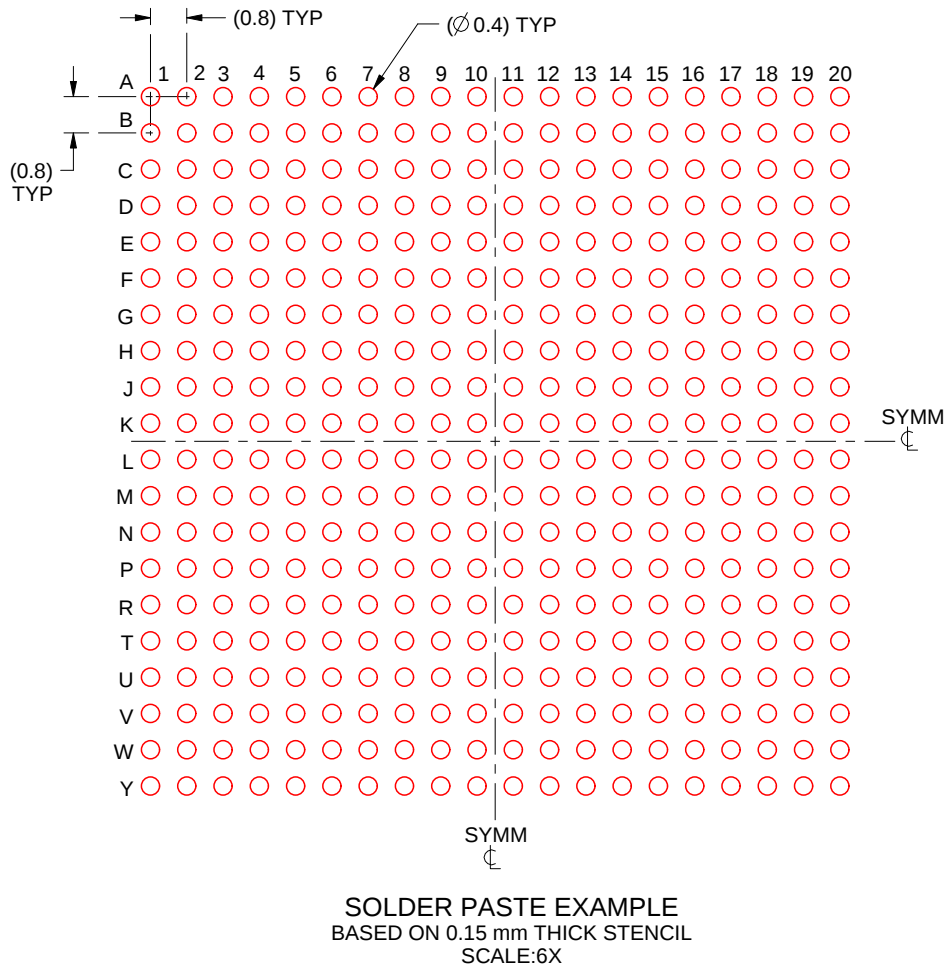
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).

EXAMPLE STENCIL DESIGN

ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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