

Precision Quad SPDT Analog Switch

DESCRIPTION

The DG333A, DG333AL consist of four independently controlled single-pole double-throw analog switches. These monolithic switch is designed to control analog signals with a high degree of accuracy. The DG333A, DG333AL minimize measurement errors by offering low on-resistance ($25\ \Omega$ typ.), low leakage ($20\ \text{pA}$ typ.) and low charge injection performance. The DG333AL features micro-power operation ($< 1\ \mu\text{W}$ typ.). This is ideal for battery operated systems. Pin 15 is not connected on the DG333A.

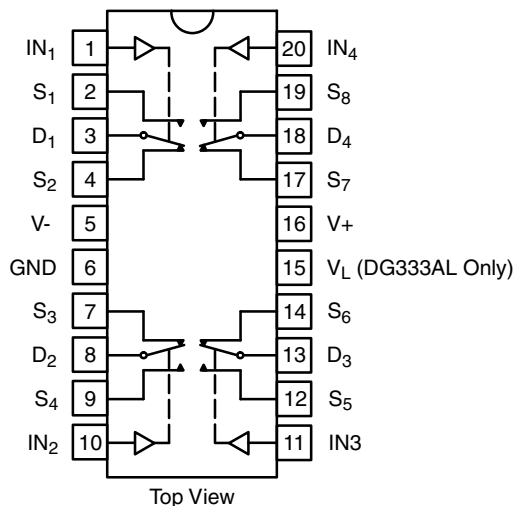
An improved charge injection compensation design minimizes switching transients. These switches can handle up to $\pm 22\ \text{V}$ signals and have an improved continuous current of $30\ \text{mA}$.

The DG333A, DG333AL is fabricated in Vishay Siliconix's proprietary HVSG-2 CMOS process, resulting in higher speed and lower power consumption. An epitaxial layer prevents latchup. Each switch conducts equally well in both directions when on. When off, they block voltages up to the power-supply levels.

BENEFITS

- Rail-to-rail analog signal range
- Simple logic interface
- High precision and accuracy
- Minimal transients
- Low distortion
- Reduced power consumption
- Improved reliability
- Break-before-make switching action

DUAL-IN-LINE, WIDE-BODY SOIC AND TSSOP



FEATURES

- $\pm 22\ \text{V}$ supply voltage range
- TTL and CMOS compatible logic
- Low on-resistance ($25\ \Omega$)
- On-resistance matched between channels ($< 2\ \Omega$)
- Flat on-resistance over analog signal range ($\Delta < 3\ \Omega$)
- Low charge injection ($1\ \text{pC}$)
- Low leakage ($0.2\ \text{nA}$)
- Fast switching ($175\ \text{ns}$)
- Single-supply operation ($5\ \text{V}$ to $40\ \text{V}$)
- ESD tolerance $> 2\ \text{kV}$ per 3015.x
- Low power ($< 1\ \mu\text{A}$) - DG333A, DG333AL

APPLICATIONS

- Audio switching
- Test equipment
- Portable instrumentation
- Communication systems
- PBX, PABX
- Computer peripherals
- Mass storage systems
- Switched-capacitor networks
- Battery-powered systems

TRUTH TABLE

LOGIC	SW1, 4, 5, 8 NORMALLY OPEN	SW2, 3, 6, 7 NORMALLY CLOSED
0	Off	On
1	On	Off

Note

- Logic "0" $\leq 0.8\ \text{V}$
Logic "1" $\geq 2.4\ \text{V}$

**ORDERING INFORMATION**

TEMP. RANGE	PACKAGE	PART NUMBER ^a
-40 °C to +85 °C	20-pin plastic DIP	DG333ADJ-E3
		DG333ALDJ-E3
	20-pin wide-body SOIC (shipped in tubes)	DG333ADW-E3
		DG333ALDW-E3
	20-pin wide-body SOIC (shipped in tape and reel)	DG333ADW-T1-E3
		DG333ALDW-T1-E3
	20-Pin TSSOP (shipped in tape and reel)	DG333ADQ-T1-E3
		DG333ALDQ-T1-E3

Note

a. For standard tin / lead external termination, remove the "-E3" from the ordering part number

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Voltages referenced V ₊ to V ₋		44	V
GND		30	
V ₊ to GND		40	
Digital inputs ^a V _S , V _D		(V ₋) - 2 to (V ₊) + 2 or 30 mA, whichever occurs first	
Current, any terminal		30	mA
Peak current S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage temperature		-65 to +125	°C
Power dissipation (package) ^b	20-pin plastic DIP ^c	890	mW
	20-pin wide SOIC ^d	800	

Notes

- a. Signals on S_X, D_X, or IN_X exceeding V₊ or V₋ will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 12 mW/°C above 75 °C
d. Derate 10 mW/°C above 75 °C

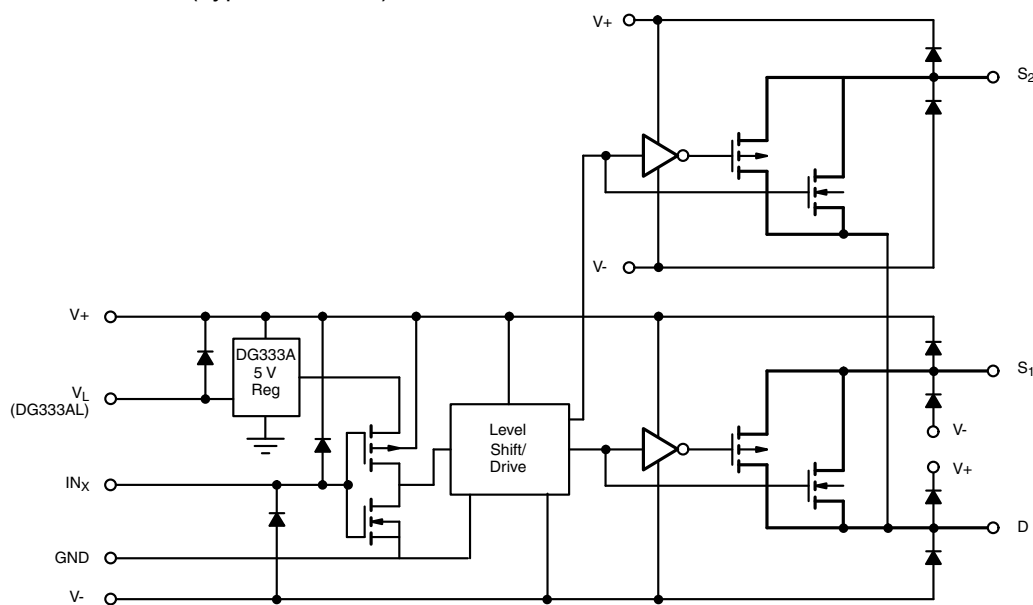
SCHEMATIC DIAGRAM (Typical channel)

Fig. 1



SPECIFICATIONS							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V ₊ = 15 V, V ₋ = -15 V V _{IN} = 2.4 V or 0.8 V ^e	TEMP. ^a	LIMITS D SUFFIX -40 °C to +85 °C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	V _{ANALOG}		Full	V-	-	V+	V
Channel on-resistance	R _{DS(on)}	I _S = -10 mA, V _D = ± 10 V	Room	-	25	45	Ω
			Full	-	-	90	
On-resistance flatness		I _S = -10 mA, V _D = ± 5 V V ₊ = 16.5 V, V ₋ = -16.5 V	Room	-	-	3	
			Full	-	-	5	
R _{DS(on)} match between channels ^f	ΔR _{DS(on)}	I _S = -10 mA, V _D = ± 10 V	Room	-	-	2	
			Full	-	-	4	
Source off leakage current	I _{S(off)}	V _D = 15.5 V, V _S = 15.5 V V ₊ = 16.5 V, V ₋ = -16.5 V	Room	-0.25	-	0.25	nA
			Hot	-20	-	20	
Channel on leakage current	I _{D(on)}	V _D = ± 15.5 V, V _{S(open)} = ± 15.5 V V ₊ = 16.5 V, V ₋ = -16.5 V	Room	-0.75	-	0.75	
			Hot	-60	-	60	
Digital Control							
Input voltage high	V _{INH}		Full	2.4	-	-	V
Input voltage low	V _{INL}		Full	-	-	0.8	
Input current	I _{INL} or I _{INH}	V _{INH} or V _{INL}	Full	-1	-	1	μA
Dynamic Characteristics							
Turn-on time	t _{ON}	See switching time test circuit see figure 2	Room	-	-	175	ns
Turn-off time	t _{OFF}		Room	-	-	145	
Break-before-make time delay	t _D	See figure 3	Room	5	-	-	pC
Charge injection ^d	Q	C _L = 10 nF, V _{gen} = 0 V, R _{gen} = 0 Ω	Room	-	-	10	
Off-isolation	OIRR	R _L = 75 Ω, C _L = 5 pF, V _D = 2.3 V _{RMS} , f = 1 MHz	Room	-	72	-	dB
Channel-to-channel crosstalk	X _{TALK}		Room	-	80	-	
Off capacitance	C _{OFF}	f = 1 MHz, V _S = 0 V	Room	-	8	-	pF
Channel on capacitance	C _{ON}		Room	-	12	-	
Power Supplies							
Positive supply current	I ₊	DG333A: V _{IN} = 0 V or 5 V	Room	-	-	200	μA
Negative supply current	I ₋		Room	-1	-	-	
Positive supply current	I ₊	DG333AL: V _{IN} = 0 V or 5 V, V _L = 5 V	Room	-	-	1	
Logic supply current	I _L		Room	-	-	1	
Negative supply current	I ₋		Room	-1	-	-	
Supply voltage range	V ₊ /V ₋		Full	± 4	-	± 22	

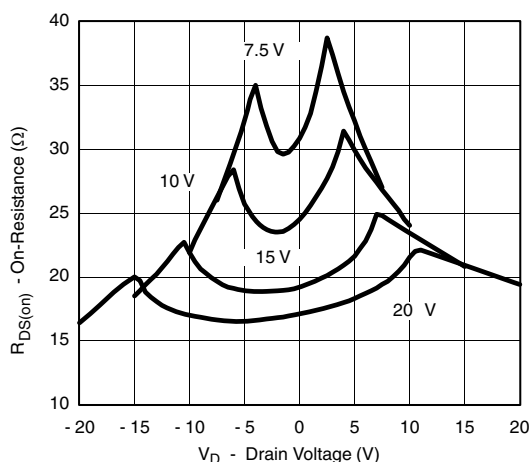
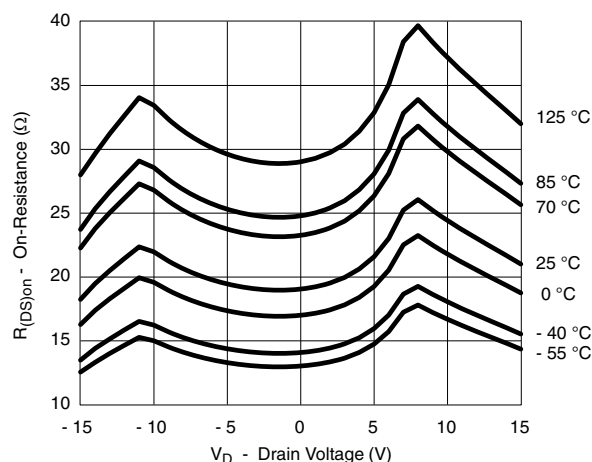


SPECIFICATIONS (Unipolar Supplies)							
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 12 V, V- = 0 V T _A = 25°C	TEMP. ^a	LIMITS D SUFFIX -40 °C to +85°C			UNIT
				MIN. ^b	TYP. ^c	MAX. ^b	
Analog Switch							
Analog signal range ^d	V _{ANALOG}		Full	V-	-	V+	V
Channel on-resistance	R _{DS(on)}	I _S = -10 mA, V _D = 10, 1 V	Room	-	35	75	Ω
Source off leakage current	I _{S(off)}	V _D = 11 V, V _{S(open)} = 1 V	Room	-	-	0.25	nA
Channel on leakage current	I _{D(on)}	V _D = 11 V, V _{S(open)} = 0 V V _D = 1 V, V _{S(open)} = V+	Room	-	-	0.75	
Dynamic Characteristics							
Turn-on time	t _{on}	See switching time test circuit see figure 2	Room	-	90	-	ns
Turn-off time	t _{off}		Room	-	45	-	
Break-before-make time delay	t _D	See figure 3	Room	5	10	-	
Power Supplies							
Positive supply current	I ₊	DG333A: V _{IN} = 0 V or 5 V	Room	-	-	200	μA
			Room	-	-	1	
Positive supply current	I ₊	DG333AL: V _{IN} = 0 V or 5 V, V _L = 5 V	Room	-	-	1	
Logic supply current	I _L		Room	-	-	1	
Positive supply range	V ₊		Room	5	-	40	V

Notes

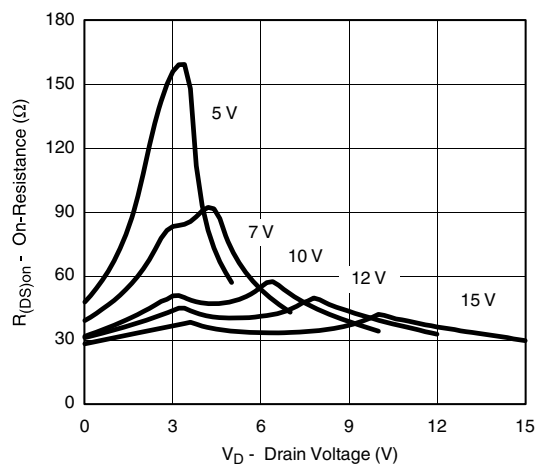
- Room = 25 °C, Full = as determined by the operating temperature suffix
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
- Guaranteed by design, not subject to production test
- V_{IN} = input voltage to perform proper function
- On-resistance match and flatness are guaranteed only for bipolar supply operation

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

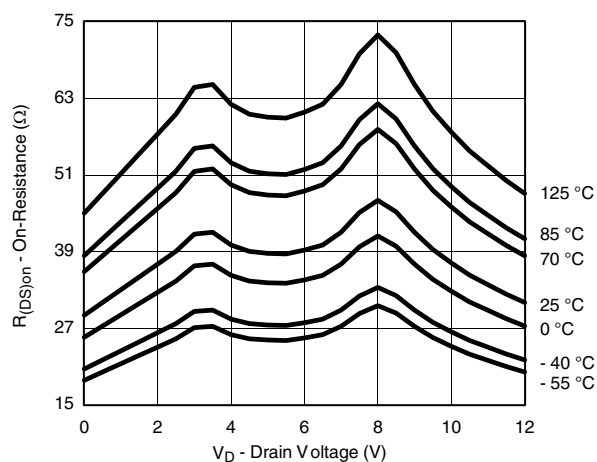
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted) **$R_{\text{DS(on)}}$ vs. V_D (Dual Supply)** **$R_{\text{DS(on)}}$ vs. V_D and Temperature (Dual Supply)**



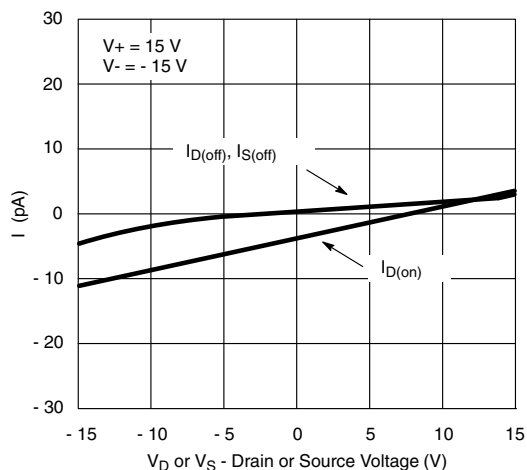
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



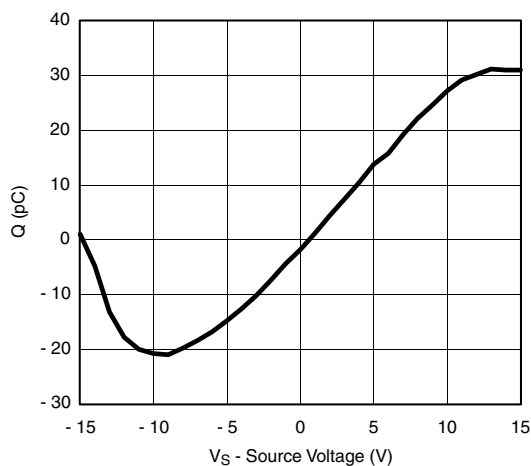
$R_{DS(on)}$ vs. V_D (Single Supply)



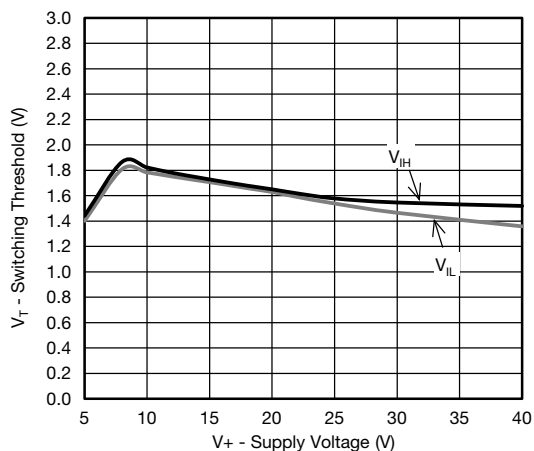
$R_{DS(on)}$ vs. V_D and Temperature (Single Supply)



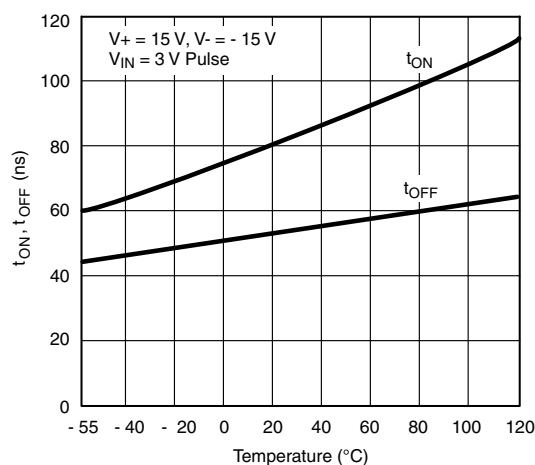
Leakage Current vs. Analog Voltage



Drain Charge Injection



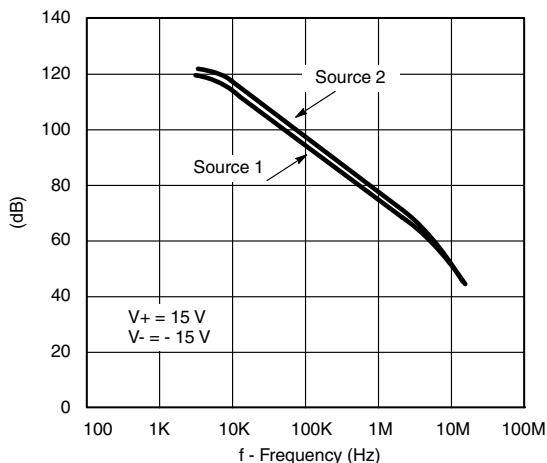
Input Switching Threshold vs. Supply Voltage



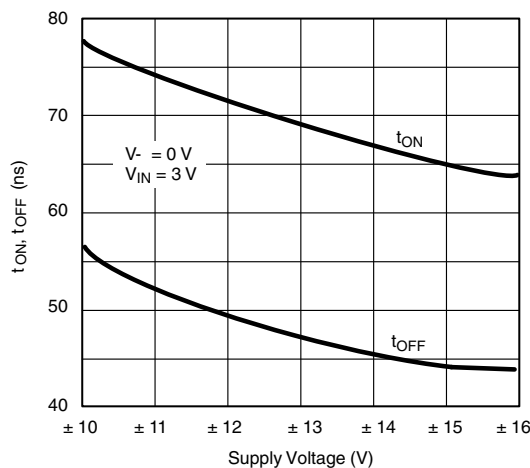
Switching Time vs. Temperature



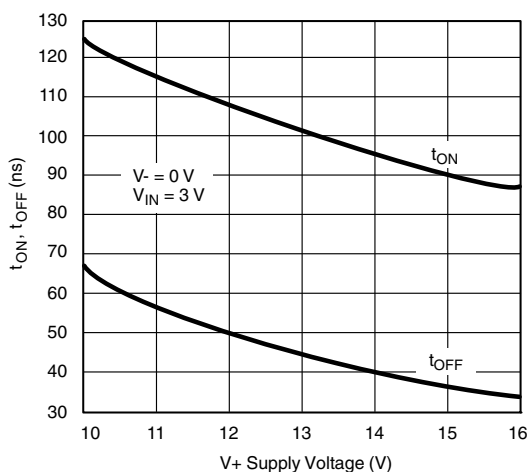
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



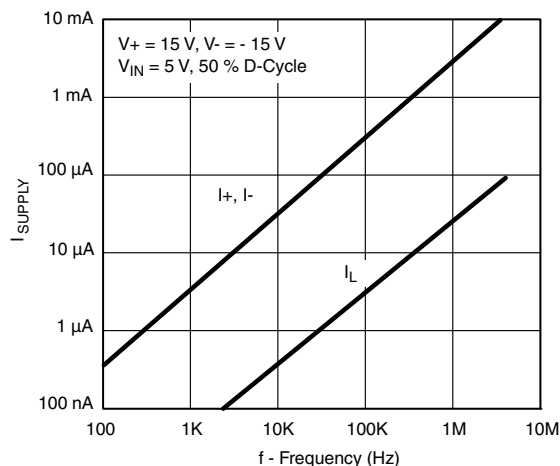
Crosstalk and Off Isolation vs. Frequency



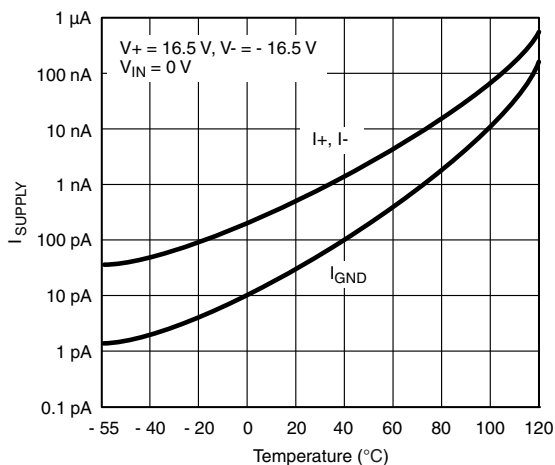
Switching Time vs. Supply Voltages



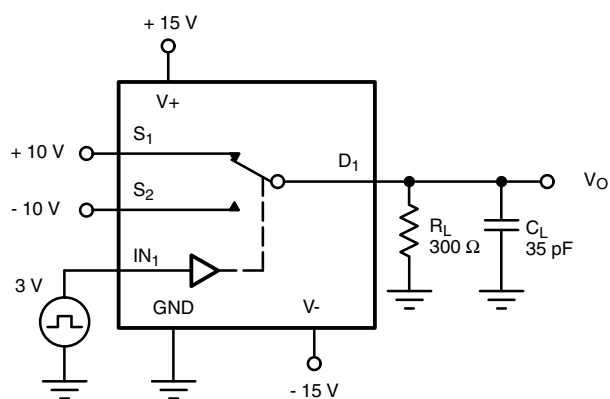
Switching Time vs. V_+



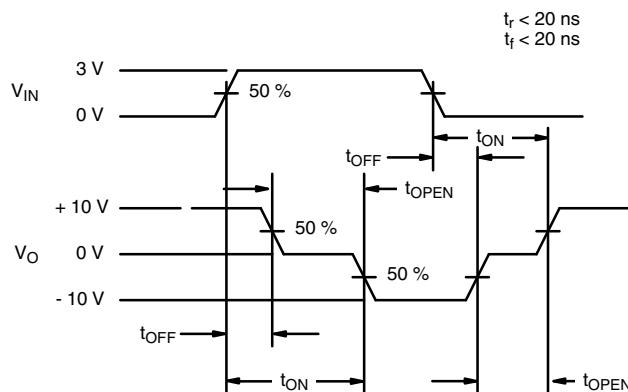
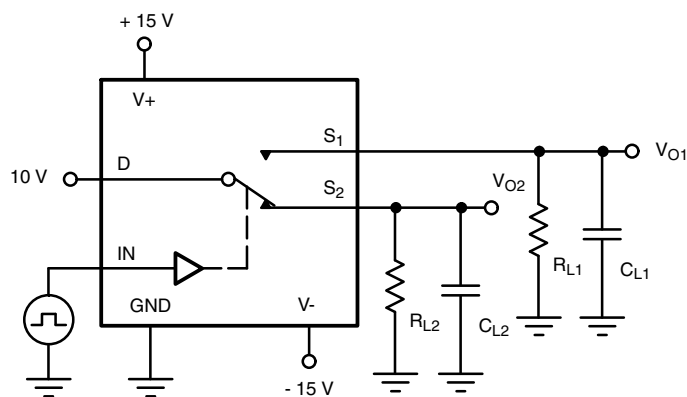
Power Supply Currents vs. Switching Frequency



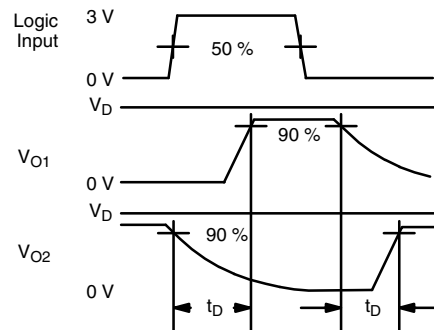
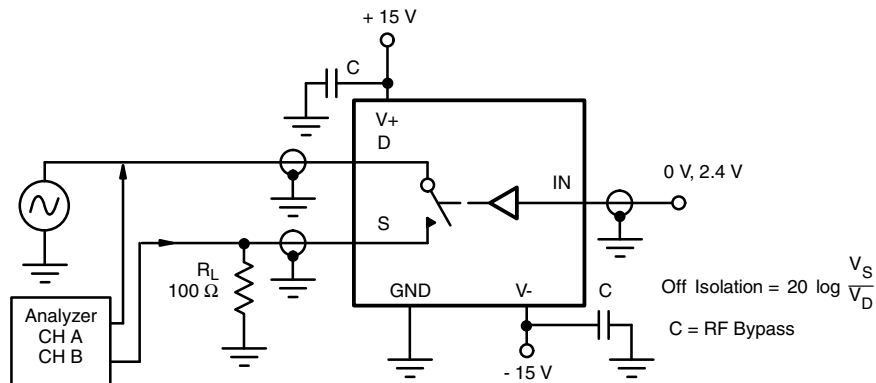
Supply Current vs. Temperature

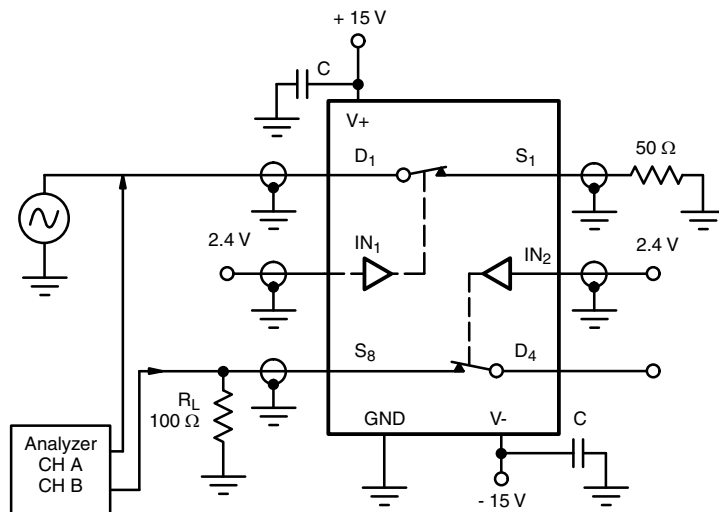
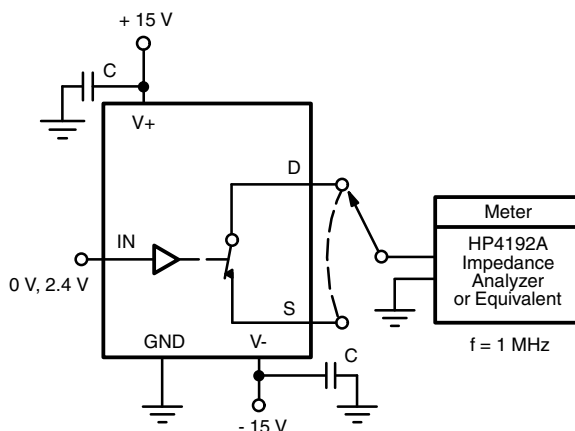
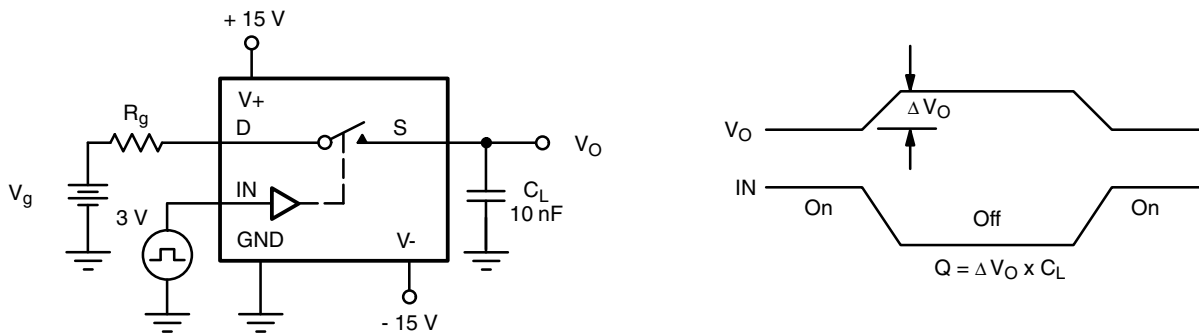
TEST CIRCUITS


Repeat Test for IN_2 , IN_3 and IN_4


Fig. 2 - Switching Time


$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$
 C_L (includes fixture and stray capacitance)


Fig. 3 - Break-Before-Make

Fig. 4 - Off Isolation

TEST CIRCUITS

Fig. 5 - Crosstalk

Fig. 6 - Capacitances

Fig. 7 - Charge Injection

APPLICATIONS

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG333A, DG333AL allow for higher clock rates and consequently higher filter operating frequencies. Figure 8 shows two capacitors being switched.

The DG333A, DG333AL is capable of switching four capacitors.

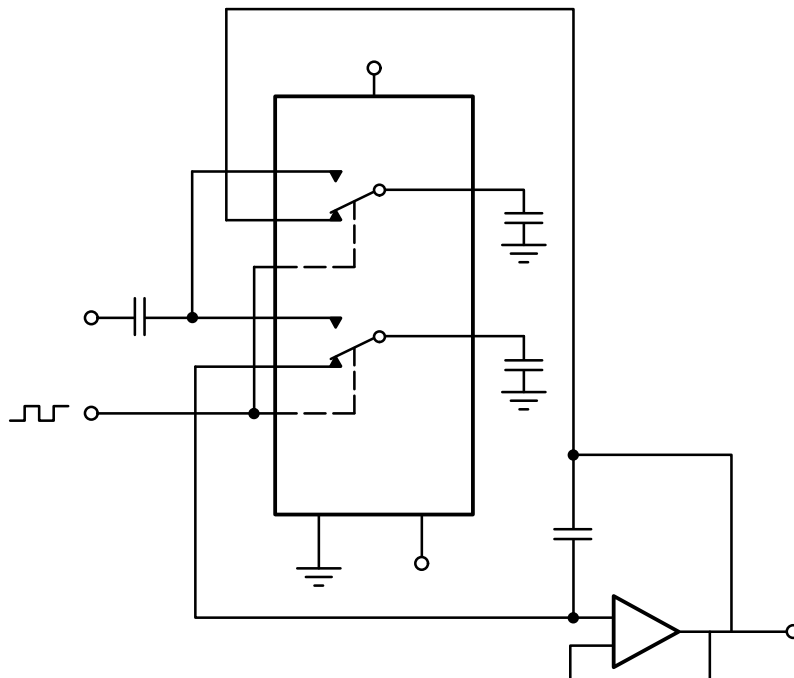


Fig. 8 - Band-Pass Switched Capacitor Filter

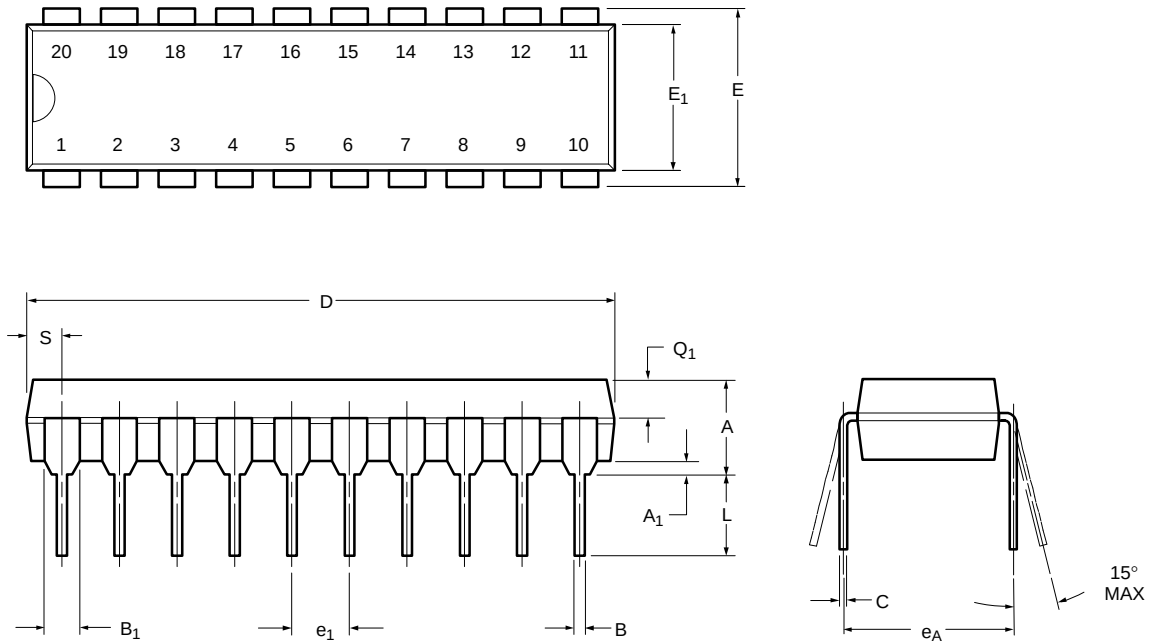
**PRODUCT SUMMARY**

Part number	DG333A	DG333A	DG333AL	DG333AL
Status code	2	2	2	2
Configuration	SPDT x 4	SPDT x 4	SPDT x 4	SPDT x 4
Single supply min. (V)	5	5	5	5
Single supply max. (V)	36	36	36	36
Dual supply min. (V)	5	5	5	5
Dual supply max. (V)	22	22	22	22
On-resistance (Ω)	25	25	25	25
Charge injection (pC)	10	10	10	10
Source on capacitance (pF)	12	12	12	12
Source off capacitance (pF)	8	8	8	8
Leakage switch on typ. (nA)	-	-	-	-
Leakage switch off max. (nA)	0.25	0.25	0.25	0.25
-3 dB bandwidth (MHz)	-	-	-	-
Package	SO-20 (wide)	TSSOP-20	SO-20 (wide)	TSSOP-20
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes
Turn on time max. (ns)	175	175	175	175
Crosstalk and off isolation	-72	-72	-72	-72

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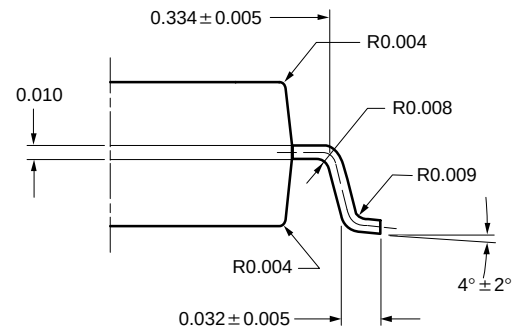
PDIP: 20-LEAD



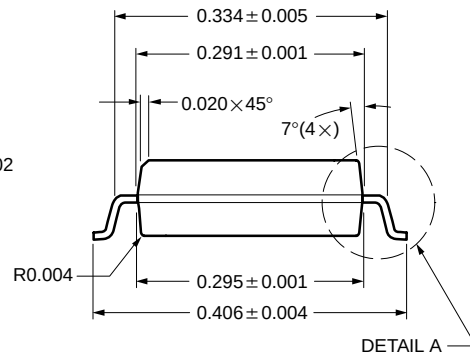
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A ₁	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B ₁	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	24.89	26.92	0.980	1.060
E	7.62	8.26	0.300	0.325
E ₁	5.59	7.11	0.220	0.280
e ₁	2.29	2.79	0.090	0.110
e _A	7.37	7.87	0.290	0.310
L	3.175	3.81	0.123	0.150
Q ₁	1.27	2.03	0.050	0.080
S	1.02	2.03	0.040	0.080

ECN: S-03946—Rev. B, 09-Jul-01
DWG: 5484

ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5848



Technical drawing of a 10-hole punch. The drawing shows a side view of the punch with ten holes. The overall length is 0.504 ± 0.001 . The distance between the centers of the first and last holes is 0.504 ± 0.001 . The distance between the centers of adjacent holes is 0.017 ± 0.0003 . The diameter of the punch is 0.091 ± 0.001 . The diameter of the holes is 0.041 ± 0.001 . The thickness of the punch is 0.006 ± 0.002 . The distance from the center of the first hole to the left edge is 0.050 TYP. The distance from the center of the last hole to the right edge is 0.098 ± 0.002 . The drawing also shows a cross-section of the punch with a diameter of 0.091 ± 0.001 and a thickness of 0.006 ± 0.002 .



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